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NOVEL RF PHASE DETECTOR FOR ACCELERATOR APPLICATIONS

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Abstract

A novel phase detector has been developed that is suitable for use in an rf phase locked loop for locking an rf source to an rf accelerator structure or phase locking the accelerator structure to a fixed or adjustable frequency rf source. It is also useful for fast phase feedback to control the phase of an accelerator rf field. The principle is applicable to a wide range of frequencies and amplitudes. The phase is uniquely and unambiguously determined over 360°, eliminating the need for external phase shifters or phase references. The operation of this phase detector is described in detail. An application is described that uses a DDS-based LLRF source as the rf input to a high-power rf system.

THEORY OF OPERATION

Introduction

Phase locked loops are often used for frequency control of accelerators. What is required is to generate an error signal that passes linearly through zero at the desired frequency. This usually involves a phase detector with a reference phase that must be set to zero at the operating frequency, compensating for the phase shift in external components. There are systems that measure phase with timed phase detectors that use a reference frequency to obtain sine and cosine data.

We describe an analog/digital phase detector that measures the phase over a 360° range without an external phase reference and can be used to phase lock an rf source to a cavity or vice versa. This eliminates complicated setups since the circuit can be used to phase lock at any angle.

Phase Detector Circuit

Figure1 is a schematic for a coupled line 3 dB hybrid coupler. The schematic shows how the outputs are related to the inputs for the lossless case. For a real hybrid coupler, the attenuations to each output don't necessarily match and there can be a few degrees phase error.

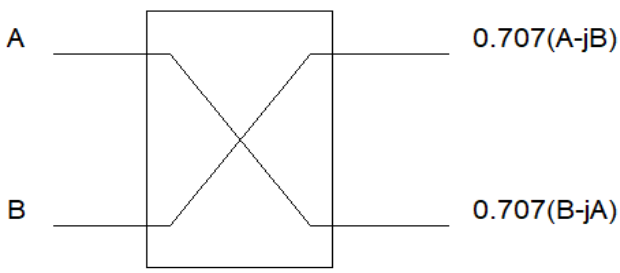

Figure 1: Hybrid coupler outputs relative to inputs.

Figure 2 shows the complete rf circuit of the JPAW phase detector.

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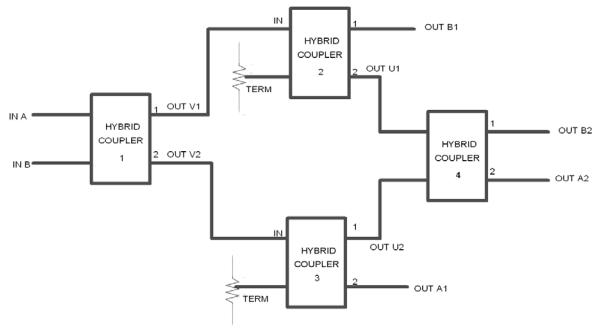

Figure 2: JPAW phase detector circuit.

The circuit has two inputs, A and B, and four outputs A1, B1, B2, and A2. Intermediate signals are labeled V1, V2, U1, and U2.

From the definition of a lossless, perfectly balanced 3dB hybrid coupler [1]

$$V1 = \frac{1}{\sqrt{2}}(A - jB) \;\&\; V2 = \frac{1}{\sqrt{2}}(B - jA) .$$

The outputs B1 and A1 are

$$B1 = \frac{1}{2}(A - jB) \;\&\; A1 = -\frac{1}{2}(A + jB) .$$

Outputs B2 and A2 are

$$B2 = -\frac{1+j}{2\sqrt{2}}(B + A) \;\&\; A2 = \frac{1+j}{2\sqrt{2}}(B - A) .$$

We then define S and C as:

$$S = |A1|^2 - |B1|^2 = A1A1^* - B1B1^* = \frac{1}{2}jA(B - B^*) ,$$

$$C = |A2|^2 - |B2|^2 = A2A2^* - B2B2^* = \frac{1}{2}A(B + B^*) .$$

With inputs A and B

$$A = A_0 \;\&\; B = B_0(\cos(\phi) + j\sin(\phi)) ,$$

we see that

$$S = A_0B_0\sin(\phi) \;\&\; C = A_0B_0\cos(\phi) .$$

Since we can directly calculate $\sin(\phi)$ and $\cos(\phi)$ we can uniquely determine the phase angle over a full 360° range. These simple calculations can be performed by a microcontroller or FPGA.

PHASE DETECTOR APPLICATION

Low Level RF Source

One application of the phase detector is in a Low Level RF (LLRF) source for an rf linear accelerator. To create a phase-locked rf signal source we need to measure the initial phase angle and compare subsequent measurements to the initial measurement to generate an error signal. The error signal is then used to correct the frequency.

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LLRF Test Circuit

To test the phase detector, we used a special version of a LLRF unit with two outputs. Both outputs are individually adjustable in amplitude and phase. Figure 3 shows the configuration for testing characteristics of the phase detector.

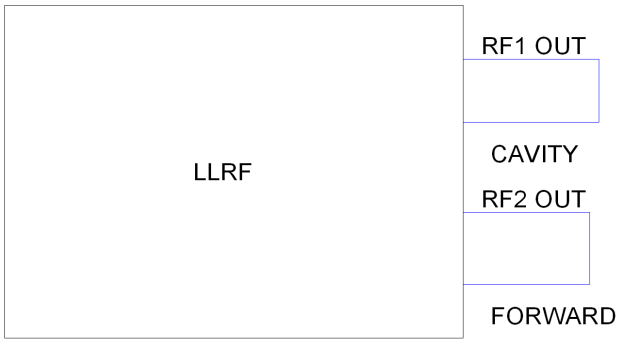

Figure 3: LLRF setup for testing the phase detector.

The two outputs RF1 and RF2 are connected, respectively, to the CAVITY and FORWARD AMPLITUDE inputs with the output level adjusted to be with in the range of the amplitude detectors and the ADC. RF2 is the reference signal and RF1 simulates a signal phase shifted with respect to the reference. The phase of the FORWARD signal was adjusted so that the amplitude of the S signal is 0 at 0° phase of the CAVITY signal.

Figure 4 is a plot of the calculated S and C values for 10° steps in the CAVITY phase. As can be seen in the figure the C signal is close to perfect. The positive and negative excursion of the signal are symmetrical and the curve crosses 0 close to 90° and 270°. The S signal is slightly asymmetrical, but similar in amplitude to the C signal. The 0-voltage point was set at ϕ equals 0° but reaches 0 again slightly short of 180°.

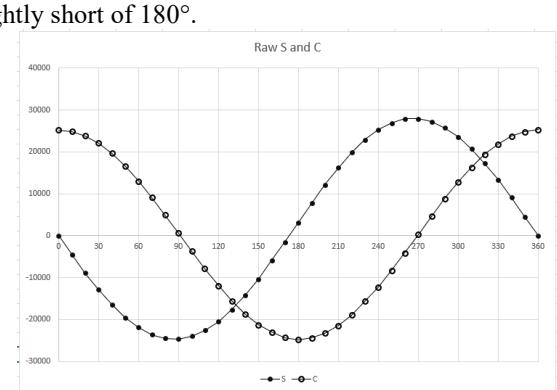

Figure 4: Plot of raw S and C data versus phase angle.

Figure 5 is a plot of the raw C versus S. The distortion is clearly seen in the figure. However, this does not alter the usefulness of the data in generating an error signal for a phase locked loop.

Figure 6 is a plot of the normalized length of vector {S,C}. This also shows the distortion of the data. It should be noted that this version of the LLRF uses Analog Devices ADL5511 detectors to get the RMS amplitude of the signals. The results are considerably better than an earlier version using diode detectors because the ADL5511s have good linearity and low temperature sensitivity.

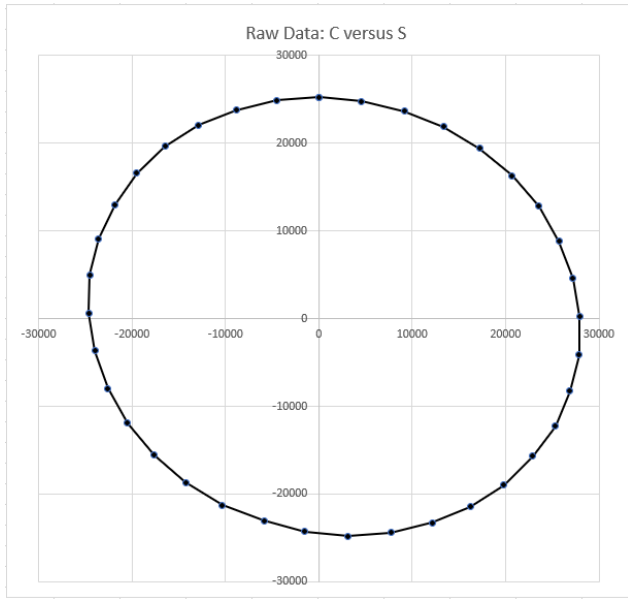

Figure 5: Plot of raw S versus C.

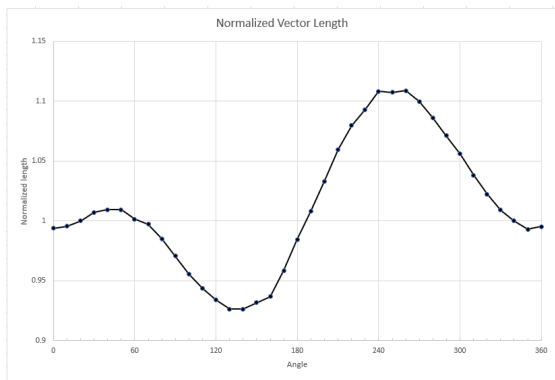

Figure 6: Variation in normalized vector length {S,C}.

Figure 7 is a plot of the measured angle versus the actual angle.

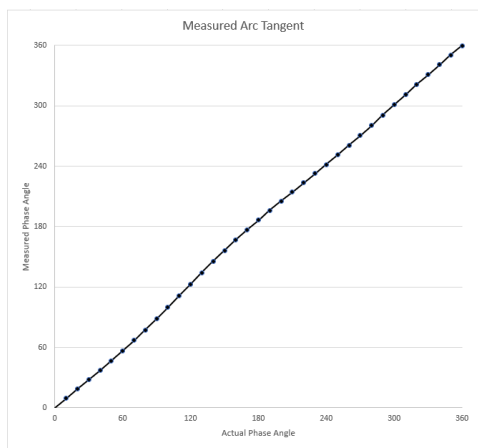

Figure 7: Plot of the measured angle versus input angle.

Error Signal

To use the phase detector in a phase locked loop we need to generate an error signal. The LLRF calculates the values of S and C on every rf pulse. The data is captured in a multichannel Sample and Hold circuit. The data is captured at

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an adjustable time, usually 75% of the pulse length after the start of the pulse.

Although the values of S and C are calculated for every rf pulse, the phase locked loop is initially not activated. The rf frequency is first tuned for maximum cavity field. When the phase lock loop is activated the most recent value of S and C are saved as the reference values S0 and C0. The error is calculated as

$$err = S\,C0 - C\,S0\ .$$

A little trig will show the expression is equivalent to $err = k\sin(\delta\phi)$, where $\delta\phi = \phi - \phi_0$, and k is a scaling constant. This is suitable for an error signal since it clearly goes through 0 linearly with the phase error. The error signal is normalized by dividing by the length of the reference vector $length = \sqrt{S0^2 + C0^2}$, making the error independent of the amplitude of the rf signals. The constant k scales the value so integer arithmetic can be used.

After the phase locked loop is activated, the frequency can be adjusted by rotating the reference phase vector {S0, C0}.

Implementation

The phase locked loop is implemented as a slew-rate limited feedback. When the error limit exceeds a certain value that can be calibrated with respect to frequency the frequency is stepped back in increments of 10% of the limit until the error goes through zero.

Figure 8 shows the measured error signal for a test cavity at 352.5 MHz with a loaded Q of 1200. From the graph the error signal is 27.819 per kHz. That corresponds to about 720 Hz for an error of 20. For the test at 352.5 MHz the error threshold is set to 20. When the error exceeds 20 in either direction the frequency steps back in 100 Hz increments until the error passes through 0.

For a Q of 1200 the frequency shift is approximately 3.9 kHz/°. An error of 720 Hz corresponds to a phase shift of 0.18°, which is much smaller than the phase stability requirements for multi-cavity accelerators.

One approach to frequency control for ion linacs is to phase lock the rf source to the RFQ accelerator. The subsequent DTL or CCDTL accelerators are phased locked to the operating frequency with slug tuners. The slew rate limited feedback is natural for stepper motor driven slug tuners. When the frequency error exceeds the threshold the slug tuner motor is turned on and runs until the frequency error passes through zero. The same phase detector works the same whether the frequency is controlled at the rf source or using slug tuners to vary the frequency of the accelerator structure.

The phase detector can also be used to stabilize the phase during a pulse with linear feedback or a feed forward control.

Error Sensitivity Versus Phase Angle

Figure 9 is a plot of the normalized error sensitivity over the 360°range, indicating that the feedback loop gain is nearly independent of the initial reference phase. The error sensitivity is the magnitude of the vector difference between two adjacent data points spaced 10° and normalized to an average value of 1.

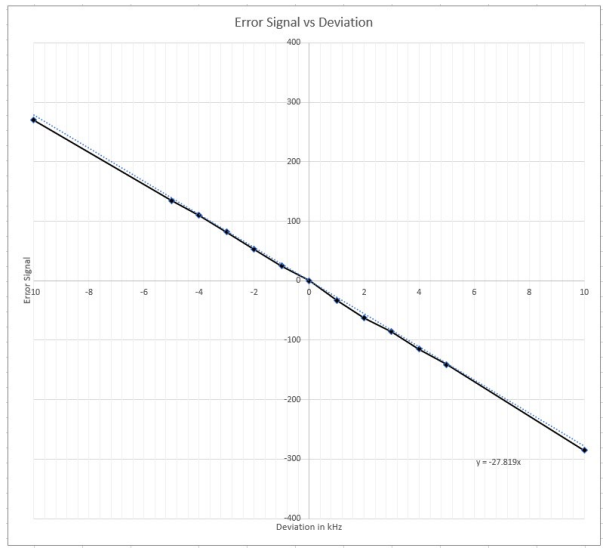

Figure 8: Error signal versus frequency deviation.

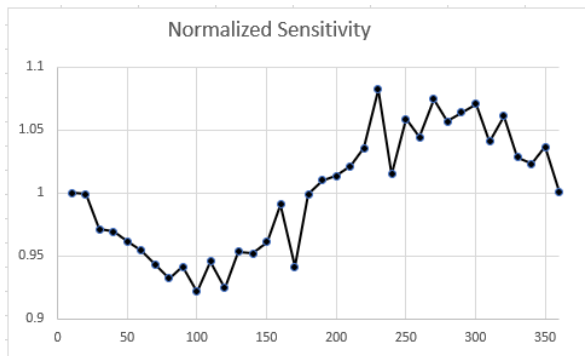

Figure 9: Normalized error sensitivity.

CONCLUSION

We have described the circuit for an analog/digital phase detector utilizing 90° hybrid couplers and linear rf detectors that measures the phase difference between two rf signals over a 360° range. We also described a phase locked rf system utilizing this detector that can be phase locked at any angle without external phase shifters. The detector can respond rapidly enough using a multi-channel simultaneous ADC to be useful in a fast phase control for phase feedback or feed forward control during an rf pulse.

The 360° phase detector described in this paper is a development of JP Accelerator Works, Inc.

REFERENCES

[1] D. Pozar, “Power dividers and directional couplers” in *Microwave Engineering*, New York, NY, USA: Wiley, 1998, p. 379.