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FRIB AND UEM LLRF CONTROLLER UPGRADE*

S. Kunjir†, E. Bernal, D. Morris, S. Zhao, FRIB, Michigan State University, East Lansing, MI, USA
C-Y. Ruan, Dept. of Physics and Astronomy, Michigan State University, East Lansing, MI, USA

Abstract

The Facility for Rare Isotope Beams (FRIB) is developing a 644 MHz superconducting (SC) cavity for a future upgrade project. The current low level radio frequency (LLRF) controller at FRIB is not able to operate at 644 MHz. The Ultrafast Electron Microscope (UEM) laboratory within the Department of Physics at Michigan State University designed an LLRF controller based on analog RF components to operate a 1.013 GHz room temperature (RT) cavity. With requirements for improved stability, performance and user controls there was a need to upgrade the analog LLRF controller. The FRIB radio frequency (RF) group designed, developed and fabricated a new digital LLRF controller, with high-speed serial interface between system on chip field programmable gate array and fast data converters and capable of high frequency direct sampling, to meet the requirements of 644 MHz SC cavity and 1.013 GHz UEM RT cavity. This paper gives an overview of the upgraded digital LLRF controller, its features, improvements and preliminary test results.

INTRODUCTION

The Facility for Rare Isotope Beams (FRIB) conducted the first user scientific experiment in May 2022 [1]. It will make the majority (~80%) of the isotopes predicted to be bound available for experiments. These isotopes will allow researchers to understand atomic nuclei and their role in the Universe. "The tremendous discovery potential of FRIB can be further extended with an energy upgrade of the FRIB linear accelerator to 400 MeV/u and to higher energies for lighter ions (FRIB400)" [2]. Figure 1 shows footprint of the current (green and black) and upgraded (blue) FRIB linac.

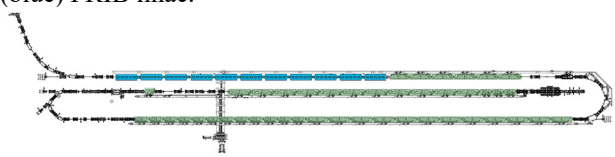

Figure 1: FRIB400 future upgrade.

The Ultrafast Electron Microscope [3] laboratory conducts research on nanoscale material processes at the fundamental length and time scales and studies the mechanisms of phase transitions (atomic and electronic) in low-dimensional systems, the photo-generated hot electron dynamics at interfaces, and the far-from-equilibrium phenomena that involve multiscale, inter-correlated channels of atomic and electronic relaxations following the creation of an excited state in complex and mostly nanostructured solids.

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† kunjir@frib.msu.edu

MOTIVATION

The current LLRF controllers in operation at FRIB were fabricated in 2016 and support frequencies only between 40.25 MHz and 322 MHz. This is in part due to the limitation of multiple integrated chip (IC) specifications and design requirements. For example, on the current controller, the maximum sampling frequency of analog to digital converter (ADC) is 65 MSPS and digital to analog converter (DAC) is 400 MSPS. With the development of higher frequency cavity for the future upgrade and the requirement of migration from analog LLRF control to digital for UEM, the overarching motivation to upgrade the LLRF controller was the need to support higher frequency operation; 644 MHz for FRIB400 and 1.013 GHz for UEM.

LLRF DESIGN

One of the requirements for the development of a new LLRF controller was to leverage the latest technologies available for FPGAs and data converters with the goal of designing a controller that can be configured as a replacement of current RF systems as well as new higher frequency systems. Another significant requirement was modularity and backwards compatibility of the controller that simplifies hardware troubleshooting and facilitates targeted maintenance of individual components.

Figure 2 shows the new LLRF controller chassis and the hardware components. The new LLRF controller's hardware comprises of (1) FPGA board, (2) RF front-end board, (3) tuner board that can be either stepper, pneumatic or piezo, (4) switching power supply and (5) solid state drive (SSD). These hardware components reside in a 2U chassis designed to be stand-alone and rack mountable.

The FPGA board is a Xilinx ZCU102 [4] evaluation board that hosts a Zynq Ultrascale plus Multi-Processor System on Chip (MPSoC), gigabit ethernet interface for networking, serial advanced technology attachment interface for SSD, universal serial bus interface for serial console debugging, high pin count FPGA mezzanine card for interfacing with RF front-end board and high-speed serial transceivers for interfacing with ADC and DAC on the RF board via JESD204B protocol.

The RF front-end board hosts high-speed data converters, RF components such as digital attenuators, switches, filters, low noise amplifiers, non-volatile memory for configuration storage, low speed ADC and DAC for interfacing with external systems and phase locked loop (PLL) that generates clocks for data converters and FPGA. The tuner board can be either stepper motor driver, pneumatic driver or piezo actuator driver and depends on the cavity type the LLRF controller is used to operate. The switching power supply is 1U fan cooled and

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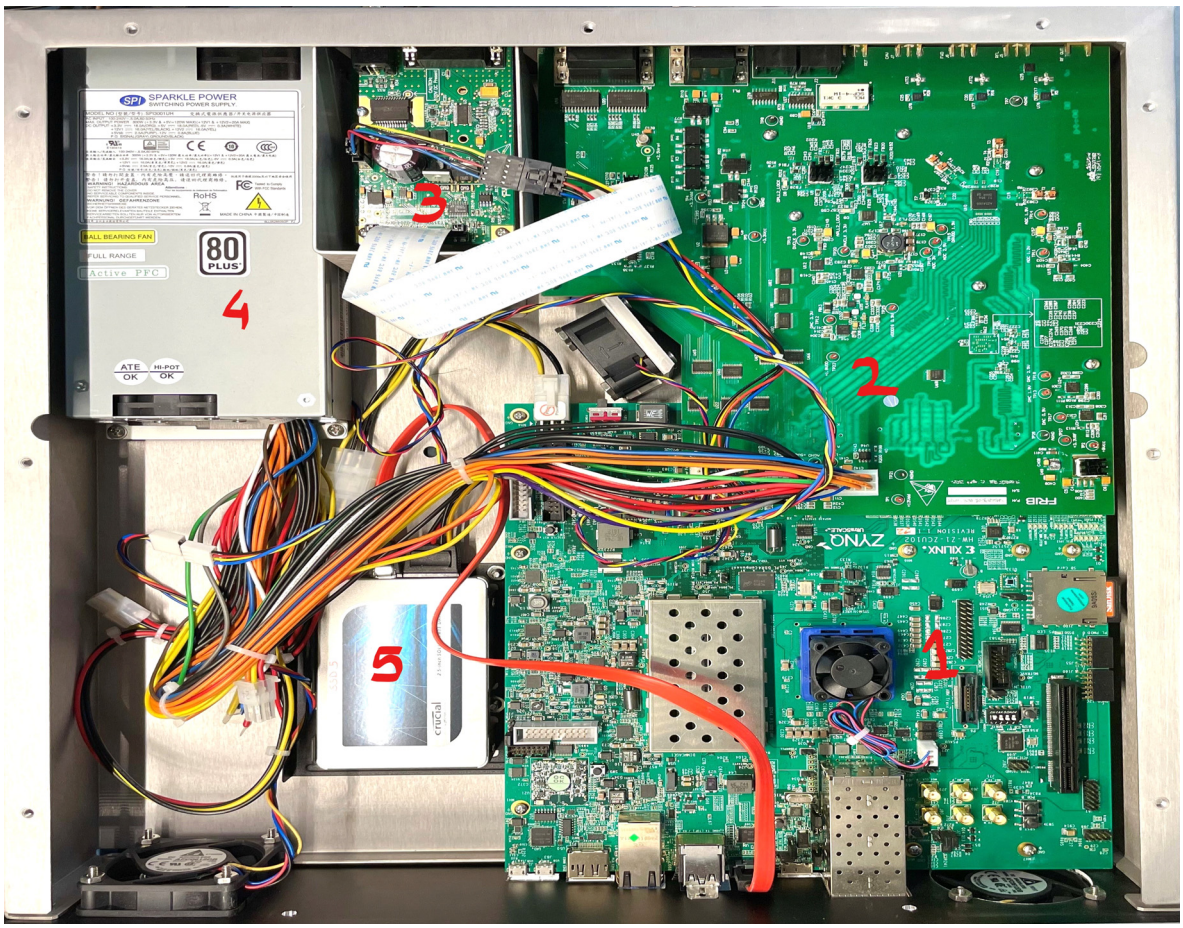

Figure 2: New LLRF controller chassis.

supplies power to all hardware components inside the chassis. The SSD hosts root file-system of the Linux operating system running on one of the processors of the SoC. Table 1 shows differences between current and new LLRF controller's component specifications.

Table 1: Controller Component Comparison

Component	Current	New
ADC	14-bit, 65 MSPS, 500 MHz bandwidth	14-bit, 500 MSPS, 900 MHz bandwidth
DAC	14-bit, 400 MSPS	16-bit, 1.6 GSPS
FPGA	Xilinx Spartan-6	Xilinx Zynq
RF board	FR4, 6 layer	RO4350B, 8 layer

RF DESIGN

The overall RF design architecture enforces the approach of eliminating active RF components in the input and output chain to reduce their temperature dependence. Hence, the RF input or output chain does not include a mixer or a local oscillator.

RF Inputs

The RF board has 4 input channels for reference clock, forward, reverse and cavity signals. The ADC chosen for the design provides 14-bit resolution with maximum sampling frequency of 500 MHz. The design approach of direct under sampling and the ADC's 900 MHz bandwidth enables sharing the same RF input chain for a wide range of frequencies. This method eliminates the need for mixing RF signals to an intermediate frequency lower than the Nyquist frequency of the signals and an appropriate sampling frequency ensures the higher order harmonics do not alias into baseband. The sampled signals are digitally mixed to generate In-Phase (I) and Quadrature (Q) data and a Cascaded Integrator Comb (CIC) filter further filters harmonics from the mixing stage (see Fig. 3 and Fig.4).

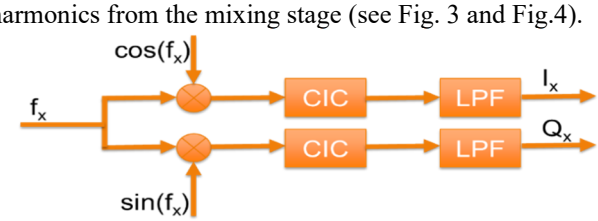

Figure 3: IQ demodulation and filtering of RF input.

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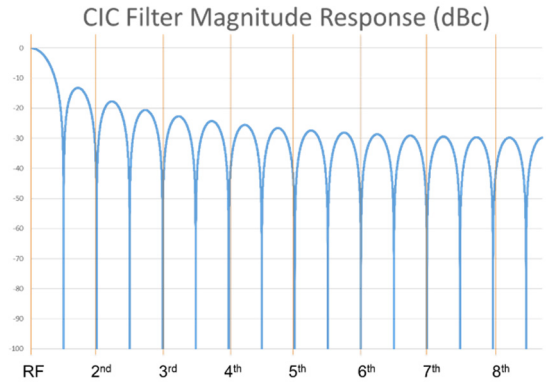

Figure 4: CIC filter magnitude response.

RF Output

The FPGA generates and sends four points (+I, +Q, -I, -Q) to the DAC and the selection of sampling frequency along with the DAC's maximum sampling frequency of 1.6 GSPS allows the desired RF output signal to either be the fundamental frequency or its harmonic that is further filtered by a band pass filter (BPF). The RF output chain is simplified by using the DAC's multiple output ports and RF switches. Based on the cavity type and desired frequency, the DAC is configured to output the signal on a different output port (see Fig. 5) and the RF switch allows sharing of the same low pass filter (LPF) and low noise amplifier (LNA) thus, reducing the number of components.

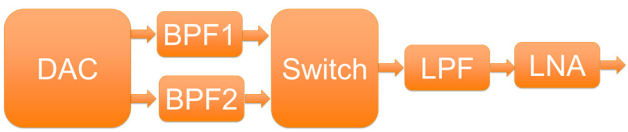

Figure 5: RF output chain.

FPGA

Firmware

The ADC and DAC communicate with the FPGA via JESD204B protocol. The advantage of this protocol is significant reduction in the number of PCB traces, simplified interface timing and its scalability to higher frequencies. It, however, poses challenges in firmware design given its complex implementation and operation. One of the main challenges is meeting timing, achieving synchronization and establishing a link between devices prior to data transfer.

Active disturbance rejection control (ADRC) [5] algorithm is implemented in firmware [6] for RF cavity closed loop control due to its capability of decoupling system variables. Other functions implemented in firmware include tuner control, signal processing, interlock handling, interfacing with external systems and fast data capture.

Software

The software application is based on embedded systems design approach. It executes high-level tasks for initializing device configuration, controlling fan speed for optimal cooling, serial console debugging and calculating parameters based on system and cavity type.

EPICS IOC

By taking advantage of the new LLRF controller's FPGA MPSoC, Experimental Physics and Industrial Control System (EPICS) Input/Output Controller (IOC) server was implemented on its A53 quad core processor. In comparison, the current LLRF controllers communicate with standalone IOC servers over Universal Datagram Protocol (UDP) (see Fig. 6).

Figure 6: EPICS IOC implementation comparison between current LLRF controller and new upgraded LLRF controller.

Running IOC on the LLRF controller simplifies maintenance by reducing the risk of affecting multiple end devices connected to one standalone IOC, allows for distributing hardware computing resources, gives IOC hardware-level access to data and interrupts from the FPGA and helps in reducing network traffic and latency by eliminating unreliable and lossy UDP connection. A challenge of implementing IOC server on LLRF controller is the increase in total number of IOC servers under management that requires more resources for configuration management systems.

PRELIMINARY TEST RESULT

Since the FRIB 644 MHz SC cavity is currently under development, the new LLRF controller was tested for operation of UEM 1.013 GHz RT cavity (see Table 2). Implementing CIC at different levels to reject spurious line noises at frequencies higher than the bandwidth of the RT cavity reduces the phase noise to within 0.01 degree rms. These results validate the new LLRF controller design and its capability of meeting design requirements for the UEM system. In the future, the controller will be tested for operation of FRIB 644 MHz SC cavity.

Table 2: Test Result for UEM RT Cavity Operation

Error	Value	Unit
Amplitude peak	0.66	%
Amplitude rms	0.36	%
Phase peak	0.13	Degrees
Phase rms	0.01	Degrees

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