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MODULAR SOLID-STATE SWITCHING AND ARC SUPPRESSION FOR VACUUM TUBE BIAS CIRCUITS

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Abstract

In this work, we present operational and performance data for a solid-state switching circuit that delivers pulsed power at up to 12 kV and 100 A. This circuit, which is comprised of a series configuration of IGBT-based subcircuits, is suitable for driving the high-power vacuum-tube amplifiers that are typically used in RF accelerator systems. Each subcircuit can switch up to 3 kV, and the subcircuits can be stacked in series to extend the overall voltage capabilities of the switch. The circuit is designed to prevent overvoltaging any single transistor during switching transients or faults, regardless of the number of series subcircuits. Further, the circuit also includes the capability for rapid arc detection and suppression.

Testing has shown effective switching at up to 100 A at 12 kV and for pulse repetition frequencies and durations in the range of 1 – 200 Hz and 10 – 50 µm, respectively. Additionally, the arc suppression circuitry has been shown to reliably limit arcs at 10 – 12 kV with a quench time of ≤1 µs and with a total energy of <0.2 J, minimizing the grid erosion in the vacuum-tube during an arc.

INTRODUCTION

In recent years, there has been continued interest in using series-stacked high-power transistors for high-voltage switching applications [1, 2]. These high-voltage switches have been used in a number of applications including high-voltage inverters and fusion systems [3]. This work presents a high-voltage switching circuit that can be used to bias high-power vacuum tube amplifiers such as those used in accelerator systems.

Conventional vacuum tube drive circuitry generally uses a constant high-voltage plate bias, with arc suppression handled by a dedicated crowbar circuit that short-circuits the main capacitor bank in the event of an arc. The method presented instead uses a solid-state switching circuit to both pulse the plate bias and suppress arcs.

This circuit has several advantages compared to conventional drive circuitry. Pulsing the plate voltage allows operation at higher bias voltages, increasing peak RF power output capabilities. For example, the YU-141 maximum DC plate voltage increases to 12 kV when pulsed, compared to 10 kV at a constant plate voltage [4].

Additionally, replacing the crowbar circuit with a solid-state switch allows for faster and more robust arc suppression. Conventional crowbar circuits operate by quickly providing a low-impedance path to drain the capacitor bank in the event of an arc; this drops the HV rail, however, it requires a crowbar circuit that can repeatedly dissipate very high instantaneous power without damage [5]. In contrast, the solid-state switch can simply be gated off to stop the arc. Since power transistors with very fast switching speeds can be used, the arc suppression response is very fast, decreasing the damage caused by an arc in a vacuum tube.

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DESIGN

V_{CE} Balancing Circuit

High-voltage power transistors are widely available with collector-emitter breakdown voltages in the range of 1 – 4.5 kV, however, high-power RF vacuum tube amplifiers frequently require much higher (≥8 kV) biases. Stacking power transistors in series is inherently risky since individual device differences can cause the voltage across each device to be unbalanced, increasing the likelihood of an overvoltage failure on one of the transistors during switching.

To protect against this type of overvoltage failure, a series V_{CE} balancing circuit has been developed. Figure 1 shows a conceptual schematic of how the balancing circuit fits into the overall switching modules. The circuit uses series Zener diodes to set the overvoltage threshold for each transistor; when the voltage exceeds the threshold, the balancing circuit drives the transistor gate to drop V_{CE} to a safe level. The current buffering circuit is designed to source enough current to quickly charge the IGBT gate when the gate driver circuit would otherwise gate off the IGBT.

Arc Suppression

A critical aspect of the design is ensuring that the V_{CE} balancing circuit behavior does not interfere with the fast switching times necessary for effective arc suppression. LTSpice simulations were used to sweep the gate resistance and current buffering circuit feedback. The final design allows for relatively stable V_{CE} balancing behavior while also preserving a sub-microsecond response time when gating off the transistor due to an arc.

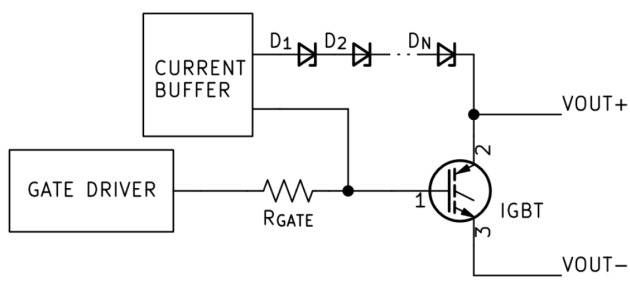

Figure 1: Conceptual schematic of Zener clamping circuit.

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TESTING

Low-Voltage Verification Testing

Initial testing of the circuit was done with two transistor stages (SiC MOSFET), both of which included a V_{CE} balancing circuit with nominal overvoltage limit of 540 V. The circuit switched an inductive load (30 µH, 12 Ω) to induce a high-voltage flyback pulse at turn-off. Figure 2 shows the behavior of this circuit. At $t = 0$, the switch turns on. After the 10 µs pulse the switch turns off, inducing a large flyback voltage due to the inductive load. The V_{CE} balancing circuit limits the voltage to approximately 540 V (plus a varying V_{GE} of approx. 0 – 20 V) until the inductive ringing naturally decays to below this threshold. Although there is some oscillation while the V_{CE} balancing circuit is active, the voltage remains within <50 V of the nominal threshold as shown in the inset.

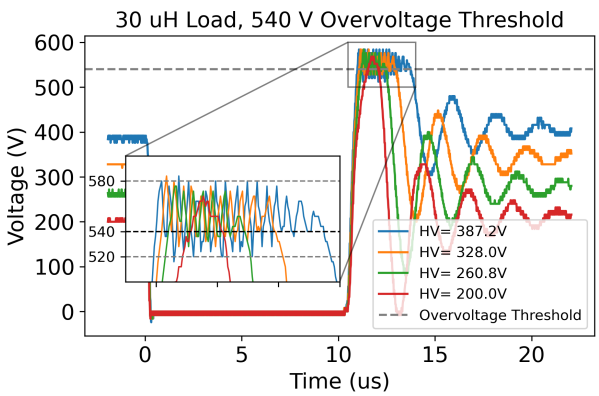

Figure 2: Zener clamp with 540 V Overvoltage Threshold.

High-Voltage, High-Current Testing

To assess the performance of the circuit at realistic vacuum tube bias voltages and duty cycles, a high-voltage, high-current test station was constructed. Figure 3 shows the conceptual schematic of the setup and Fig. 4 shows the physical design. In this setup, each individual stage was based on an IGBT with a continuous maximum V_{CE} of 4 kV and a V_{CE} balancing circuit with a nominal overvoltage limit of 3.24 kV. The total 4-stage circuit (component A in Fig. 4) was then capable of switching more than 12 kV.

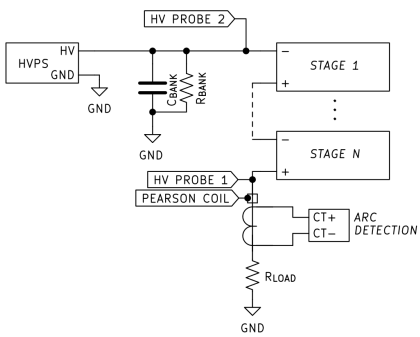

Figure 3: *N*-Stage Switching Test Circuit.

The rest of the test setup consisted of a 100 Ω resistive load (component B), a 0.75 µF capacitor bank (component D), and a TDK-Lambda ALE-202 high-voltage power supply (component C). Two 1000:1 voltage divider probes were used to measure voltages, and a Pearson coil was used to measure load current.

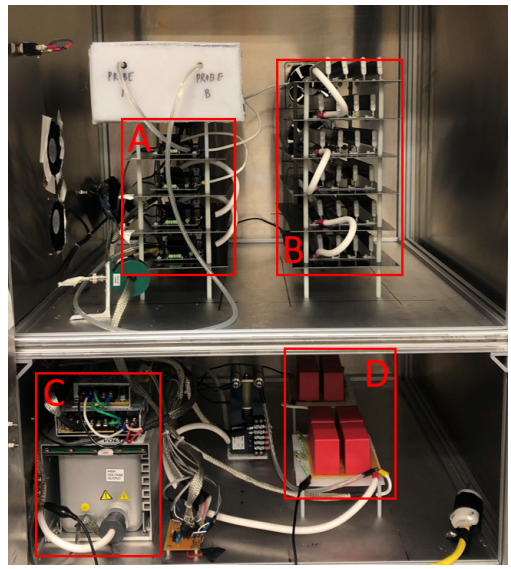

Figure 4: 4-stage high voltage, high-current test setup.

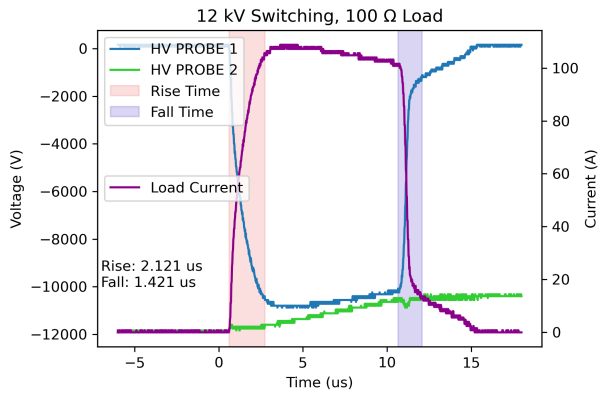

Figure 5: High-Current Switching Waveforms.

This setup was used to assess the switching time and thermal performance with a high-current load. Figure 5 shows a typical switching waveform from this test setup with the rise/fall time highlighted.

To evaluate thermal characteristics of the circuit, a FLIR thermal camera was used to manually observe the temperature of the IGBT heatsink during various switching conditions. At 12 kV, 100 A switching, and a duty cycle of 0.06% (10 µs pulse, 60 Hz), the range of temperatures on the four IGBT stages was approximately 52 – 70 ° °C.

Arc Suppression Testing

To determine the arc suppression performance, a spark gap was used to generate arcs in parallel with the load (R_{LOAD} =2 MΩ). Figure 6 shows a conceptual schematic of this setup, and the inset shows an image of the spark gap assembly. Arcs were detected by using a current transformer

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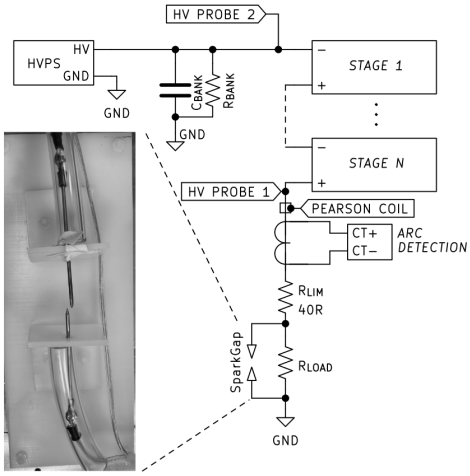

Figure 6: *N*-Stage test circuit with spark gap.

to monitor the load current; when the load current exceeds a set threshold, the transistor is gated off. Arcs were induced by first raising the high-voltage node to the desired arc voltage, and then enabling the gate. Arcs from approximately 8 – 12 kV were evaluated in this manner.

Figure 7 shows the circuit behavior during a typical arc. At approximately t =1.1 µs, the rapid drop in load voltage and rise in arc current show the beginning of the arc (also shown by the shaded region). The arc current then rapidly drops and remains approximately zero for the rest of the 10 µs pulse, indicating that the arc suppression system has gated off the transistor.

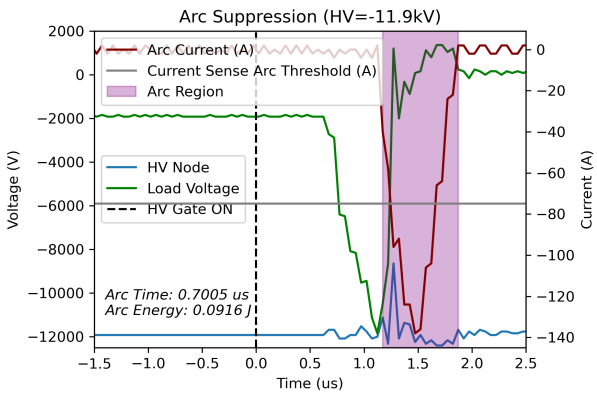

Figure 7: Arc suppression at 12 kV.

Table 1 shows the calculated time and energy from the full set of arcs at 8 – 12 kV voltage set points. As shown by the shaded region in the plot, the arc time is calculated starting when the arc current exceeds 5 A and ending when it drops to below 5 A; the total arc time then includes both the response time of the arc suppression circuit and the shut-off time of the transistor. Since the arc simply discharges the capacitor bank through a small current-limiting resistor, arcs at a higher initial voltage have larger instantaneous current at a given time and therefore lower total arc times and energies.

Table 1: Arc Times and Energies

Voltage (kV)	Mean Time (µs)	Mean Energy (J)
8.20	0.95	0.10
8.96	0.85	0.11
10.0	0.80	0.097
10.8	0.73	0.067
11.9	0.65	0.083

CONCLUSION

The series V_{CE} balancing circuit has been shown to safely switch voltages up to 12 kV, and currents exceeding 100 A, without overheating or overvoltaging the series-stacked transistors. Fast and reliable arc suppression limits 8 – 12 kV arcs to <1 µs in duration and <0.2 J in total energy, protecting vacuum tube loads from arc damage.

Since the V_{CE} balancing circuit protects against overvoltage damage, future applications could include pulsed power devices that require protection from inductive or unspecified loads. The modular stages could also be stacked to reach voltages far exceeding 12 kV.

REFERENCES

[1] J. W. Baek, D.-W. Yoo, and H.-G. Kim, "High-voltage switch using series-connected IGBTs with simple auxiliary circuit", *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 1832-1839, Nov.-Dec. 2001. doi:10.1109/28.968198

[2] S. Ma, W. Shang, D. Wang, M. Zhang, B. Zhu, K. Yu, and Y. Pan, "A reliable voltage clamping submodule based on SiC MOSFET for solid state switch", *Rev. Sci. Instrum.*, vol. 92, p. 024713, 2021. doi:10.1063/5.0027135

[3] B. Beaumont, E. Bertrand, R. Brugnetti, D. Chatroux, F. Kazarian, R. Milly, M. Prou, and H. Rigole, "100 kV solid-state switch for fusion heating systems, Fusion Engineering and Design", vols. 75–79, pp. 1281-1285, 2005, ISSN 0920-3796. doi:10.1016/j.fusengdes.2005.06.202

[4] CPI Eimac Division, "YU-141 Planar Triode", 19 Nov 1992.

[5] C.-P. Käsemann, L. van Lieshout, M. Huart, and C. Sihler, "Thyristor crowbar system for the high current power supplies of ASDEX upgrade", *Fusion Eng. Des.*, vol. 75–79, pp. 149-153, 2005. doi:10.1016/j.fusengdes.2005.06.128