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Current Status and Prospects of FRIB Machine Protection System

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Introduction

Fast response of the machine protection system is critical for FRIB beam commissioning and operation to prevent damage to equipment. The beam commissioning of the first LINAC segment (LS1), including fifteen cryomodules, has been completed. During the beam commissioning, from the ACCT net-work detecting a fault of over-power or power-loss-over-threshold conditions, or from fast events detected by the LLRF controllers, to the moment when beam is inhibited, the response time of MPS is within 35 µs [1]. This paper focuses on MPS system structure and its FPGA logics currently implemented in the production line for LS1 commissioning and discussion of its fu-ture improvements.

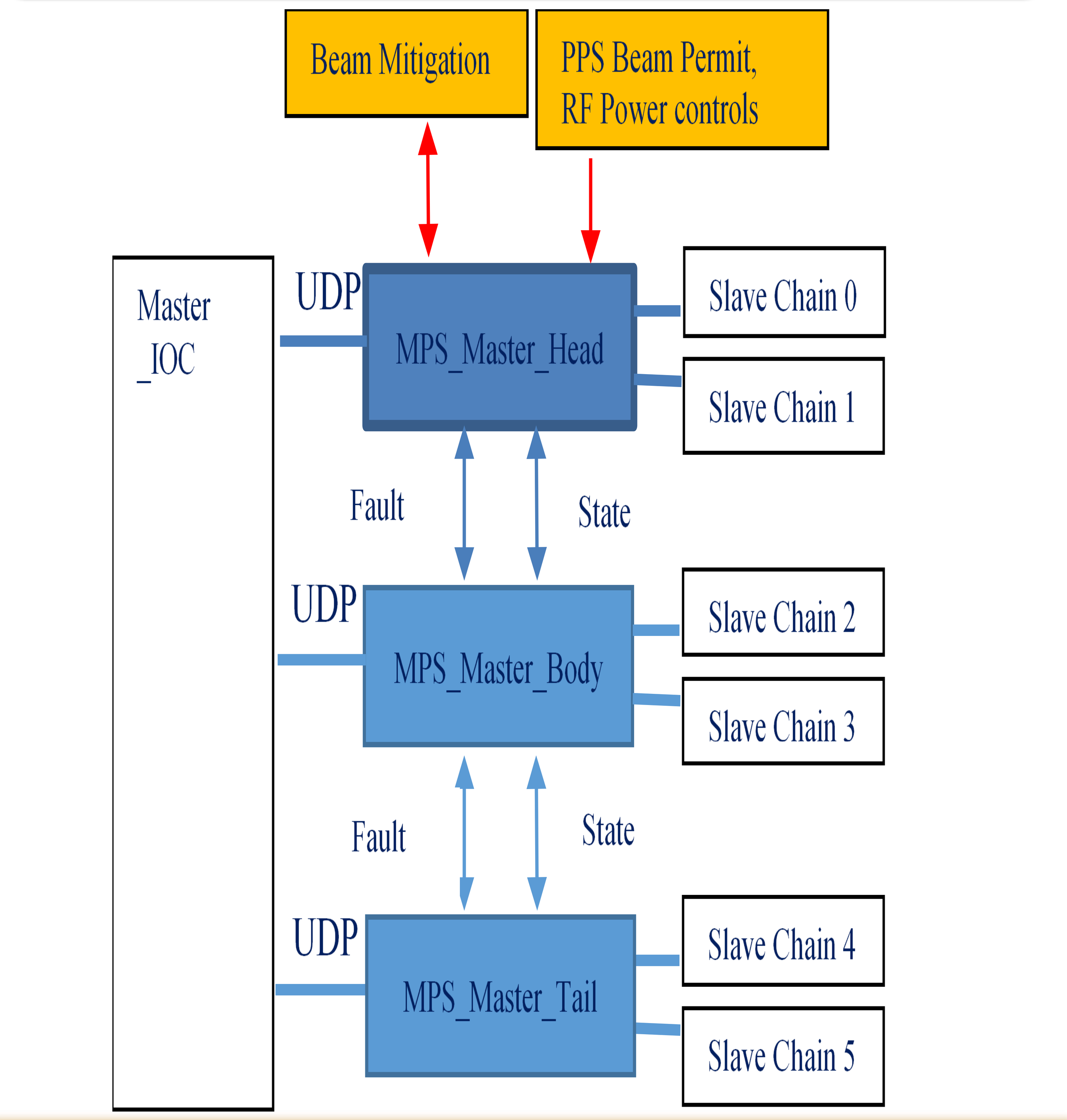

Figure 1: MPS of reptile structure deployed in production.

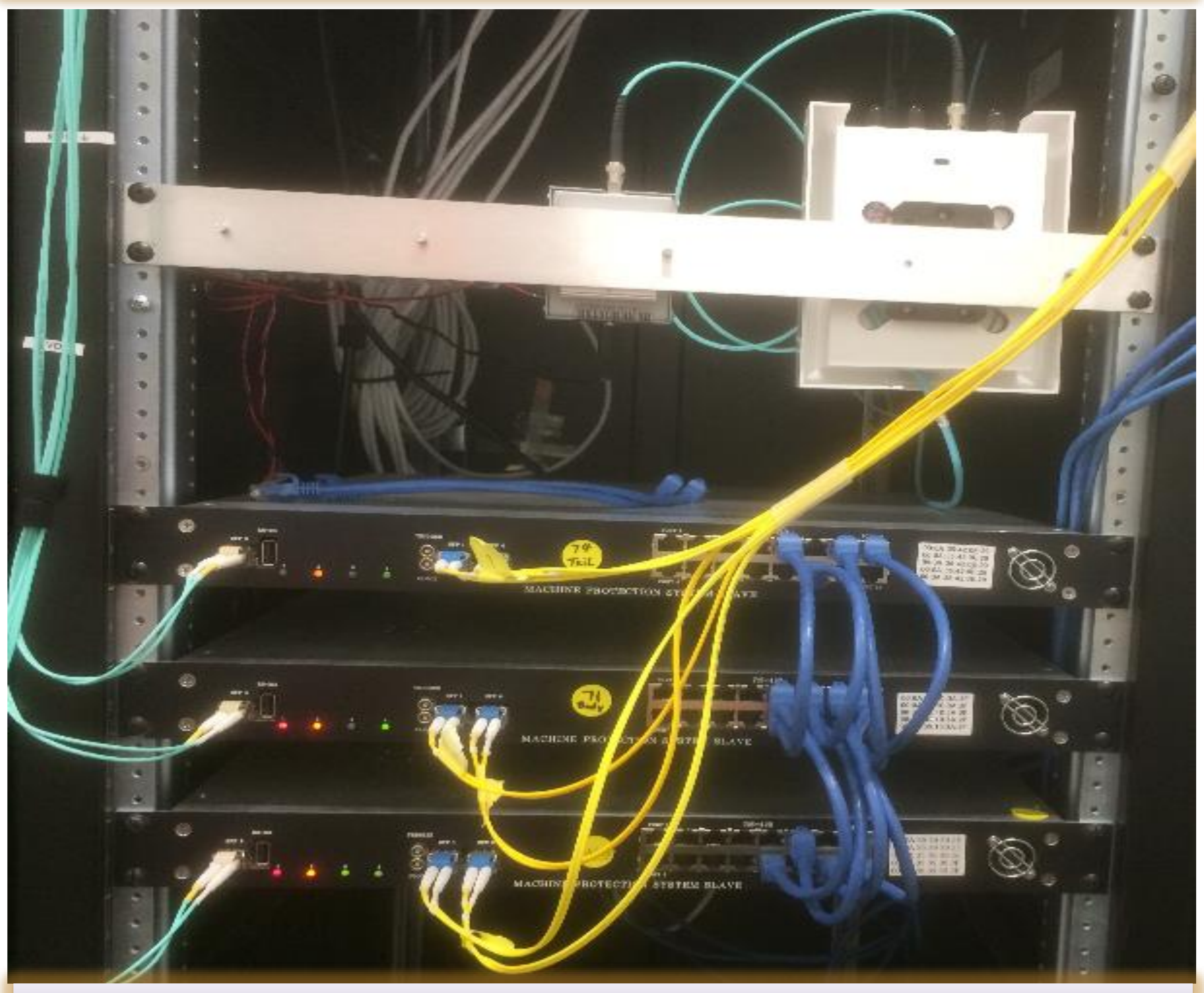

Figure 2: MPS master head, body and tail in the production line.

MPS Current Implementation

A "reptile" structure of MPS was deployed in the production line where we have multiple master nodes consisting of "head", "body" and "tail". Each master node can hold 2 daisy chains with maximum of 16 slave nodes. It requires 33 slave nodes and 6 master-slave daisy chains to fully cover FRIB front end and LS1 area for machine protection. One advantage of such a "reptile" structure MPS is that it can grow as many daisy chains as user needs by adding additional body sections. Another advantage is that each section (master or slave node) of this "creature" is controlled by a FPGA and it can decide a fail-safe mode in case communication to master head is lost.

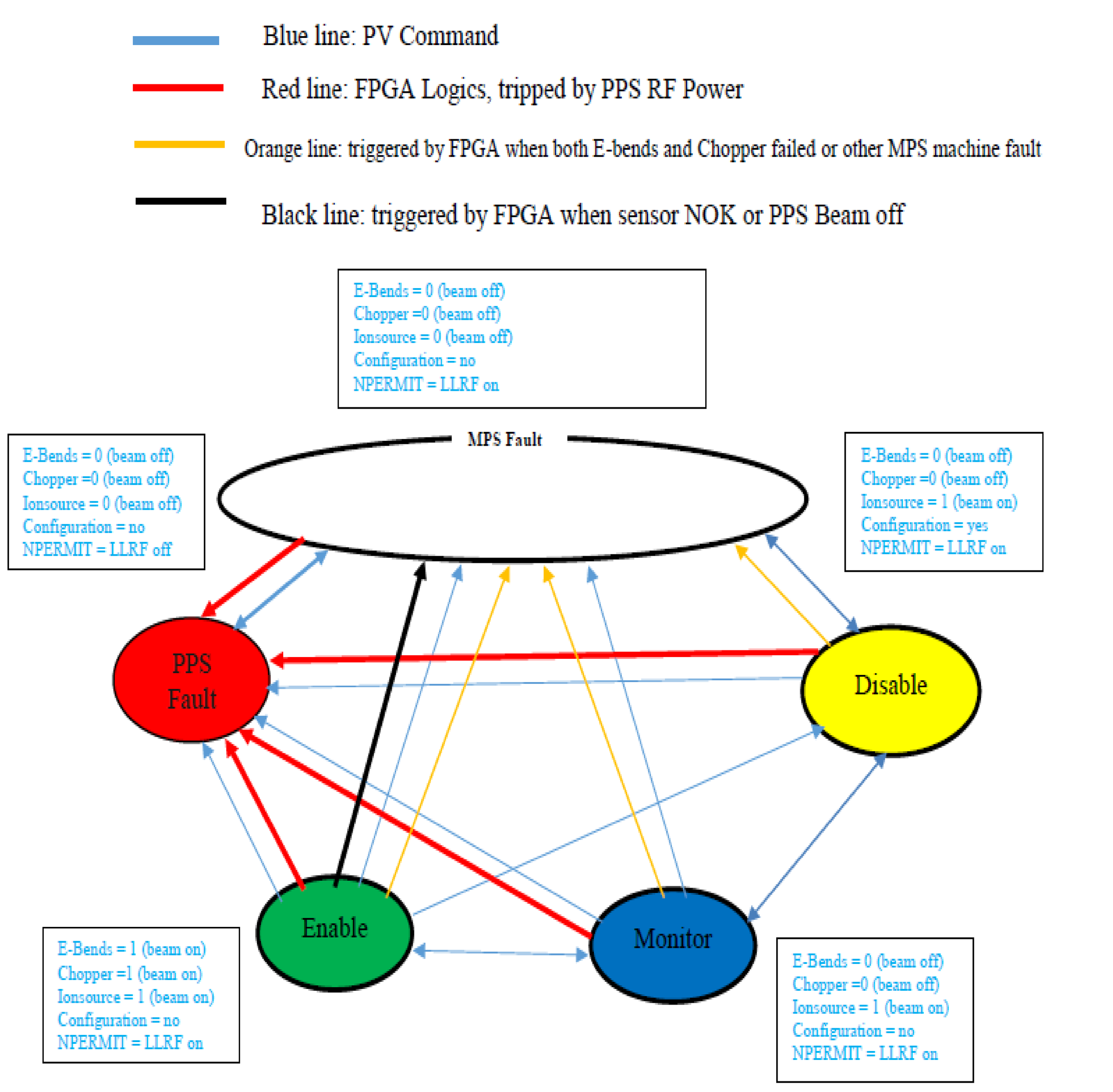

Figure 3: MPS master operation state diagram. Highlighted in blue line, Master head can listen to the PV commands to change the operation states, the rest master nodes can only accept the commands from the head through the state link. Highlighted in red line, each master node will enter PPS fault state at PPS event. Highlighted in yellow and black line, each master node can decide to enter fault state based on the inputs from MPS sensor devices, machine status of MPS. Each master node can broadcast its fault state to the entire MPS network though fault links and daisy chains.

MPS Control Logics

All MPS master nodes run with state machine which provides a reliable and steady controls to mitigation devices as well as to LLRFs. The final decision of beam mitigation is made by MPS master head who listens to each enabled MPS sensor from the entire MPS network and trips off the beam in case of sensor NOK (not OK) and informs LLRF through slaves to turn off RF cavities in case of PPS NOK. MPS master state machine has 5 operation states: MPS fault, disable, monitor, enable and PPS fault. PPS fault state are for RF cavity protection. LLRF controller is required to turn off RF drive in case of a PPS event which results in AC power to the RF amplifiers being removed. NPERMIT signal is required to connect to LLRF to control the circular buffer of post mortem data and power off the RF cavity within 10 µs of design expectation which provides enough time to turn off the RF cavity before power supplies decay (~10 ms).

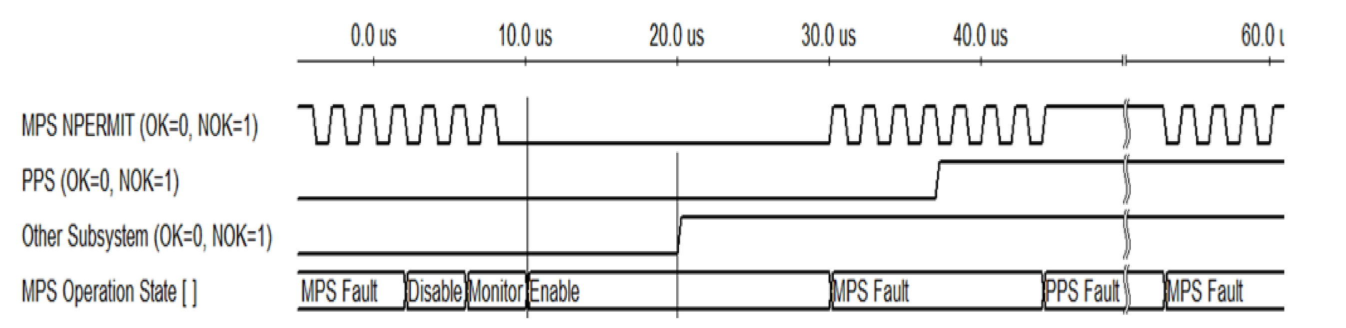

Figure 4: NPERMIT signal vs. MPS operation state. MPS moves into MPS fault state from enable state when subsystem is NOK and then to PPS fault state when PPS is NOK, NPERMIT signal is changed from steady 0 to 1 µs pulse and then steady 1 signal.

Test in the Beam Line

The MPS response time measurement has been done with ACCT and chopper monitor in the LS1 commissioning and the result is within design expectation of 35 µs. Also, 116 LLRFs currently installed in the production line are tested with an automated test program, the worst case scenario is within 10 µs from that LLRF sends out NOK to that MPS master head latches the fault and activates the mitigation devices; the worst case response time for PPS event is within 2 µs from that MPS master sends NPERMIT signal of PPS event to that LLRF receives the signal and reacts. Also, all PLCs which monitor front end area and cryomodules and 13 MicroTCAs (diagnostic devices) connected to MPS are tested to trip MPS successfully with forced NOK signals.

Conclusion

The MPS with 6 daisy chains and 33 slave nodes which connects diagnostic devices, LLRFs and PLCs in the area of the front end and LS1 passed the LS1 commissioning and its machine protection response time is within 35 µs. Currently a reptile structure with multiple master nodes is implemented in the production because of FGPDB hardware limitation. A proposal is made to use latest Xilinx Zynq FPGA to host embedded IOC in its Petalinux kernel plus Debian file system and to combine multiple master nodes into one Zynq FPGA board. A prototype of embedded IOC has been successfully developed on ZC706 board which can control the GPIO ports through EPICS PVs. Therefore the future MPS system with advanced FPGA technologies will be much fast and reliable in terms of EPICS controls, response time, post modem data acquisition, fault pattern tracking and analysis.

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