Beam Intensity Monitoring System For The PIP-II Injector Test Accelerator

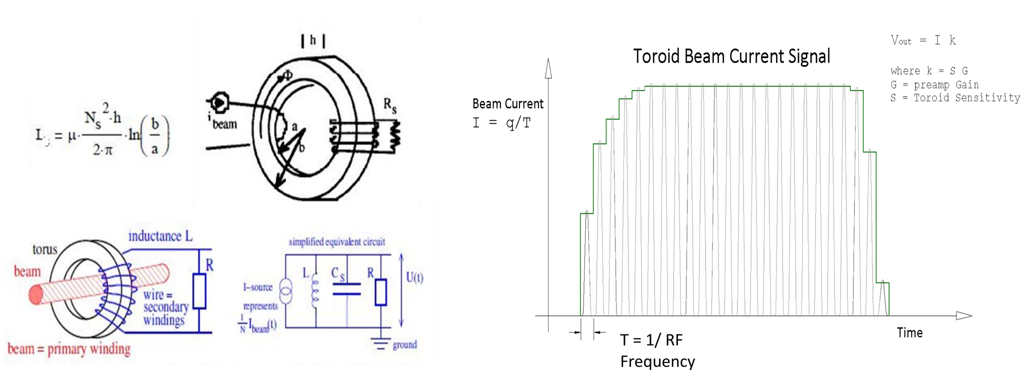
N. Liu, J. Diamond, N. Eddy, A. Ibrahim, N. Patel, A. Semenov

Fermi National Accelerator Laboratory

ABSTRACT The PIP-II injector test accelerator is an integrated systems test for the front-end of a proposed CW-compatible, pulsed H^- superconducting RF linac. This linac is part of Fermilab's Proton Improvement Plan II (PIP-II) upgrade. This injector test accelerator will help minimize the technical risk elements for PIP-II and validate the concept of the front-end. Major goals of the injector accelerator are to test a CW RFQ and H^- source, a bunch-by-bunch MEBT beam chopper and stable beam acceleration through low-energy superconducting cavities. Operation and characterization of this injector places stringent demands on the types and performance of the accelerator beam diagnostics. This paper discusses the beam intensity monitor system.

Toroidal Beam Intensity Monitor

To ensure the beam intensity remains close to pre-determined levels, beam intensity monitors with magnetically-coupled toroidal pickups are used as a non-interceptive method to measure the total transferred intensity in the LEBT and MEBT transport line.

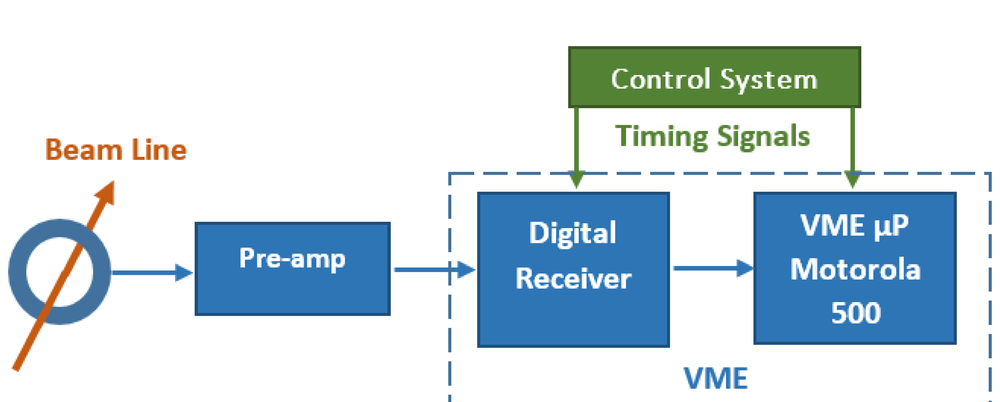


The toroidal pickup follows basic transformer theory. Passing through the center of the toroid, the beam forms a single-turn primary coil of the transformer. The induced voltage is measured across a burden resistor which terminated the secondary coil.

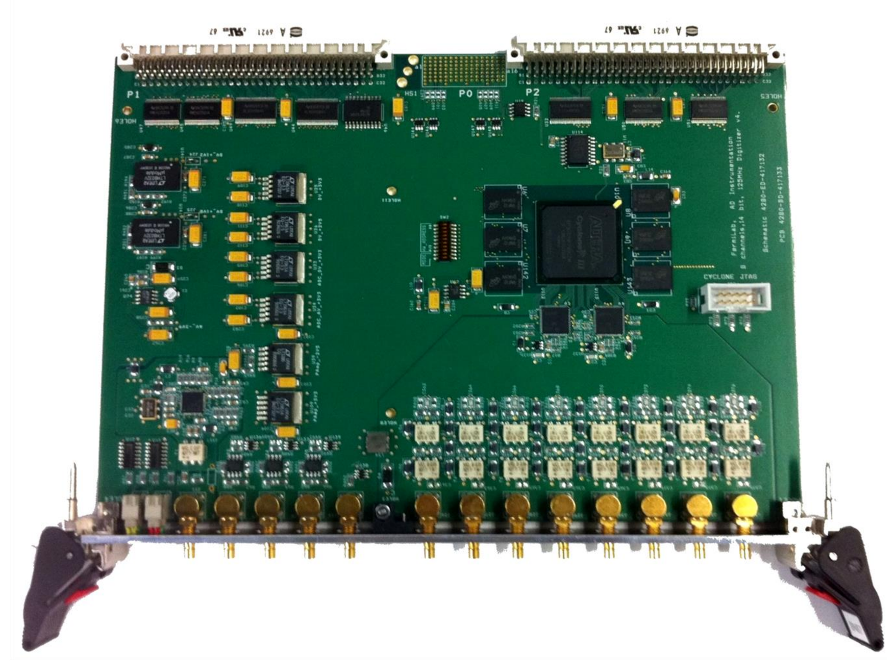
$$Total\ Intensity = \frac{Q_{Total}}{e_{charge}} = \frac{T}{k \cdot e_{charge}} \cdot \sum_{n=0}^{M} v_n$$

$$Average\ Current, I_{AVG} = \frac{Q_{Total}}{PW} = \frac{T}{k} \cdot \frac{1}{PW} \cdot \sum_{n=0}^{M} v_n$$

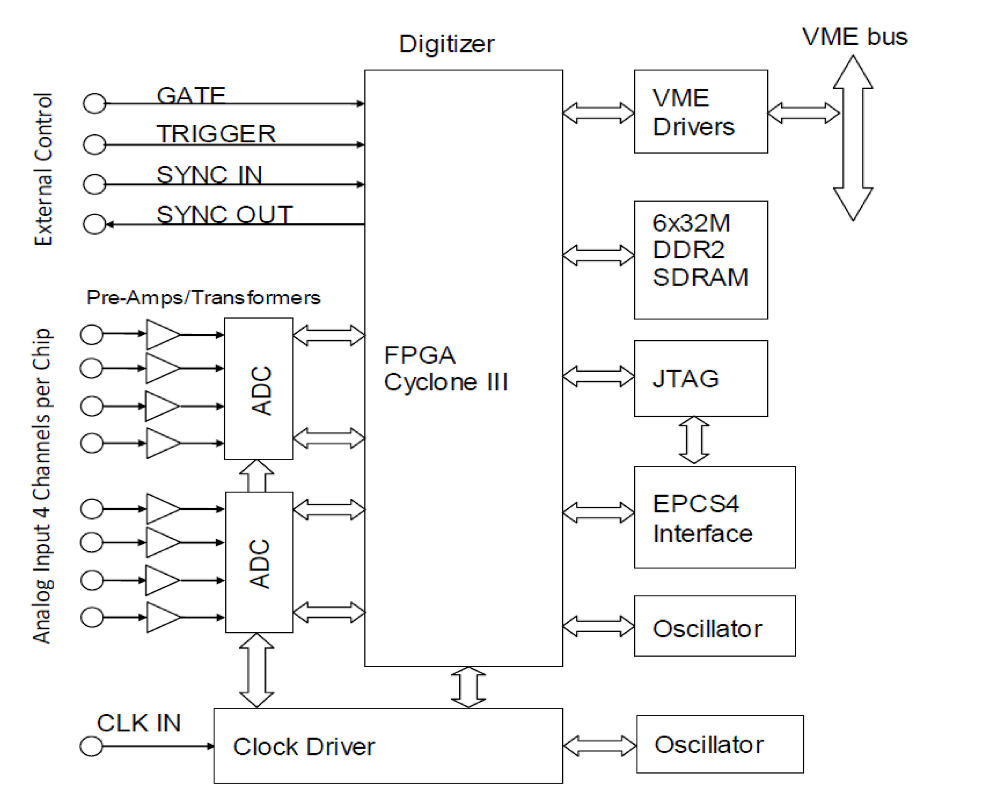
The beam intensity monitor system consists of the toroid assembly, the signal conditioning circuit as well as the dada acquisition electronics



125MHz 14-bit 8 Channel Digitizer

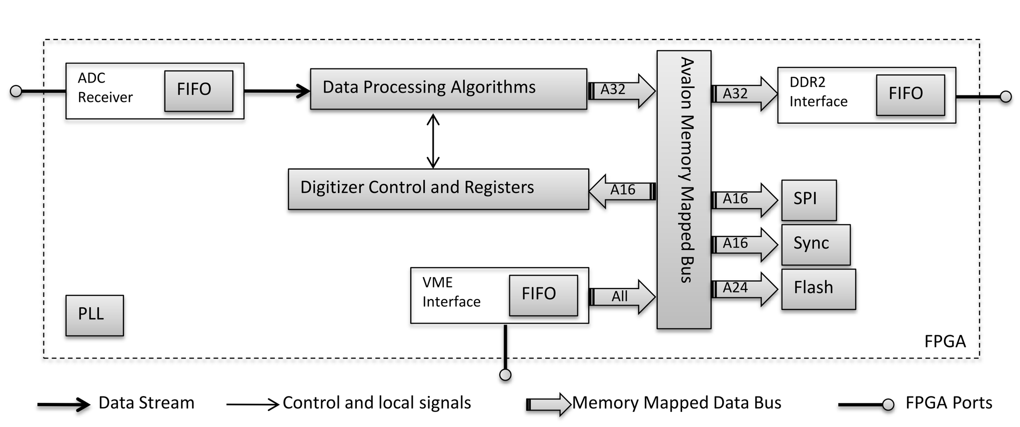


- In-house designed, 6U VME board, sampling rate up to 125MSPS
- 8 analog input channels, selectable AC/DC coupling
- Programmable clock distribution circuit, smart triggering scheme
- Onboard Altera Cyclone III FPGA chip, 192MB DDR2 SDRAM



Simplified digitizer hardware diagram

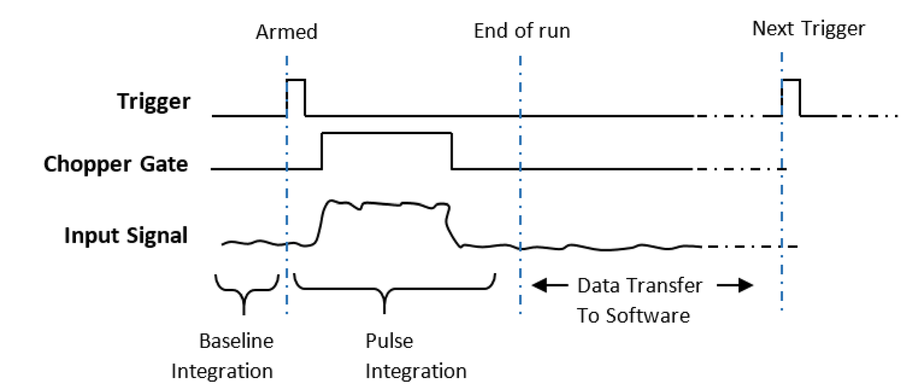
FPGA Design Structure



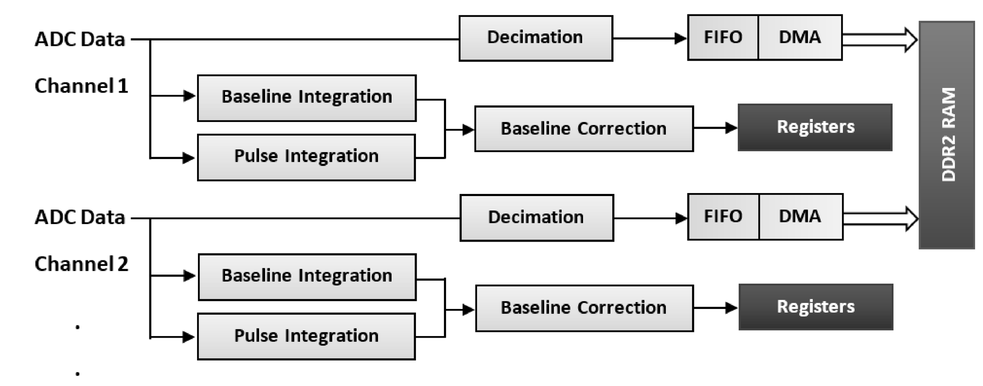
The firmware contains I/O interfaces including the ADC interface, VME bus driver, memory interface, serial interface, etc. as well as application specific algorithms. The connection between the design blocks was developed using the Qsys tool provided by Altera.

FPGA Signal Processing

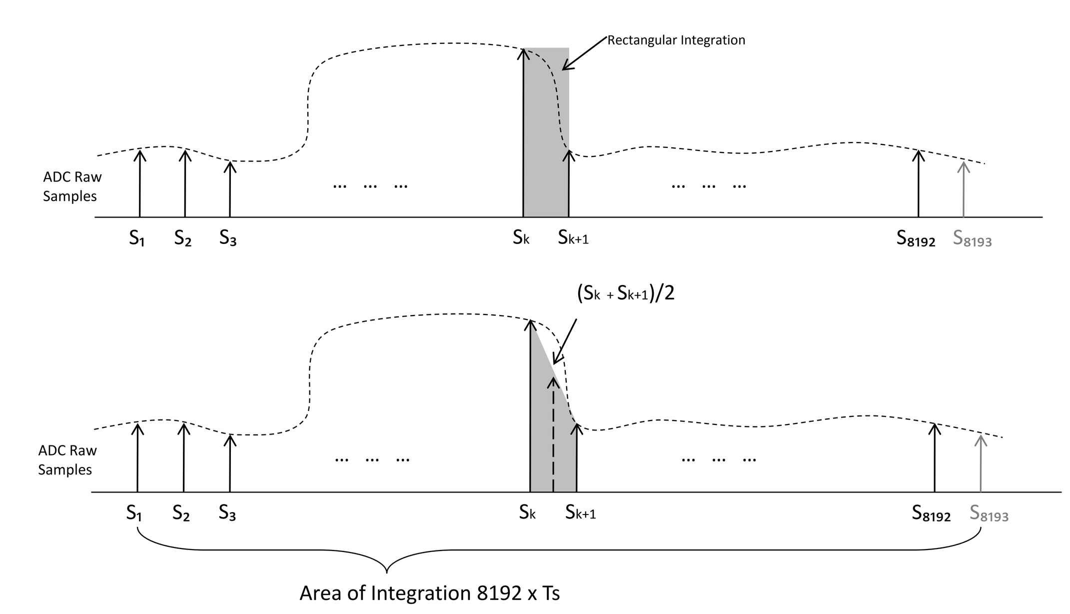
- A 10Hz trigger event starts the operation
- Calculations for all 8 channels performed in parallel
- Baseline data is buffered in real time and integrated
- Pulse is integrated within a dynamic window
- Baseline correction is performed from two integrations
- A TTL Chopper gate is used to determine pulse with
- An optional edge detection can be used instead of gate
- Decimated ADC data are saved in memory for diagnostics



Integration and Baseline Correction



Trapezoidal Integration

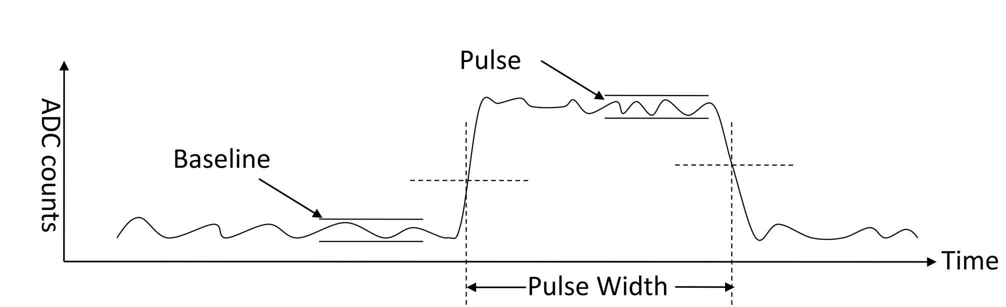


$$Int._{Rectangular} = \sum_{k=1}^{8192} s_k$$

$$Int._{Trapezoidal} = \sum_{k=1}^{8192} \left(\frac{s_k + s_{k+1}}{2}\right) = \frac{s_1}{2} + \sum_{k=2}^{8192} s_k + \frac{s_{8193}}{2} = \sum_{k=1}^{8192} s_k + \frac{s_{8193}}{2} - \frac{s_1}{2}$$

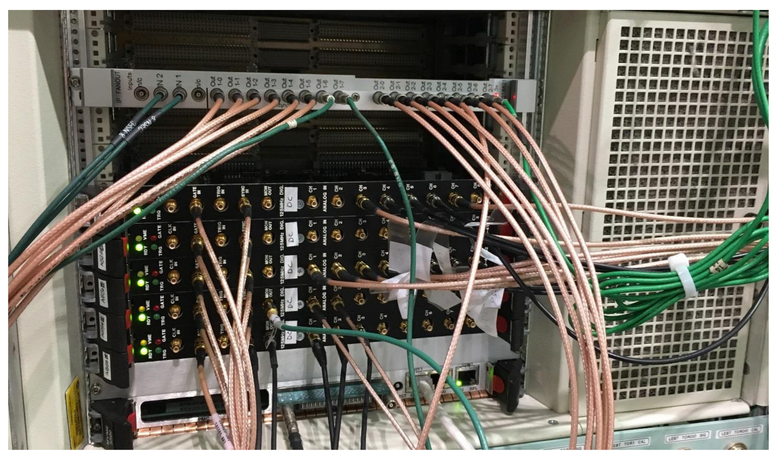
The integrator uses trapezoidal instead of rectangular integration to account for quick changes in pulse current.

Edge Detection



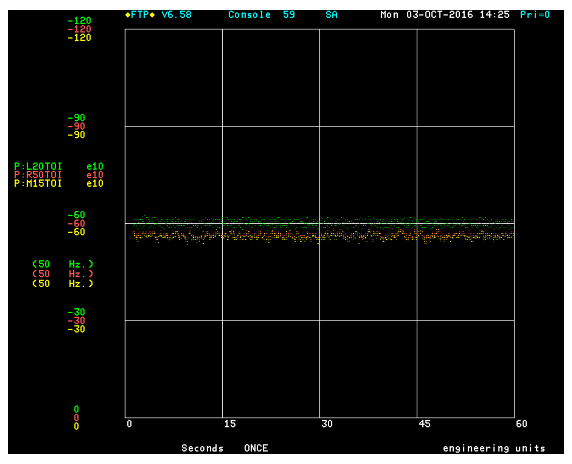
A buffer records the variation of the baseline/pulse. When input samples exceed the recorded range by a predetermined threshold, the edge is detected.

System Installation

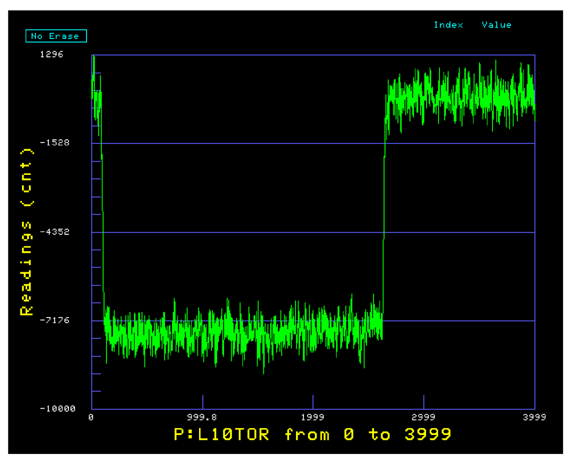


VME based electronics and timing signal fan-out

Measurement Screenshots



Intensity readings for three Toroid devices in LEBT and MEBT



Decimated ADC data array

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