AN INTERNET RACK MONITOR-CONTROLLER FOR APS LINAC RF ELECTRONICS UPGRADE

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Abstract

To support the research and development in APS LINAC area, the existing LINAC rf control performance needs to be much improved, and thus an upgrade of the legacy LINAC rf electronics becomes necessary. The proposed upgrade plan centers on the concept of using a modern, network-attached, rackmount digital electronics platform –Internet Rack Monitor-Controller (or IRM-C) to achieve the goal of modernizing the rf electronics at a lower cost. The system model of the envisioned IRM-C is basically a 3+1 tier stack with a high-performance DSP in the mid-layer to perform the core tasks of real-time rf data processing and controls. The Digital Front-End (DFE) attachment layer under the DSP bridges the application-specific digital front-ends to the DSP. A network communication gateway, together with an event receiver (EVR) in the top layer merges the Internet Rack Monitor-Controller node into the networks of the accelerator control infrastructure. Although the concept of the IRM-C is very much in trend with today's Internet-of-Things (IoT), this implementation has actually been used in the accelerators for over two decades.

CHALLENGES

The APS LINAC rf electronics covers the functions of rf control, monitoring, as well as the equipment protection in general as a typical "Low-level rf" (LLRF) system does. However, upgrading the electronics with an aim at improving the rf performance in precision has a set of challenges mainly due to two factors. The first is the use of SLED (SLAC LINAC Energy Doubler) in the rf power source as an economical method of boosting the rf power. The second has to do with an adopted strategy of operating the klystrons in saturated conditions for the purposes of prolonging the klystron life and minimizing the rf overpower trips. Both the choice of SLED and the operation strategy are appropriate for the given mission of the LINAC merely as a beam injector. However, that also has created some challenges to the future electronics upgrade for the rf improvement. Specifically,

1. The rf output from the SLED pulse compressor has a very narrow, and rapidly decaying pulse waveform which lacks the desirable flat-top that the waveforms from a non-SLED rf source normally have. The accelerating structures typically have a rf filling time of ~800nS. Over that time period, the SLED rf power drops by more than 80% from its peak as shown by the yellow scope trace in Figure 1, and it results in a severely lopsided rf field distribution in the accelerating structures (or A-S) indicated by the A-S output waveform (red trace). It is very difficult to accurately measure the rf level and phase with such dynamic waveforms, and would require in the new electronics to use the digitizers of ultra-high speed and high-resolution, and clocked with a very low-jitter timing. The very-high peak power of the severely lopsided SLED rf waveforms puts a lot of stress on the high-power rf components, and has created the need in enhancing the rf protections.

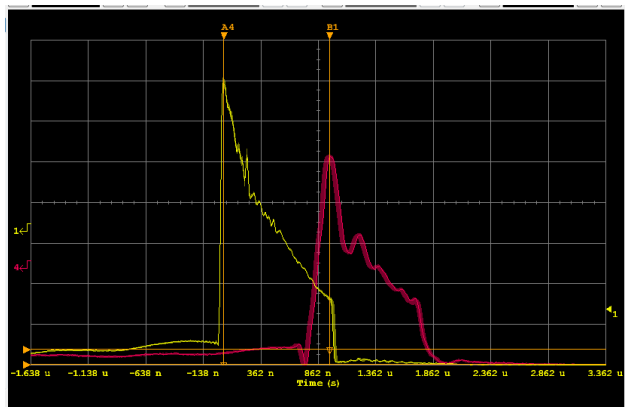

Figure 1: Rapidly decaying rf waveforms of APS LINAC rf driven by a SLED-based rf source, A-S Input rf power (yellow trace) and A-S Output Power (red trace).

2. Operating the klystrons in saturation has a significant impact on the rf control. Under such conditions, the klystrons work like Class-C amplifiers, and that has two implications. 1) the normal capability of effectively controlling the klystron output power through changing the rf input level is lost, and so goes the capability of fast rf power control. 2) The klystron output rf phase would change dramatically as the rf operating power level is changed. The result is that the rf power and phase cannot be independently adjusted, which makes the beam operation difficult. Correcting this undesirable rf power-phase coupling requires some very fast and sophisticated DSP technology.
3. With the existing rf system, the SLED timing jitter gets translated into the beam energy jitter. Because of the rf power-phase coupling issue, APS has adopted an alternative way of the controlling the rf "power" without affecting the phase. That is done by timing the A-S rf filling such that when the beam passes through, the A-S is only partially rf-filled as shown in the scope picture in Figure 2. By adjusting the SLED timing to change the degree of the partial rf-fill, the total amount of rf power that the beam experiences

when it flies through the A-S is therefore changed. This scheme basically works fine in terms of rf "power" control. But it has also made the rf "power" to the beam sensitive to the jitter in the SLED timing. The SLED timing routinely has a jitter of about 20 nS. It is estimated from a study that this 20nS jitter in the SLED timing translates to about 1% jitter in the beam energy by one klystron station. The implication is that as a part of the rf improvement, the timing jitter needs to be much reduced in the upgrade.

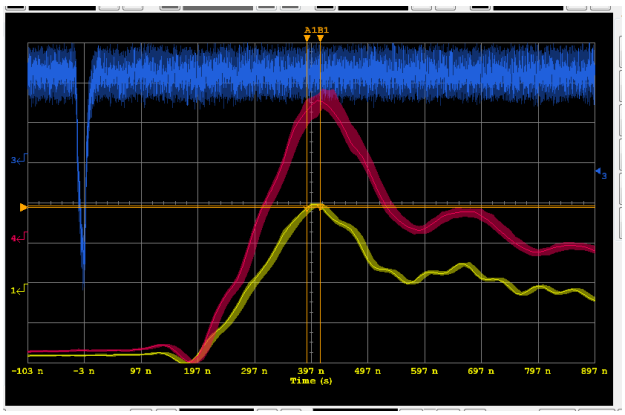

Figure 2: APS LINAC uses a partial rf-fill method as a mean to control the amount of rf power that the beam sees when it passes through an A-S. In this scope screenshot, the beam (blue trace) arrives 200nS prior to the time when the rf power (red and yellow trace) has propagated to the exit port of the accelerating structure.

4. The legacy hardware platforms in the existing system also need to be updated. However, finding a new hardware platform suitable for the purpose is a problem. The common off-shelf commercial crates, from the old VME to the new uTCA, have always been ill-fitting for the rf control application due to some well-known shortcomings like lack of real-time data bus. To work around these problems, it was typically resorted to a messy hybrid solution of adding the external enclosures of different kinds, and connecting the sidecar enclosures to the crate with the fieldbus. The even bigger problem with using these commercial crates are the significantly increased risks in the development costs and schedule. The primary drivers for the risk escalation are the much reduced hardware choice, and the introduction of a significant amount of additional development for the crate system that is not directly related to the rf control. This problem was well understood more than twenty years ago. The experts in the national accelerator laboratories have been working on the alternative solutions for the accelerator control backbone hardware since [1][2][3][4]. Their pioneering work inspired the proposal of the Internet Rack Monitor-Controller to be described as the following.

INTERNET RACK MONITOR-CONTROLLER HARDWARE

The IRM-C module needs to have the necessary hardware resource, interface and I/O ports for the implementations of the necessary functionalities for the rf control, and to be integrated as a node in the accelerator control networks. The key attributes of the required I/O's are listed in Table 1.

Table 1: Hardware Requirements: Primary I/O's

Port/Device	Attribute	Spec.
rf Input ADC Channels	Carrier freq.	2.865GHz
	Ch. number	>48
	Response BW	>100MHz
	Sampling rate	>250MHz
	Ch. Isolation	>80dBc
	Overall distort.	<-70dBc, IMD3
	Resolution	>14-bit
rf Output DAC Channels	Carrier freq.	2.865GHz
	Ch. number	>8
	Response BW	>100MHz
	Update rate	>500Msps
	Ch. isolation	>70dBc
GPIO, digital	Ch. Num.	TBD
GPIO, analog	Ch. Num.	TBD
Gigabit Ethernet	Protocol support	ARP, IPv4, TCP, ICMP, UDP, etc.
Event Network	APS Protocol	8-bit, 100Mbps
	Future Support	16-bit, 1.25Gbps
DFE Links	Std./Ch. Num.	JESD204B / >10
PCI Express	Standard	Gen2,3, 4 or 8-lane

SYSTEM ABSTRACTION

The IRM-C is designed to be a self-contained, stand-alone node to be seamlessly integrated into the accelerator control networks. Functionally, the IRMC model is a simple 3+1 layer stack as illustrated in Figure 3.

Network Gateway layer on the top presents a particular IRMC entity as a node in the network and exchanges the data with other nodes in the system, including the remote EPICS IO Controllers (IO/C) and servers. The network gateway layer is primarily comprised of a Gigabit Ethernet controller and an accelerator timing event receiver.

DSP-Control layer is the core of the IRMC. It is comprised a collection of custom IP's specific to the designed function of the processing, control of the rf data from the various Digital Front-ends (DFE's)

DFE Attachment layer facilitates the data communication between the DSP-Control layer and the application-specific DFE's through real-time data links and buffers.

DFE & I/O layer at bottom provides the bridges the digital world of IRM-C and the analogue word of the application-specific (rf) front-end devices.

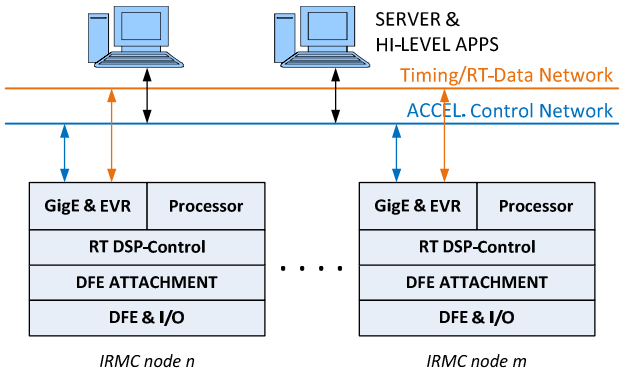

Figure 3: IRMC nodes in the accelerator control networks.

LINAC SPECIFIC ELABORATION

As in a typical accelerator rf control system, the APS LINAC rf electronics system covers the controls of six klystrons stations distributed over the LINAC gallery, and has over 48 channels of rf signals from these stations to monitor. Therefore, deviating from the original IRM idea of including everything in one enclosure [1], the IRM-C design is physically partitioned into three parts to optimize the performance. It has one central DSP module hosting an external CPU and a group of distributed DFE modules at each klystron station as illustrated in Figure 4.

Central DSP module

Instead of having six individual rack monitor nodes in the network for the six klystron stations, the LINAC IRM-C plan consolidates the digital signal processing and control function of all six nodes into a single central DSP module, and is connected to the network as one node. The primary consideration for such an arrangement is to achieve the most important performance required for the rf control of a large scale accelerator, that is, the synchronized, real-time signal data processing and control in one location for the multiple rf stations. This is also an efficient of way of utilizing the hardware resources of today's ultra-density FPGA devices like Xilinx Virtext-7 series. The central DSP module also provides the connectivity to the accelerator control networks. As an integral part of the synchronized data processing and control, the EVR will be implemented as a custom IP embedded in the FPGA, supporting both the current APS 8-bit, 100Mbps, and the possible future upgrade of 16-bit, 1.25Gbps protocol.

CPU module

An external CPU module is planned in the design for gaining the capability of "soft real-time" processing of large amount of data. A commodity rackmount PC would be considered as a cost-effective solution for the hardware. An 8-lane PCIe-over-cable bus makes the high data-throughput connection between the CPU module and the central DSP module.

Distributed DFE modules

The DFE modules digitize the S-band rf signals from all six klystron stations, and buffer the data. Due to the large number of rf signals from six rf stations to be processed in the central DSP module, the DFE section is partitioned out of the central DSP module, and are packaged in six separate, rf-shielded enclosures installed near the rf sources at each klystron stations. The rf signal data of each station is then transmitted to the central DSP module through the real-time data link over optical fiber cables. This approach will not only reduce the amount of expensive and cumbersome rf cabling, but also eliminate the associated phase noise and drifts.

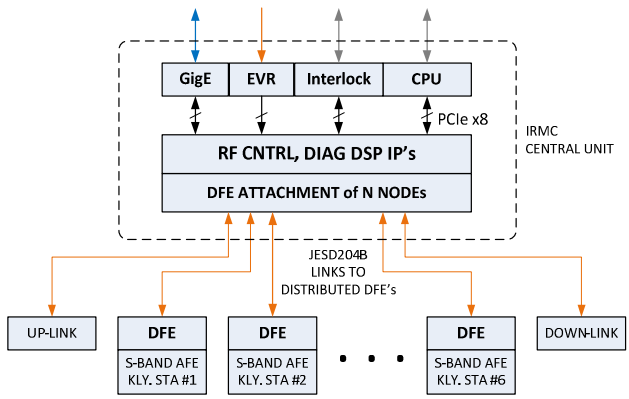

Figure 4: LINAC-specific IRM-C system configuration.

CONCLUSION

The proposed hardware plan of the Internet Rack Monitor-Controller for the APS LINAC rf electronics upgrade centers on the idea of achieving the best rf control performance at a lower cost, using the proven internet rack monitor approach. It presents an alternative hardware solution to the long-standing problem of the real-time data exchange and processing for a large number of rf stations which is an essential requirement for the large-scale accelerator rf controls. Further study and development for the detailed implementations are definitely needed, and will be pursued in the near future.

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