



REAL-TIME MOTOR CONTROL SYSTEM FOR BEAMLINES

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INTRODUCTION

Closed-loop control is a vital part of a control system. The parameters of closed-loop control and the advantage and disadvantage of an analog inputuoung system will als influence on the control system results. This text is designed to discuss about the applications for Closed-loop control and analog input oungut system, in order to enhance the stability and accuracy of beamline motor control system. Consequently, we adopt analog input/output system. FPGA and closed-loop control for design.

Because the stepper motor equipped with a reducer con analyze mobile platform to 10 nanometers per stepper, with FPGA accompanied to simultaneously trigger the activation of an analog input/output system, the addition of a closel-loop control mode firmware into this hardware structure can enhance the stability of the beamline motor system, and the convenience of real-time adjustment against stability. Thus, the beamline control system will be about stability, accurate and convenience.

SYSTEM ARCHITECTURE

The control system structure in this test is designed by way of R-T closed-loop control, with the analog inputioning to module acting as the reading and processing center, and FPGA module and firmware controllers acting as its hardrawen. The computer end serves to give location orders and besides, the stepper motor serves as the hardrawer of actual motion and the reading sensor serves to return its actual moving distance for the Encoder.



Figure 1: Close-loop Control architecture of Motor control system

Control system description

The hardware related to the control system in the test is composed of three portisms: the first is, the computer-controlled center, including the PVA-1004 mailtoire processor equipped with R-1 module, the analog is pusitoinput module. TPGA module: the analog is pusitoinput module in onlight forms, and the analog is pupitoirely module in onlight forms, and are then along the pupitoirely module in the first of the analog is pupitoirely module in the along to pupitoire motion signal along the reserving that as inspection information on distance charges can be accessed the value of Encoder Cont.



Figure 2: System architecture of R-T control system

PROGRAM INTERFACE

Program interface applies National Instruments Lab/IEW as the layout. One can acquire system information from the graph, including Encoder, analog output waveform and set point information; moreover, the content of the program is composed of high resolution analog output module reading program, data storage, dual core control and synchronice motion control program.



Figure 3: The visual Control interface

FIRMWAVE CONTROL

To enhance stability and instantaneity, the integration of firmware's closed loop controls and motor controllers is used to maintain the accuracy of required locations through reduced time of communication with computers. In the following procedure of firmware's closed loop control, the required location is identified through analog output on the computer. While the location information required by controllers through analog input is digitized by way of the firmware program. the closed loop controlled module of the firmware system will initiate location modification. Since there's the farthest distance be-tween the starting point and the targeted one, the enhanced motion distance will be the likewise farthest. The shorter motion distance is then used to make modifications. While the location is reached within the range of tolerable errors, the closed loop control will run into a status of placidity and the entire system will run stably. In this state of stability, if any displacement takes place the system will move its structure to a correct position in order to lock in the location.



Figure 4: Flow chart of Firmware control system

CONCLUSION

The FPGA hardware module can trigger signals activation and integrate with highresolution analog input/output module to inaccompany. RT System, while the software applies the closed loop control module, which can enhance the stability of stopper motoe control to a 10-nanometer level. Consequently, the system can effectively enhance the stability and convenience of beamine controlling, and the RT system can effective enhance the area can address and FPGA system can reduce signal error caused by deferred time and thus improve the real-time efficiency of signal process.

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