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FIRST SELAP ALGORITHM OPERATIONAL EXPERIENCE OF THE NEW LLRF 3.0 RF CONTROL SYSTEM*

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Abstract

The JLAB LLRF 3.0 system has been developed and is replacing the 30-year-old LLRF systems in the CEBAF accelerator. The LLRF system builds upon 25 years of design and operational RF control experience (digital and analog), and our recent collaboration in the design of the LCLSII LLRF system. The new system also incorporates a cavity control algorithm using a fully functional phase and amplitude locked Self Exciting Loop (SELAP). The first system (controlling 8 cavities) was installed and commissioned in August of 2021. Since then, the new LLRF system has been operating with cavity gradients up to 20 MV/m, and electron beam currents up to 400 μA. This paper discusses the operational experience of the LLRF 3.0 SELAP algorithm along with other software and firmware tools like cavity and klystron characterization, quench detection and dynamic power allocation for beam current.

INTRODUCTION

The CEBAF Accelerator at Jefferson Lab provides electron beams to four different physics (experimental) halls at energies up to 12 GeV. This is accomplished using two linacs with over 400 superconducting cavities (SC) in 53 cryomodules. The linacs are connected with two recirculating arcs. Three of the experimental halls can receive up to five passes and a fourth can receive 5.5 passes [1]. The overall delivered dp/p rms energy spread is $5x10^{-5}$ at currents up to 400 uA (cw).

As part of the CEBAF improvement plan, a new cryomodule, C75, has been developed by modifying an existing older cryomodule [2]. The modified cryomodule cavity's Q_{ext} is 1.5 x 10^7 and has a Q_0 of 8 x 10^9. Average cavity gradient for C75 cavities is approximately 16 MV/m. In addition to the cryomodule upgrade, the plan calls for upgrading the RF zones with new LLRF systems (LLRF 3.0), which will replace the old analog LLRF (LLRF 1.0) designed in late 1980s. Every cavity is powered and controlled individually, similar to the older RF systems. The cavity amplitude and phase field stability remains unchanged and must be smaller than 0.04% and 0.5 deg rms. respectively, for measured frequencies > 1 Hz.

LLRF 3.0 HARDWARE

The new LLRF system design builds upon experience from the older CEBAF LLRF designs, and the recent participation in the LCLS-II LLRF design. The system utilizes a modular architecture concept, where the RF receiver, RF transmitter, fast digitizer and the FPGA carrier are separate printed circuit boards.

RF Transceiver

There are three high frequency receiver channels (1497 MHz) and one high frequency transmitter channel (1497 MHz). The RF receiver and transmitter use heterodyning in a double balanced, level 13 frequency mixer. The RF receiver channels are designed to provide very high channel to channel isolation (>90 dB).

The RF receiver and transmitter are in the same chassis as the digitizer and FPGA carrier. This was done to keep the cost low and allow the new system to fit into the existing racks. The down side of this is an added crosstalk of 6 dB to the receivers from the transmitter, which is still within the LLRF requirement of 80 dB.

Fast Digitizer and FPGA Board

Digitizer has four inputs to the ADC, two DAC outputs and a clock generator. AD9653 is used for ADC to process the 70 MHz inputs from RF receivers, DAC9781 for the DAC to generate the 70 MHz for RF transmitter and LMK03328 for the clock generator. Input to the clock generator is 70 MHz master reference.

The FPGA board is designed based on Intel Cyclone 10GX 672 pin FPGA. This board uses a MAX10 FPGA for power sequencing and monitoring and is available in four different sizes for resources (85k Logic Elements, 105 k, 150 k and 220 k). It is flexible in this sense that the user can choose one of the options at the time of assembly without changing the design. The FPGA board can be connected to a server using the SFP module or RJ-45 for communication over Ethernet. QSFP modules are useful, if there is a need to exchange information between the boards at high speed (e.g., 2.5 Gbps).

The RF chassis communicates with an IOC using UDP protocol. RF chassis in a zone are connected to an IOC over a private network. All the chassis can transfer the data at 1 Gbps as the link between the server and the switch is 10 Gbps.

CONTROL ALGORITHM

The control algorithm is based on a digital Self Excited Loop concept [3-5] and extended by an amplitude and Phase Lock feature. This replaces the analog GDR (Generator Driven Resonator) based systems LLRF 1.0 and digital SEL/GDR LLRF 2.0 firmware. To distinguish this from of GDR topology we use name SELAP (SEL with amplitude and phase locked). Figure1 shows a block diagram of this algorithm that was first developed for LCLS-II LLRF project [5]. At JLAB we developed a full (cavity +SELAP

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controller) Matlab model to better understand dynamical behavior of this topology, followed by developing VHDL firmware.

As one can see when the magnitude PI controller output is constant and the phase PI controller equals 0, the system is in free running SEL mode. Applying magnitude feedback, the amplitude is locked (stabilized), although the system is still in SEL mode. This mode (called SELA) helps with compensating small amplitude modulation caused by SEL mode imperfections.

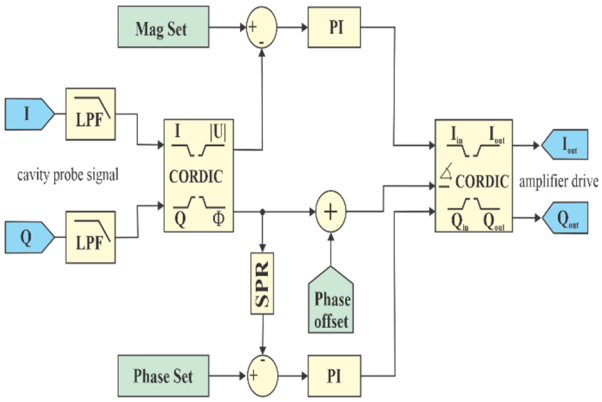

Figure 1: Locked amplitude and phase (SELAP) concept.

Once the phase loop is closed (SELAP), the system will compensate any cavity detuning by adding an offset vector (Q in Fig.1). In practice, the system remains in full SELAP mode as long as it has enough RF power. If the system clips/saturates the RF power, the phase loop unlocks itself. The system generates a beam shutdown signal for the machine. Once detuning drops below power saturation, the phase loop locks back and beam operation can continue.

During simulation (Fig. 2) the narrow region in the middle of the graph reveals enough RF amplifier power to fully lock the cavity phase. When detuning rises again, forward power grows until it loses phase lock and the system reverts to unlocked phase operation.

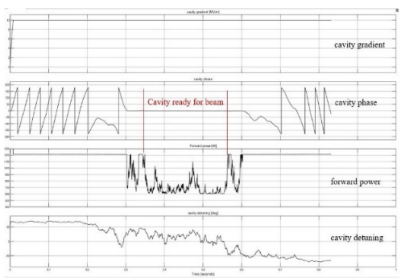

Figure 2: SELAP simulation.

Cavity phase information, depending on the status of the phase lock, needs to be processed by the so called "Stateful Phase Resolver" (SPR) [6]. The SPR output is equal to +/- Pi when the phase is spinning clockwise/counterclockwise or follows the cavity phase when sufficient RF power is available.

C75 OPERATION

SELAP operation starts with klystron characterization. This procedure, automatically measures the maximum linear power of a klystron and then calculates X and Y vector limits. While the Y vector limits depends on cavity gradient and expected maximum, detuning allowance thus can be calculated "off-line", X vector limits depends not only on cavity gradient but also on the beam load. The information about beam current is constantly monitored and is used to adjust this limit.

The klystron characterization routine is executed without cavity detuning (bypassing) by using very short RF pulses (< 200 microseconds). This short period prevents significant cavity field build-up.

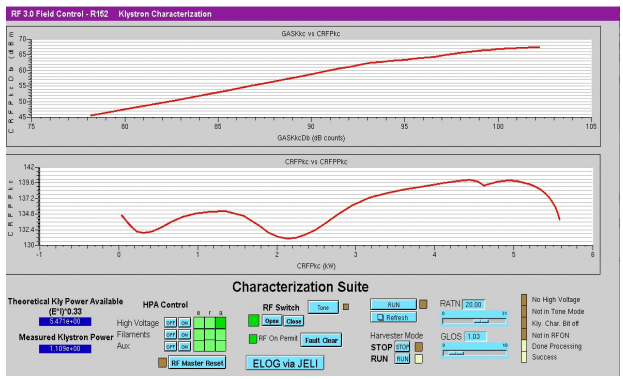

Figure 3: Klystron characterization screen.

Figure 3 shows a graph with completed amplitude and phase vs power (kW) measurement.

The next routine, called cavity characterization, provides a fully automated measurement of cavity external Q and gradient calibration (Fig. 4). Once characterization is completed, both coefficients are loaded into respective PVs (EPICS Process Variable).

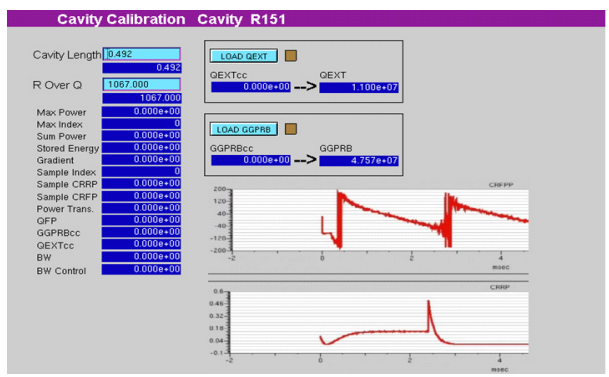

Figure 4: Cavity characterization screen.

There are a few more steps before the RF system is ready for beam operation. These include:

- Operate cavity in SEL mode and find optimal control loop phase (for given amount of RF power, cavity reaches maximum gradient).
- Final check of resonance control system operation and detuning angle zeroing.
- Switch to SELA mode. Forward power should not rise significantly (<10%). Larger value may suggest incorrect control loop phase.
- Switch to SELAP mode. Forward power rises due to compensation of the cavity detuning (microphonics). Cavity is ready for beam operation.

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Once SELAP mode is established, there is no reason other than system maintenance /troubleshoot to switch to other modes for cavity recovery. In the case of an RF trip, an operator only needs to push RF ON button and the cavity is ready for beam operation within 1-2 seconds.

Cavity field regulation was measured using third party instrumentation and therefore includes the LO (Local Oscillator) noise, which is typically subtracted from results presented in many papers. The cavity gradient stability maintained by the SELAP controller is shown in Fig. 5. Amplitude modulation is 0.00726% rms and +/-peaks are below +/-0.03%. This result well exceeds the CEBAF SC cavity field gradient stability requirements of 4.5×10^{-4} [7]. During initial setup we use LLRF acquired waveforms to ptimize P and I gains for the gradient loop.

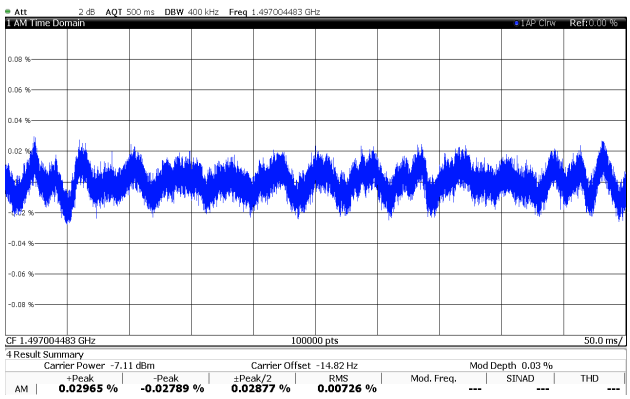

Figure 5: Cavity gradient noise measurement.

Figure 6 shows integrated (1Hz-10 kHz) rms phase noise of 60 mdeg (or 112 fs) measured for the C75 cavity. Phase loop regulation exceeds stability requirements by a factor of eight. The cavity microphonics detuning (25 Hz- 60 Hz) is well compensated by the feedback, where all mechanical mode related noise peaks are below -70 dBc. Marker M1, located at frequency of 383 Hz, shows phase modulation purposely induced by the CEBAF Master Oscillator Modulation System, a beam based linac cresting routine. This phase modulation is small enough that the energy spread generated by this variation remains insignificant.

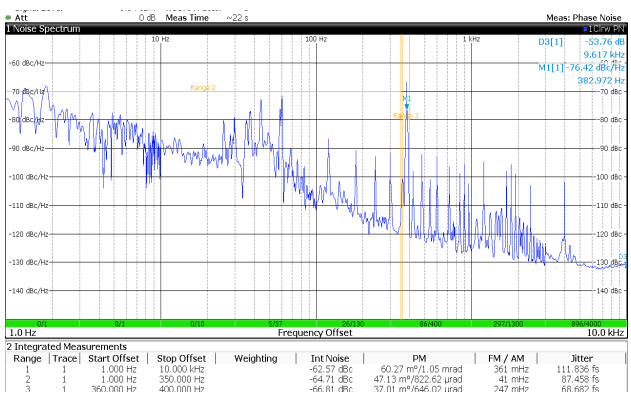

Figure 6: Cavity field phase noise.

CONCLUSION

The new design builds upon our own experience as well as our collaboration on the LCLS-II LLRF project. The modular architecture can easily accommodate new operational frequencies as needed in CEBAF. The upgraded firmware greatly improves superconducting cavity operability. Recovery from an RF trip is instant (once conditions causing trip have been resolved) and does not require any human interaction.

System performance while in SELAP mode is similar to when placed in GDR controller mode. It can be challenging to select limits for X and Y vectors when a cavity is driven near the klystron limit. One possibility is to lower cavity gradient, another is to accept an elevated number of beam trips.

LLRF 3.0 hardware/firmware/software is now used in two CEBAF zones (2x8 cavities) and LLRF 3.0 firmware has been installed in older LLRF hardware (LLRF 2.0) and controls one zone. We are planning to propagate SELAP controller firmware to all digital LLRF systems for SC cavities in the CEBAF accelerator.

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