FRIB

FRIB FAST MACHINE PROTECTION SYSTEM: CHOPPER MONITOR SYSTEM DESIGN LINAC18, TUPO007

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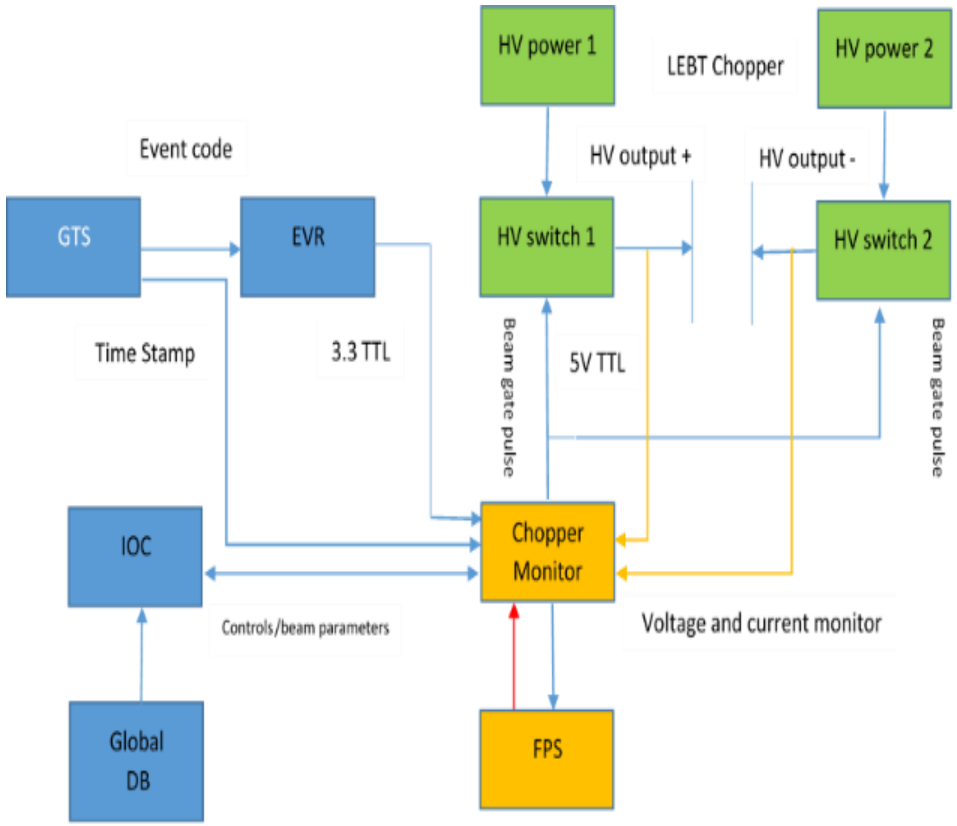
LINAC18 TUPO007 Talk Outline

- Introduction
- Chopper Monitor System Design
- Chopper Current Monitor
- Chopper Monitor Verification Test for Commissioning Cryomodule
- Conclusion

Introduction

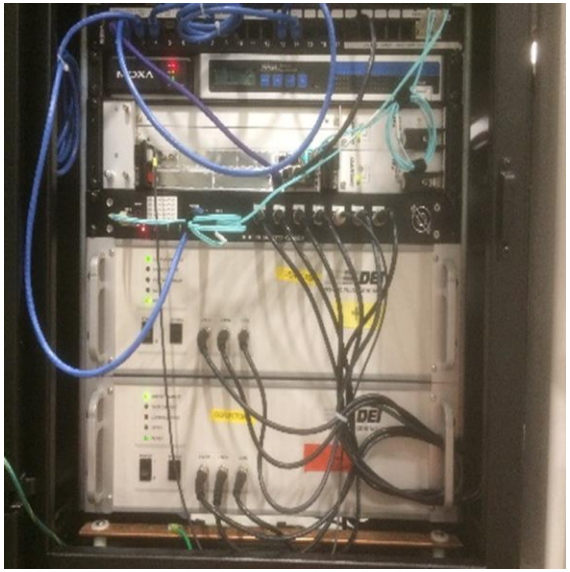
- FRIB Tunes the beam power from 0 to 400KW with a LEBT beam chopper
- A chopper monitoring system is employed to verify proper chopper operation to avoid delivery of undesired high-powered beam and to inhibit beam for machine protection purposes
- Challenges to design the chopper monitoring system include monitoring a dynamic beam gate pulse structure with pulse lengths as short as 0.6 μs and high voltage power supply current pulses at chopper of ~25 ns



Chopper Control System Block Diagram

Chopper Monitor System Design

- The system consists of chopper monitor chassis, EPICS IOC and CSS OPI
  - IOC/OPI: establish the chopper operational state, configure the chopper monitor for checking the beam pulse pattern for various beam modes, and providing the threshold values necessary for checking the amplitudes of each HV pulse and charge/discharge current.
  - Chopper monitor: FGPDB and high speed ADC board developed to communicate with MPS, check the beam gate signal from the EVR and HV switch, provide gate control inputs to the HV switches, monitor the HV switch output voltage and current signals (V_{mon} and I_{mon}). The I_{mon} signal is integrated by a high speed integrator circuit at ADC board.



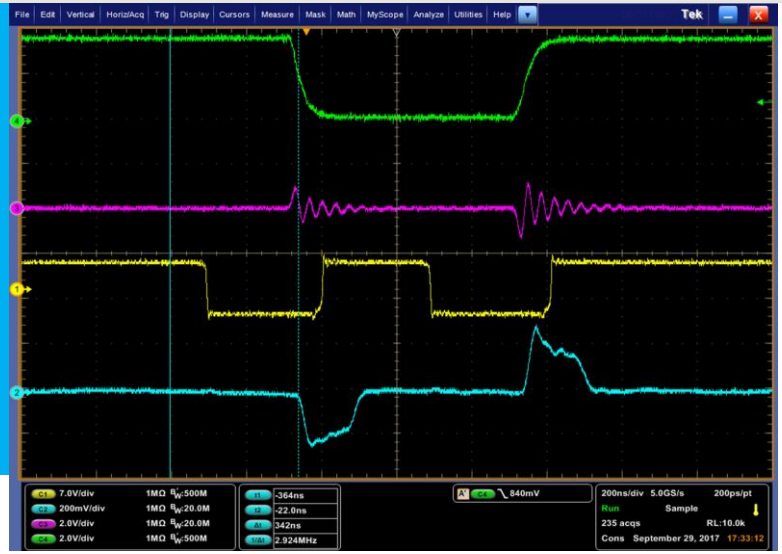
Chopper Monitor Rack at LEBT

FGPDB and high speed ADC board developed

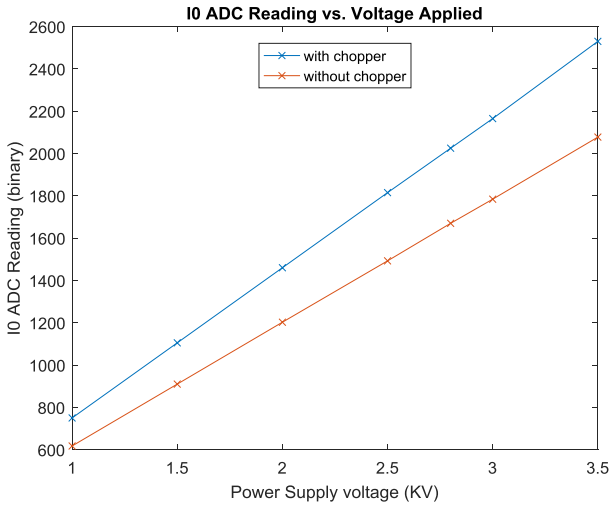
Chopper Current Monitor

- The major challenge is to monitor charge/discharge current of chopper
- A fast integrator with reset circuit is designed. The ADC reading of I_{mon} integrator output is proportional to the charge changes of chopper.
- Chopper capacitance calculated to be 53.9 pF by measuring integrator output while capacitive load is with and without chopper, result is close to actual value. A disconnected electrode is thus easily detected

Signals of integrate and hold circuit. Channel 1 is the charge reset signal (active high), channel 2 is integrator output, channel 3 is the current monitor output from HV switch, and channel 4 is the voltage monitor output.

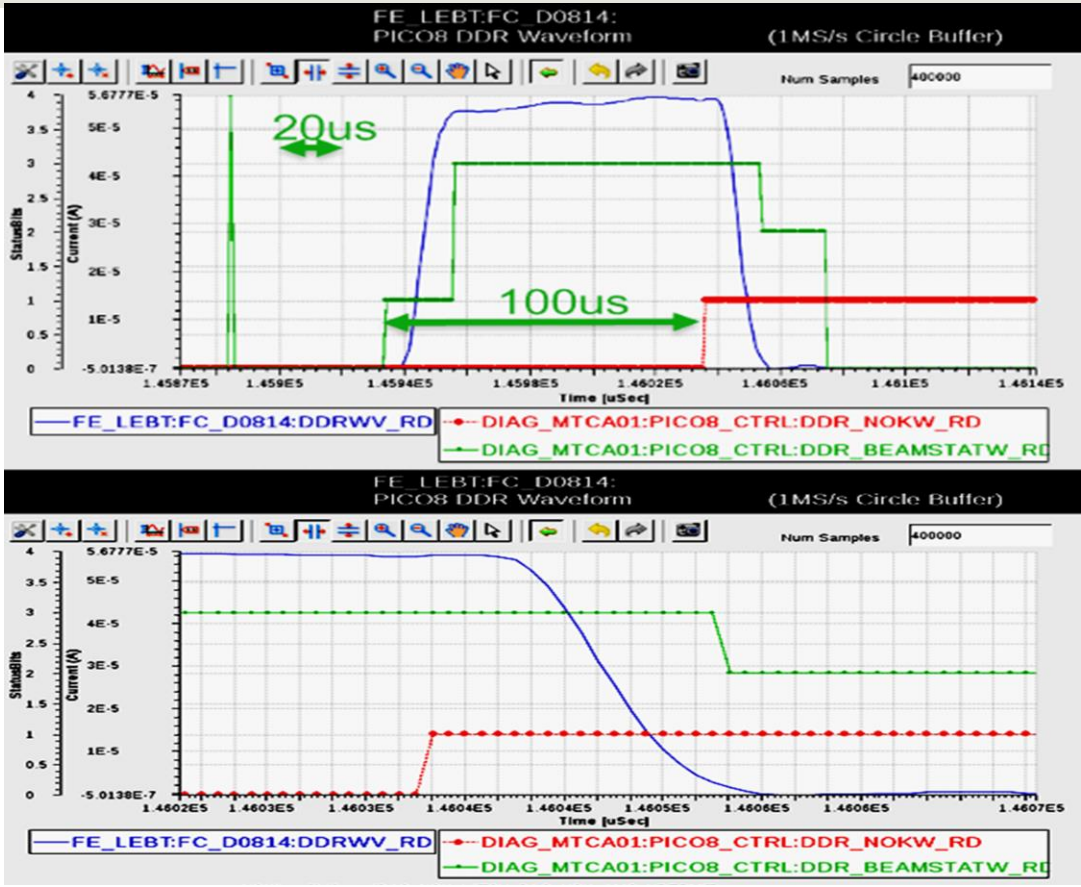


ADC reading of charge/discharge current versus high voltage applied to the capacitive load of HV switch, with and without chopper



Chopper Monitor Verification Test for Commissioning Cryomodule

- The chopper monitor function of pulse checker, voltage and current monitoring and machine protection are verified under conditions to limit total average beam power for FRIB beta=0.041 cryomodule commissioning.
  - In one of tests, system is configured with 100 μs duration periodic pulse while chopper monitor is configured with 100 μs+-1.2 μs, beam is delivered and monitored at a Faraday Cup (FC) immediately downstream of the chopper. Once 100 μs operation is established, a change to 120 μs pulse duration is requested without chopper monitor reconfiguration. It shows that chopper cuts off beam within tens of ns while pulse duration exceeds 101.2 μs.



State transitions immediately following the request for 120 μs pulse duration while chopper monitor is configured with 100 μs +- 1.2 μs

Conclusion

- Chopper monitor functions have been tested for commissioning the cryomodule and diagnostic beamline, all results meet MPS requirements.
- Implementation of the FPGA logic to check the dynamic beam power ramp up processes will be the next level development for the chopper monitor.

Questions? You are very welcome toTUPO007 Poster