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IMPLEMENTATION OF THE BEAM LOADING COMPENSATION ALGORITHM IN THE LLRF SYSTEM OF THE EUROPEAN XFEL

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Abstract

In the European XFEL, a maximum number of 2700 electron bunches per RF pulse with beam currents up to 4.5 mA can be accelerated. Such large beam currents can cause a significant drop of the accelerating gradients, which results in large energy changes across the macro-pulse. But, the electron bunch energies should not deviate from the nominal energy to guarantee stable and reproducible generation of photon pulses for the European XFEL users. To overcome this issue, the Low Level RF system (LLRF) compensates in real-time the beam perturbation using a Beam Loading Compensation algorithm (BLC) minimizing the transient gradient variations. The algorithm takes the charge information obtained from beam diagnostic systems e.g. Beam Position Monitors (BPM) and information from the timing system. The BLC is a part of the LLRF controller implemented in the FPGA. The article presents the implementation of the algorithm in the FPGA and shows the results achieved with the BLC in the European XFEL.

INTRODUCTION

The European X-Ray Free Electron Laser (XFEL) [1] is coherent light source providing laser pulses of tunable wavelength by the SASE process. It uses an electron beam accelerated to 17.5 GeV in 2 km long superconducting linac, which operates in a pulsed mode. The main superconducting linac in XFEL has been divided into 25 RF stations. Each of the RF stations consist of four cryogenics accelerating modules (CM), one klystron and a dedicated LLRF system that is split into master and slave subsystems [2].

The XFEL general bunch pattern consists of up to 2700 electron bunches with a variable charge distribution at a repetition rate of 4.5 MHz. To ensure highly reproducible and stable photon pulses for users, it is required to regulate precisely the RF filed inside the accelerating cavities, which should be ensured by the Low Level RF (LLRF) system.

The key element of the LLRF system is the digital feedback controller, which is a distributed system that has been implemented in Micro Telecommunications Computing Architecture (MTCA.4) [3]. Its main task is to compensate for field perturbations inside cavities using the feedback information about this field. However, high beam current can cause a significant drop of the accelerating gradient which cannot be compensated using a feedback controller i.a. due to its limited bandwidth. To overcome this issue it is required to use more complex algorithms like Beam Loading Compensation (BLC).

LLRF SYSTEM OVERVIEW

There are two MTCA.4 crates installed at each of the RF stations, one crate in the master and one crate in the slave LLRF subsystems. The simplified block diagram of a RF station is presented in Fig. 1.

One LLRF MTCA.4 crate is filled out with six pairs of down-converter (uDWC) - digitizer (uADC) boards, LLRF controller (uTC), CPU, crate management module (MCH), timing card (x2timer) and a vector modulator placed only in the master crate. Each LLRF subsystem processes RF signals from two cryo-modules while only the master system provides the drive signal to the klystron.

The uTC board in the master subsystem contains the main LLRF controller. It collects all the feedback data which are required to generate proper drive. All the algorithms are implemented in the FPGA chip located on the uTC board. The feedback data are transmitted over optical links or over differential lines within the crate and are received by the main controller using Multi-Gigabit Transceivers (MGTs).

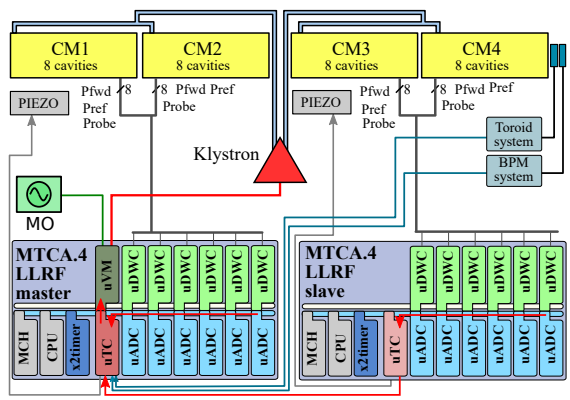

Figure 1: Simplified block diagram of the LLRF system installed at one RF station in XFEL.

BEAM CHARGE INFORMATION

The information about current beam charge can be obtained from the Beam Position Monitor (BPM) and toroid systems. They are located upstream the RF station [4]. Each of these systems sends the data in a real time to the main LLRF controller over a separate optical link working at 3.125 Gbps. A dedicated protocol has been settled, which defines packet of the data transmitted to the LLRF controller. The BPM data packet is presented in Fig. 2.

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Additionally to the current beam charge information the timing system provides the expected bunch pattern information. This information is sent from x2timer to the uTC board using the Multipoint-Low Voltage Differential Signaling (M-LVDS) lines located in MTCA.4 crate backplane before the RF pulse starts.

Byte			
3..0	Start of Frame (K27.7 & 0x00)	Intra pulse Bunch Number	header
7..4	Charge [pC] (float)		data0
11..8	Position X (float)		data1
15..12	Position Y (float)		data2
19..16	Status (16 Bit)	Detected Bunch Num	data3
23..20	CRC 32		CRC
28..24	End of Frame (K29.7)		EOF
bit	31 16	15 0	

Figure 2: BPM data packet send to the LLRF system.

BEAM LOADING COMPENSATION ALGORITHM

An electron beam passing through the cavity induces a voltage proportional to the current and the cavity shunt impedance which results in the cavity gradient drop. The feedback loop tries to compensate for this perturbations but due to the limited bandwidth it is not able to do it (Fig. 3a). Solution to this problem is to include scaled beam charge information into the feedforward signal [5]. However, the beam charge information appears in the LLRF system with the delay resulting from the detection of bunches and data transmission. As a result, the first bunches see a different cavity gradient. Also after the last electron bunch there is an overcompensation (Fig. 3b). To overcome this issue a pre-compensation and gating algorithm is used. The principle of its operation consists in insertion of the beam charge information from the previous pulse before the charge information from the current pulse arrives, and then disable BLC when the beam is not awaited (Fig. 3c). The algorithm requires the expected time of the beam. This is ensured by the module that receives the data from the timing system (x2timer). The module can generate indication of the expected beam as well provide coarse values of the expected beam charge.

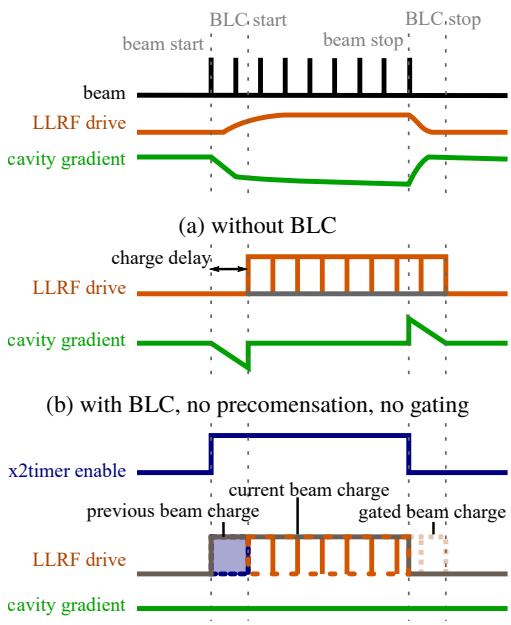

Figure 3: Beam loading compensation and cavity gradient.

At the European XFEL the maximum bunch repetition rate is 4.5 MHz. This is also the frequency of data received by the BLC algorithm. However, the repetition rate of bunches might be lower. In such a case, the algorithms puts zero charge in the place of missing bunches. This gives automatic scaling to the current by controlling of the duty cycle of the compensation signal. It will be shown in the result section.

FPGA IMPLEMENTATION

The main LLRF feedback controller is implemented in FPGA Kintex7 chip located on uTC board (commercial available card DAMC-TCK7). The project was build using the MTCA.4 firmware framework developed in DESY [6].

The block diagram of the firmware including most important components of the main LLRF controller is presented in Fig. 4. The signal flow starts with the calculation of the vector sum, resulting from the contribution of partial vector sums (PVS) of four cryomodules (CM). The controller starts with an error calculation followed by a proportional and a multiple input, multiple output (MIMO) feedback controller. The beam loading compensation (BLC) is placed just after feedforward (FF) and FF correction signals. Finally the klystron linearizion and output correction are applied before the signal is send to the vector modulator for up conversion.

The block diagram of the BLC component is given in Fig. 5. This module implements previously described algorithm. The orange fields in the figure indicate registers that are set by the user during a calibration process. Mainly the scaling of the beam charge and the rotation of the correction vector has to be set. The source of the beam charge infor-

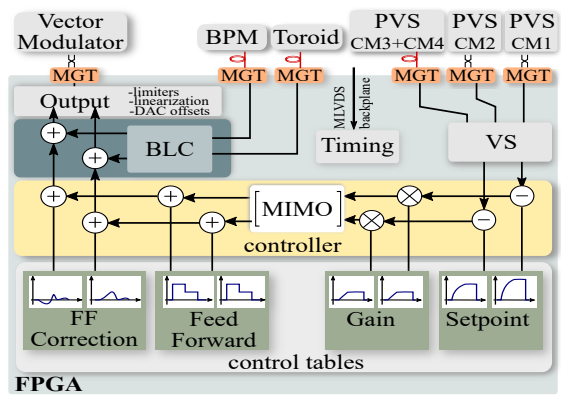

Figure 4: Block diagram of the uTC firmware including the most important components of the LLRF controller.

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mation can be selected between BPM and Toroid systems, which gives redundancy and the possibility to select the best source.

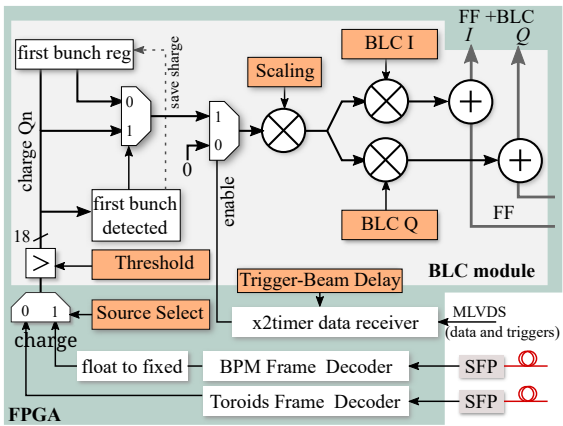

Figure 5: Block diagram of BLC module implementation.

RESULTS

The BLC has been implemented and successfully tested at the European XFEL. Up to now, tests were performed only with the beam charge information provided by BPM system. The results of BLC working for a bunch pattern with 0.25 nC and 1 MHz repetition rate are presented in Figs. 7 and 6. The results of BLC working for a bunch pattern with 0.25 nC and 4.5 MHz repetition rate are presented in Figs. 8 and 9. These figures present the controller output with included BLC signal as well the cavity gradient with enabled and disabled BLC while the feedback loop is closed. We can observe different behavior of the controller output depending on the bunch pattern, as it was described in BLC algorithm section. Presented figures shows that BLC can successfully compensate gradient disturbance caused by passing beam. In Fig. 9 we can see the overcompensation after the beam is off. In this case, it is due th fact the bunch number is shorter then the expected one.

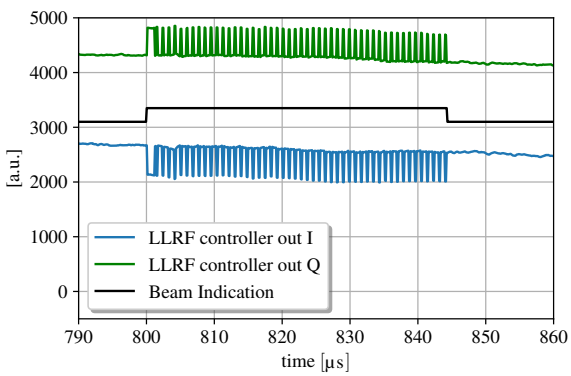

Figure 6: Controller output with the BLC enabled for beam with 50 bunches with 0.25 nC @1 MHz repetition rate.

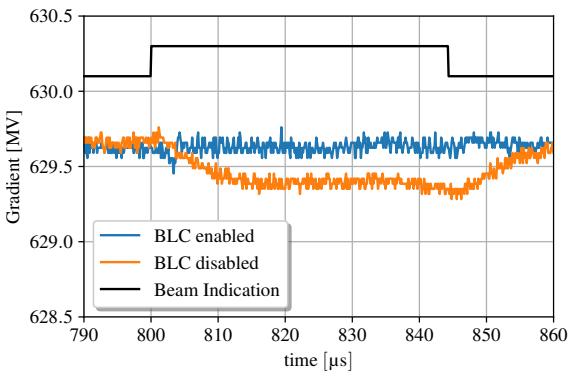

Figure 7: Cavity gradient with BLC enabled and disabled for beam with 50 bunches with 0.25 nC @1 MHz repetition rate.

CONCLUSION AND OUTLOOK

This paper describes a concept of the beam loading compensation method used at the European XFEL. The algorithm as well as its implementation has been described. The presented results show that the addition of the real-time BLC to the LLRF system improves the system response to beam transients.

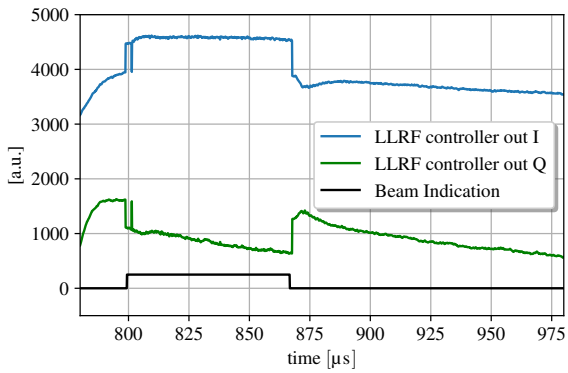

Figure 8: Controller output with the BLC enabled for beam with 300 bunches with 0.25 nC @4.5 MHz repetition rate.

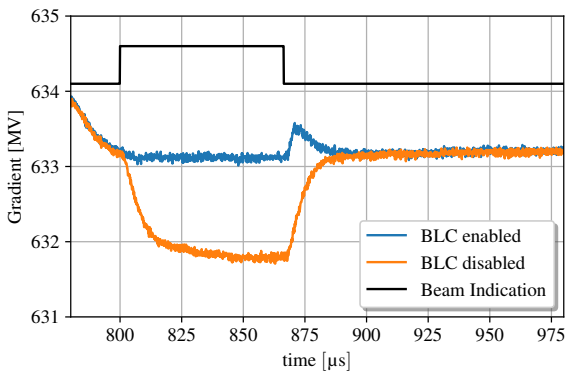

Figure 9: Cavity gradient with BLC enabled and disabled for beam with 300 bunches with 0.25 nC @4.5 MHz repetition rate.

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