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FRIB FAST MACHINE PROTECTION SYSTEM: CHOPPER MONITOR SYSTEM DESIGN *

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Abstract

The Facility for Rare Isotope Beams tunes the beam power from 0 to 400KW by chopping the beam current with a beam chopper in the Low Energy Beam Transport. A chopper monitoring system is employed to verify proper chopper operation to avoid delivery of undesired high-powered beam and to inhibit beam for machine protection purposes. The system monitors the incoming beam gate time structure, the chopper switch high voltage pulses, the chopper electrode charge/discharge currents, and the status of machine protection system. It is designed to switch off the beam within tens of nanoseconds of a detected fault. Challenges include a dynamic beam gate pulse structure with pulse lengths as short as 0.6 μs and high voltage power supply current pulses of ~25 ns. A high speed "integrate and hold circuit with reset", Field Programmable Gate Array based digital control circuit and high speed ADC circuit were developed to fulfil the required functions. Design approach, simulation, and test results with the beam are the focus of this paper.

INTRODUCTION

The average beam power in Facility for Rare Isotope Beams (FRIB) [1-3] is determined by the instantaneous beam current and the duty factor. When beam is requested, the duty factor is determined solely by the beam chopper in the Low Energy Beam Transport (LEBT). Therefore, chopper is actually a fast-acting, 0-400 kW control knob on the beam power. The FRIB chopper control devices, displayed in Fig. 1, include an Event Receiver (EVR) providing the beam gate signal, positive and negative high voltage (HV) power supplies providing 0-4kV and -4kV-0V respectively, and positive and negative HV switches to drive the chopper electrodes in the beam line. The chopper monitor system serves the ultimate purposes of preventing delivery of undesired high-powered beam and inhibiting beam for machine protection purposes [4]. The system is designed to receive the beam gate signal from the EVR, verify its acceptability for the current beam mode, drive the HV switch inputs, monitor the high voltage output pulses, monitor the chopper charge/discharge current, monitor the status of Fast machine Protection System (FPS) [4], and to inhibit the beam within tens of nanoseconds of a fault. The beam gate can exhibit a dynamic structure to ramp up beam power in a few seconds and the pulse lengths can range from 0.6 μs to nearly 10 ms. It is an engineering challenge to monitor every pulse of this ramp up process with a set of configurable parameters. The high voltage pulses exhibit rise and fall times ≤25 ns which poses difficulty for accurately measuring the charge and discharge currents. A Field Programmable Gate Array (FPGA) based digital control circuit, high speed "integrate and hold circuit with reset", and high speed ADC are employed to fulfil the required functions. Design approach, architecture, simulation, test results to meet these challenges are discussed in the following sections.

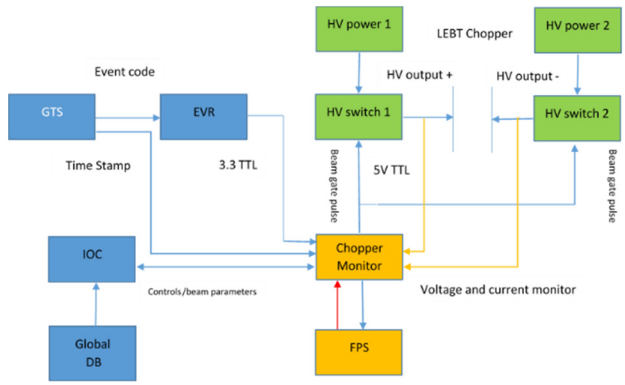

Figure 1: FRIB Chopper Control and Monitor System block diagram.

DESIGN

The chopper monitor system consists of chopper monitor chassis, Input Output Controller (IOC), and Operator Interface (OPI). The IOC/OPI serves to establish the chopper operational state, configure the chopper monitor for checking the beam pulse pattern for various beam modes, and provide the threshold values necessary for checking the amplitudes of each HV pulse and charge/discharge current. The chopper monitor system hardware consists of an FRIB General Purpose Digital Board (FGPDB) [4], the chopper monitor ADC board, and required power supplies. The chopper monitor ADC board interfaces to the MPS, the beam gate signal from the EVR, the control inputs to the HV switches, and the HV switch output voltage and current monitor signals (V_{mon} and I_{mon}). The I_{mon} signal is integrated by a high speed integrator circuit. A 14 bit, 125 Msps low power quad ADC, the LTC2175, is used to digitize the V_{mon} and integrated I_{mon} signals. The ADC board also contains a high speed DAC circuit to calibrate the ADC circuit and a circuit to monitor the board power. The FGPDB controls the DAC circuits, resets the integrator, initializes the ADC, and reads ADC outputs. The core of the FGPDB is a Spartan-6 XC6SLX150T-2FGG900C FPGA [4].

The FPGA firmware architecture includes a Micro-Blaze System to manage the circular buffers of ADC waveform data, EPICS communication and other management functions. It also includes a chopper monitor logic which consists of an embedded EVR, MPS-related logic, pulse

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checkers, ADC and DAC logic, and board power monitor logic.

PULSE CHECKER

The pulse checker verifies the beam gate pulse structure from EVR and the HV pulse applied to the chopper. FRIB beam modes require various beam gate time structures, where those of the beam power ramp up processes are the most dynamic and complicated. Each ramp up process consists of N_{RP} number of ramp up phases where pulse width or cycle time will be linearly ramped up to a target value at each phase through numbers of steps. Following parameters are used to define these steps: S_w, the step size to increase pulse width; N_{sw}, the total number of steps to increase pulse width; S_c, the step size to increase the pulse rate; N_{sc}, the total number of steps to increase the pulse rate; N_R, the numbers of repeated machine cycles at each step. Each machine cycle starts with a gap time of T_G (usually 50 µs) and repeats the machine cycle time T_{MC} (usually 10 ms). The pulse will be repeated with the numbers of N_p at each machine cycle and the pulse width T_w and the pulse period of T_c. The pulse checker is configurable with all the parameters described above to check various beam mode pulse structures. The pulse check is designed with a clock rate of 80.5MHz and time resolution of ~12.5 ns to check the pulse width and cycle time.

VOLTAGE AND CURRENT MONITOR

The voltage monitor circuit includes Vmon analog output from HV switch, attenuator, ADC and FPGA. A sample of Vmon is displayed in channel 4 of Fig. 2. Both the low and high of the Vmon will be measured and registered in FPGA. The current monitor circuit includes Imon analog output from HV switch, the 'integrate and hold circuit with reset', attenuator, ADC, and FPGA. The Imon signal of each HV switch is integrated for 25-50 ns during the electrode voltage transition time. The integrator output is held until it is readout by the ADC, and then reset before the next electrode voltage transition. The integrator must be fast enough to separately capture the current at both the rise and falling edge of a 0.6 µs pulse. Current monitor signals are displayed in Fig. 2 with a 3.5 kV pulse is applied to a capacitive load equivalent to real case. Channel 4 is the voltage monitor output from the positive HV switch showing 3.5 kV switched off for 600 ns and then back on. Channel 3 is the current monitor output from HV switch, showing the discharge current (with some ringing) when HV is removed from positive plate of chopper and then the charging current when HV is re-applied. Channel 2 is the integrator output, which represents the total charge applied to or removed from the chopper plate and associated cables. Channel 1 is the charge reset signal (active high) which resets the integrator capacitor. This capacitor is reset just before the charge and discharge current arrives to minimize signal offsets. The delay apparent between the reset signal and the integrator output resetting to zero is caused by switch-on time of the analog switch used in the reset circuit.

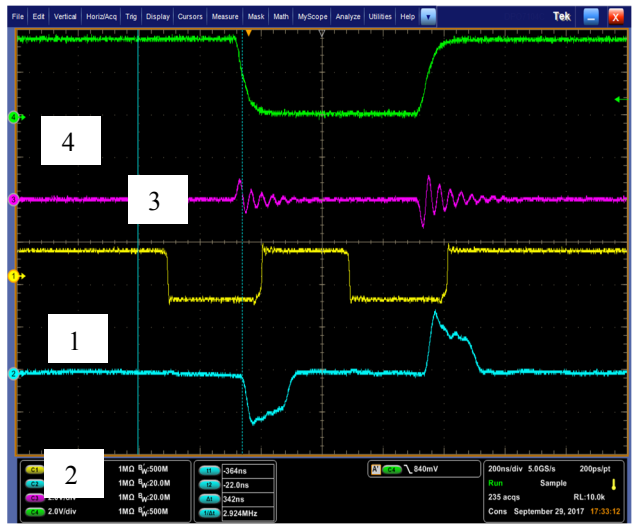

Figure 2: Signals of integrate and hold circuit. Channel 1 is the charge reset signal (active high), channel 2 is integrator output, channel 3 is the current monitor output from HC switch, and channel 4 is the voltage monitor output.

The sensitivity of the charging current measurement to faults in the HV electode and associated cabling is as follows. Let the load capacitance of the HV switch be C_{load}, which is the sum of C_{sw} (the HV switch internal capacitance), C_{cable} (the HV cable capacitance), and C_{chop} (the chopper electrode capacitance). Let V_H be the HV switch output voltage, Q_{chop} be the charge required to achieve V_H at the electode, R_{int} and C_{int} be the integrator parameters, V_{in} and V_{int} respectively be the integrator input and output voltages, and k be a constant.
The following equations apply:

$$Q_{chop} = V_H \times C_{load}$$

$$V_{int} = \int_0^T \frac{V_{in}}{R_{int}C_{int}}\,dt = \frac{kQ_{chop}}{R_{int}C_{int}}$$

$$C_{load} = C_{sw} + C_{cable} + C_{chop}$$

R_{int}=50 Ω, C_{int} =1nF, C_{sw} = 120 pF, C_{cable} = 129 pF.

This shows that V_{int} measured is proportional to Q_{chop}. Measured V_{int} versus V_H is shown in Fig. 3. Find V_{int} is 2530 when V_H is 3.5 kV with chopper electrode connected

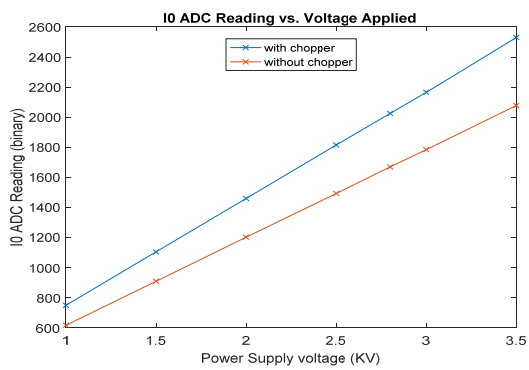

Figure 3: ADC reading of integrated charge/discharge current versus high voltage applied to the capacitor load of HV switch, with and without chopper (with C_{cable} and C_{sw} only).

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and 2080 with the same set up but chopper electrode disconnected. The above equations then give C_{chop} = 53.9 pF, which is very close to actual value of chopper capacitance. A disconnected electrode is thus easily detected.

$$I0_{ADC} = 710 * Vout + 39$$

TEST IN THE BEAM LINE

The chopper monitor chassis is installed in a rack directly beneath the chopper in the LEBT beam line. Starting from the bottom, the negative HV switch, positive HV switch, chopper monitor chassis and EVR chassis are mounted in the rack. The chopper monitor function of pulse checker, voltage and current monitoring and machine protection have been verified under conditions to limit total average beam power for FRIB beta=0.041 cryomodule commissioning. An example of a pulse check verification test is given below.

To validate the response to changes in pulse duration, beam events are configured for 100 µs duration pulses at 100 Hz. Chopper monitor is configured to check the same pulse width with error range of 1.2 µs. Beam is delivered and monitored at a Faraday Cup (FC) immediately downstream of the chopper. To validate the MPS response, a change to the pulse duration is requested that lies outside the allowed limits of 1.2 µs. Once 100 µs operation is established, a change to 120 µs pulse duration is requested without chopper monitor reconfiguration.

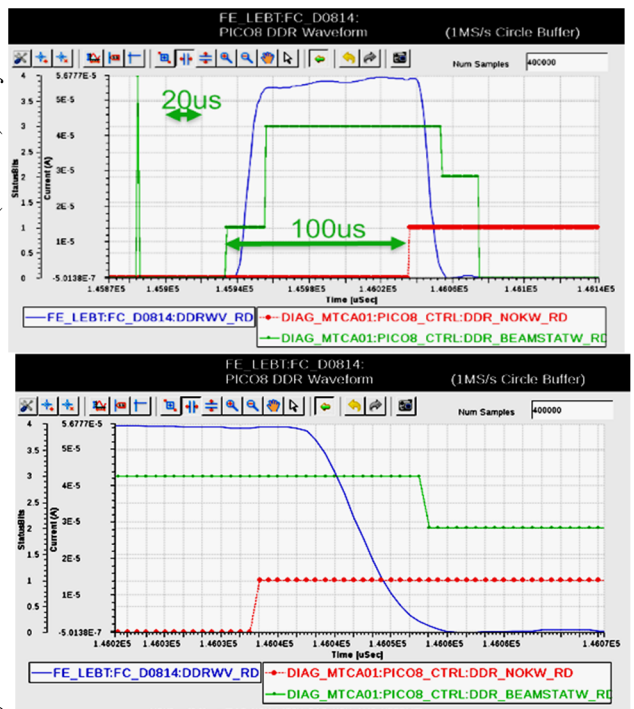

Figure 4: State transitions immediately following the request for 120 us pulse duration. Top display: the chopper monitor detects a beam-on condition (green) persisting longer than authorized, initiating the MPS NPERMIT response (red). Bottom display: expanded view of Faraday cup beam current signal.

Figure 4 displays the beam state transitions immediately following the 120 µs pulse duration request. It shows detection of beam-on condition persisting longer than authorized, initiation of the MPS NPERMIT response, and the resulting beam shutdown. The blue pulse is the beam current, the green line is the beam state detected at FC, where value 1 is beam start and 3 is beam on. The total pulse width applied is 120 µs. The red line is the MPS NPERMIT asserted high when a fault. When chopper monitor detects the pulse width exceeded 101.2 µs, it applies HV to chopper to cut off beam within tens of ns, meanwhile sends fault to MPS, MPS is tripped and sends NPERMIT high to FC, this period of time is about 3 µs. The blue pulse current in Fig. 4 cuts off 5 µs after NPERMIT high because of display delay of FC. The real beam actually is cut off before NPERMIT high. This test demonstrated that chopper monitor and MPS behave as expected [4].

CONCLUSION

The FRIB chopper monitor system is designed and deployed in the front end area of the high power heavy ion accelerator. The system checks every pulse width and cycle time, monitors the chopper high voltage pulses and the charge and discharge currents of the chopper electrodes, and forces a beam shutdown if any of these parameters are out of configured range. Chopper monitor functions have been tested for commissioning the FRIB beta=0.041 cryomodule and diagnostic beamline, and all results meet MPS requirements [4]. Implementation of the FPGA logic to check the dynamic beam power ramp-up processes will be the next level development for the chopper monitor.

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