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CEBAF PHOTO GUN RF SYSTEM*

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Abstract

During the CEBAF 12 GeV Upgrade at Jefferson Lab, a fourth experimental hall, "D", was added to the existing three halls. To produce four beams and deliver them to all halls concurrently requires new frequencies and a new timing pattern of the electron bunches. Since a photo-gun is used to produce electron bunches, the gun's drive laser pulses need to be synchronized with the required bunch rate frequencies of 499 MHz or 249.5 MHz. To meet these new operational requirements, a new RF system has been proposed.

Very specific requirement of dual frequency operation prohibited us from using a typical LLRF system. Limited budget and time forced us to use commercial off-the-shelf digital platforms. The commercial boards we chose include, the Texas Instruments FPGA board, the high-speed 8-Channel, 14-Bit ADC board, and a 4-Channel, 16-Bit DAC board. The DAC board includes the clock generator for clocking ADCs, DACs and the FPGA. A custom designed RF transceiver section provides the RF to the digitizer and vice versa for the DACs. The Gun Laser RF system has been designed, built, and recently commissioned in the CEBAF Injector. This paper will detail the design and report on commissioning activities.

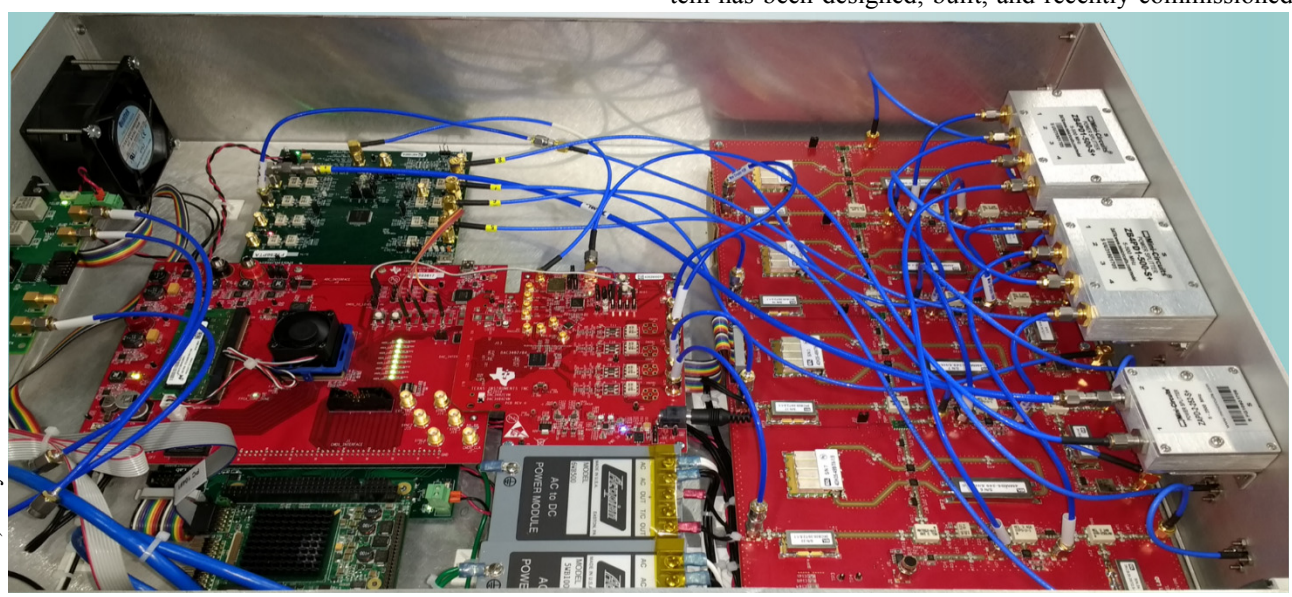

Figure 1: LLRF Chassis.

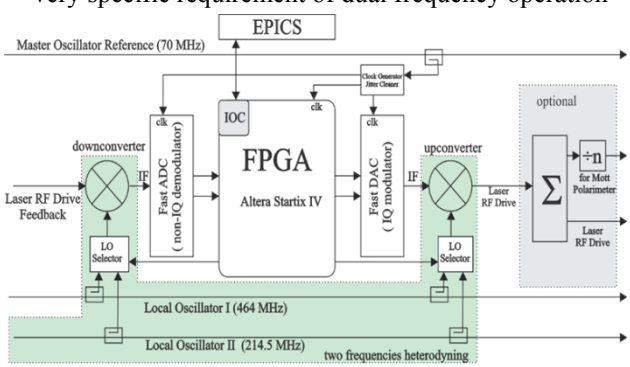

Figure 2: One channel of the Laser LLRF.

SYSTEM DESCRIPTION

Laser RF System consists of four RF receivers and four RF transmitters (see Fig. 1) allowing independent operation of four RF driven lasers [1]. The RF front-end section uses heterodyning in order to obtain 35 MHz IF signal (see Fig. 2). Depending on the required frequency of operation (499 MHz or 249.5 MHz), one of the two local oscillator (LO) frequencies (464 MHz or 214.5 MHz) can be selected. The digital section of the system contains an Altera Stratix IV FPGA, 1 GB memory and support up to 1.5 GSPS LVDS I/O rates for both ADCs and DACs (see Fig. 3). This board was built by Texas Instrument as a pattern generator/data capture system, and is compatible with multiple ADC and DAC boards from this manufacturer.

The ADS5294EVM board is an eight-channel, 14-bit serial LVDS interface, analog-to-digital converter with sampling speeds up to 80 MSPSs. that can be connected directly to the FPGA board. The DAC3484EVM is a DAC board that allows a user to operate a four-channel, ultra-

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low power, 16-bit, 1.25 GSPS DAC3484 digital-to-analog converter with 16-bit or 8-bit wide DDR LVDS data input, integrated 2x/4x/8x/16x interpolation filters, 32-bit NCO and PLL. We are using the DAC board's CDCE62005 based PLL system to generate clock signals for ADC and FPGA boards as well. For both boards, data and clock are sent through HSMC (High Speed Mezzanine Card) connectors.

The purpose of the digital section of RF is to regulate the magnitude and phase of the measured RF signal to a controlled set point. The input to the digital section is from an analog-to-digital converter that is driven by the down converted IF signal (35 MHz) which is clocked at 56 MHz (IQ sampling). The digital controller then compares this to the set points and processes the error signal such that a correction can be applied to the concerned signals. The correction signal from the FPGA drives a single digital to analog converter running at 140 MHz and then is up-converted to the required frequency. Although the presented RF system has a bandwidth of several MHz, feedback bandwidth will be limited down to a few kHz by digital filtering.

System is connected to the accelerator network via a PC104 operating as an EPICS input-output computer (IOC).

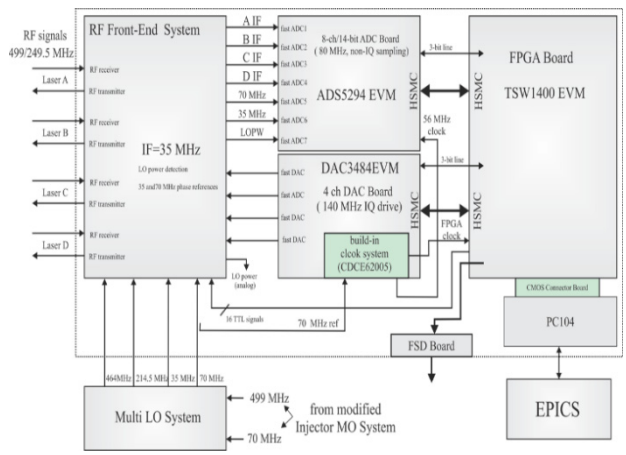

Figure 3: Block diagram of the system.

ADC/DAC BOARD CONFIGURATION

In order to send the register configuration to ADC and DAC boards without using the PC-USB interface (as expected by manufacturer), the TSW1400EVM board was modified in order to add six signal lines. Three of these lines are used to configure the ADC board and another three for the PLL clock configuration.

As it was already mentioned, for clock generation we use a CDCE62005 Clock Generator, Jitter Cleaner with Integrated Dual VCOs installed on the DAC board. RMS noise of this generator is typically below 1ps. We did consider to add alternative ultralow noise PLL system but bench testing of the existing one shows adequate noise performance.

PLL settings provides configuration of the on-chip PLL and is stored in EEPROM. This allows system to resume appropriate operation after power cycle.

BEAM FAST SHUTDOWN

Two out of eight ADC channels (ADS5294EVM) are used for continuous phase monitoring of two external reference signals: 70 and 35 MHz. In the case of a phase disturbances larger than 5°, the system interrupts beam delivery via the fast shutdown (FSD) system. The reason we monitor these signals is possibility of phase ambiguity produced by frequency divider used in Local Oscillator System (shown in Fig. 3).

OPERATIONAL EXPERIENCE

Figure 4 shows the four [2] gun operation screen. Operators can set amplitude, phase and one of the two possible beam frequencies for laser RF drive signal. Changing the frequency requires the RF signal to be off. EPICS expert level screens with detailed diagnostic and configuration tools can be launched from the operator screen. Selected signals are stored in the accelerator archiver and can be used off-line for system troubleshooting.

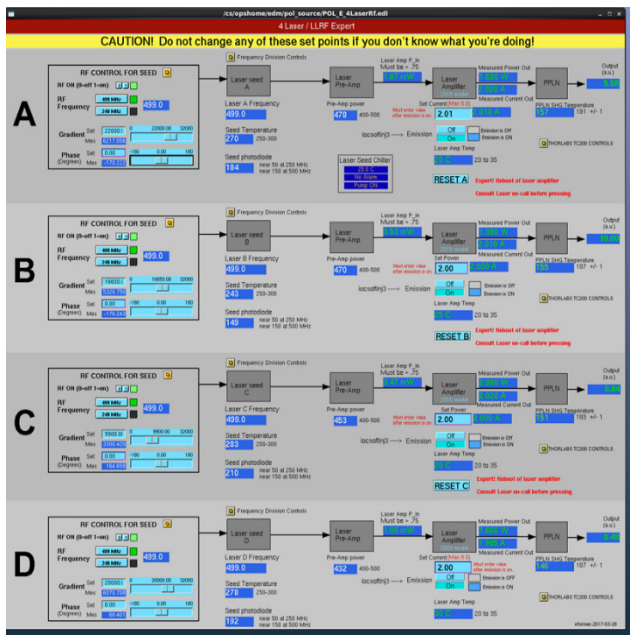

Figure 4: Operation screen.

In situ performance measurements were made during system commissioning. There was no measureable phase drift between beams over the course of several days. All RF signal spurs remained below -50 dBc, well below requested -40 dBc. Figure 5 shows chopper cavity viewers with four beams running at 249.5 MHz. By using one beam and sweeping the phase setpoint from -180 to +180 deg, the beam makes two successive circuits on the 499 MHz (2ns) chopper view screen.

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Figure 5: Four beams visible on the chopper viewer.

SUMMARY

This project is a good use of single unit production based on "off-the shelf" available evaluation modules rather than in-house design. The only custom design part remains the RF transceiver. By following this strategy we achieved significant reduction in the design effort, the cost of materials (e.g. cost of FPGA EVAL board is smaller than FPGA itself) and the delivery time.

There is no guarantee of future availability of evaluation modules, therefore purchasing additional spares is critical. There is always the possibility in the future of changing the system requirements, but by using modular product evaluation boards we have the flexibility to make future changes.

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