GATED FIELD-EMITTER CATHODES FOR HIGH-POWER MICROWAVE APPLICATIONS

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Abstract

Gated field-emitter cathodes have been fabricated on silicon wafers. Two fabrication approaches have been employed: a knife-edge array and a porous silicon structure. The knife-edge array consists of a pattern of knife-edges, sharpened to ~200 Å radius, configured with an insulated metal gate structure at a gap of ~500 Å. The porous silicon cathode consists of an insulating porous layer, containing pores of ~50 Å diameter, densely spaced in the native silicon, biased for field emission by a thin gate metalization on the surface. Emission current density of 20 A/cm^2 has been obtained with only 10 V bias. Fabrication processes and test results will be presented.

Introduction

The gigatron is a design for a compact, efficient microwave power tube suitable for use as a driver for future linac colliders [1]. The design concept features three novel developments: First, a gated field-emitter array is employed for the cathode, to produce a microwave-modulated electron beam directly into the vacuum. Second, rather than the conventional round beam, a ribbon beam geometry is adopted to mitigate limitations from space charge. Third, a traveling wave coupler is used to obtain optimum output coupling even with a wide ribbon beam. These features make possible a calculated performance suitable for linear collider requirements[2]: • 18 GHz operating frequency; • 100 MW/m peak power; • >50% efficiency.

The Accelerator Research Laboratory at Texas A&M University has developed two different technologies for the gated field-emitter cathode which is the heart of the gigatron.[3] A stripline knife-edge cathode was developed in which the control gap for modulation is ten times narrower than the gate/base separation. A porous silicon cathode was developed, in which ~50 Å diameter pores densely cover a silicon surface. Prototype 1 mm^2 cathodes have achieved 20 A/cm^2 peak current for a gate modulation voltage of only 10 V. These technologies provide ample performance for gigatron, and are the focus of our current development.

Gated field emission for microwave cathodes

Field emission occurs when an electron in a conductor tunnels through the potential barrier at the surface under the influence of a surface electric field E. The barrier height is the surface work function ϕ; the barrier width is $\sim \phi/E$. The current density j of field emission is the classic Fowler-Nordheim response [7]:

$$j = AE^2 e^{-b/E} \tag{1}$$

where A is proportional to the surface density of emitting sites; and

$$b = \frac{4\sqrt{2m}}{3\,\hbar e}\phi^{3/2} \tag{2}$$

C.S. Spindt et al.[4], H. Gray et al.[5], and W.J. Orvis et al. [6] have developed microfabrication techniques by which they can prepare planar arrays of gated field-emitting tips. The gated field-emitter cathode makes it possible to produce a high-current, fully modulated electron beam directly from a cathode structure. The performance of a gated tip array for microwave applications is governed by several key features [8]. First, the emission current is modulated by applying a d.c. bias and a microwave signal to the gate-base junction. Second, the gate-base junction is rendered on a microscopic scale ($\sim \mu$m) so that the modulation performance is not limited by transit time or phase dispersion up to ~ 100 GHz. Third, because the gate-base separation is narrow, the junction capacitance is large ($\sim 1\ nF/cm^2$) and represents a low reactance for microwave modulation. Fourth, emission from each tip structure actually originates from a single microregion (size a~50 Å) [9]; emission from the rest of the tip surface is suppressed by the space charge of the emitted electrons in the tip/gate region, leading to a "natural selection" of a single-most-emissive microregion on each tip.

We have developed two alternative field-emitter geometries which improve microwave cathode performance by increasing emitter density and reducing gate capacitence: a stripline knife-edge geometry shown in Fig. 2, and a porous silicon cathode shown in Fig. 3. Fig. 4 shows the emission characteristics for a) a molybdenum tip array fabricated by Spindt, b) a stripline knife-edge cathode, and c) a 2 μm thick porous SiO_2 cathode fabricated at Texas A&M. Table 1 summarizes the values of the several cathode performance parameters for the three technical approaches. The values of A/a^2 and a · b were derived from the measured I/V response for the tip array and the porous SiO_2 cathodes, as discussed above. The values of A/a^2 and a · b for the stripline cathode are estimates obtained by scaling the tip array data for the appropriate surface density of emitters and surface field enhancement of the stripline geometry.

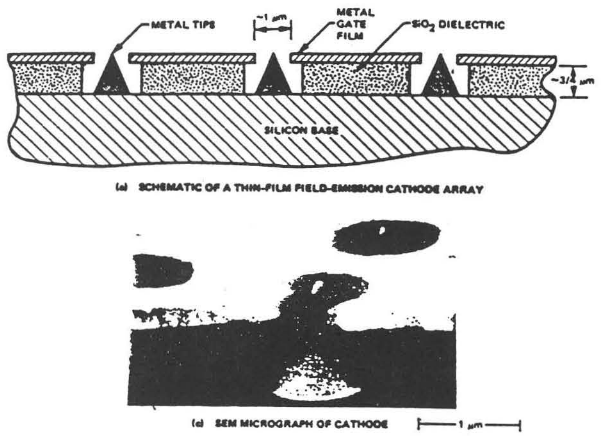

Fig. 1 Gated field-emitter tip array, from Ref 4.

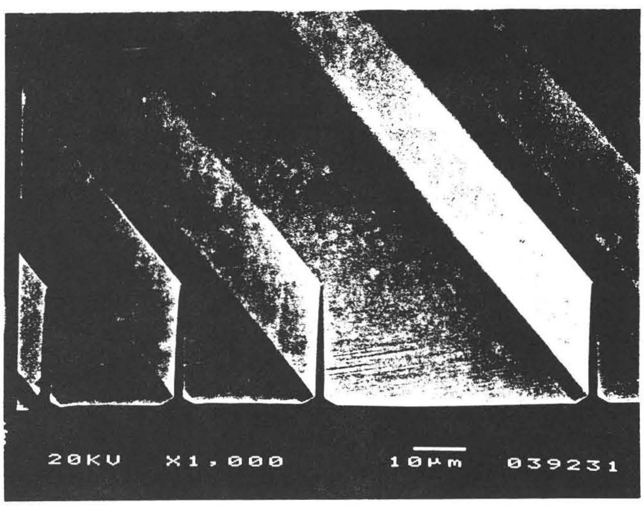

Fig. 2 SEM of stripline knife-edge cathode.

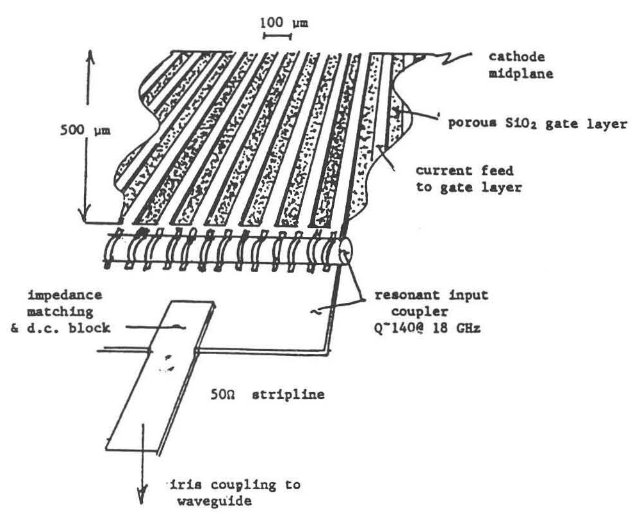

Fig. 3 Porous SiO_2 cathode structure.

The modulation voltage requirements were calculated to provide an rms current density of 50 A/cm^2 from the cathode, and a 10:1 ratio of on:off phase current. This emission would support 100 MW output power from a 1-m-long gigatron with 200 kV tube voltage. The last column presents the gain-bandwidth product of a gigatron employing each cathode technology.

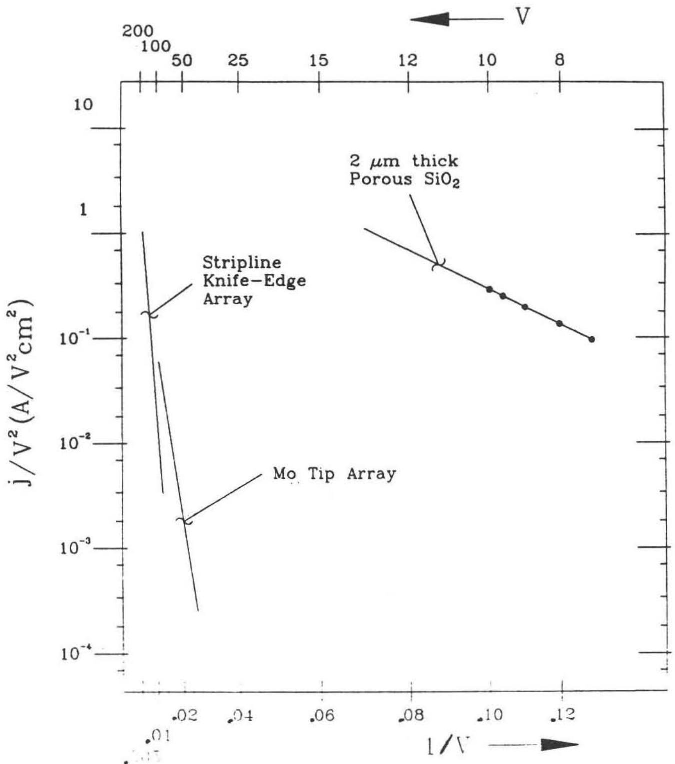

Fig. 4 Fowler-Nordheim response of tip, knife-edge, and porous silicon cathodes.

TABLE 1
Modulation Characteristics of Three Field-Emitter Cathodes

Cathode	A/a^2 $[A/V^2]$	$a \cdot b$ [V]	bias mod V_{DC}	V_{rms}	$\bar{C}$ $[nF/cm^2]$	$G \cdot f$ [THz]
tip array[a]	3.3	450	84	9.2	4.8	4
stripline[b]	270	1040	99	6.5	2.3	16
porous SiO_2[c] 2μm	14	36	14.3	2.6	.5	500

[a] Tip #28C-189-8N from Ref. [4], Fig. 4.
[b] A/a^2, $a \cdot b$ scaled from case a for tip density and surface field.
[c] Measured response of 1mm^2 cathodes.

Porous SiO_2 cathodes

Porous silicon is a remarkable material. When a heavily doped silicon wafer is electrolytically etched in hydrofluoric acid, a dense pattern of trunk-like pores are etched into the surface, with an average pore diameter on the order of one nanometer. The pattern is very dense: typically, half of the silicon is removed from the porous layer. The layer thickness can be controlled by etch time over a range of 0.1-100 μm. The pore diameter and the brachiation of pores can be controlled by process parameters (galvanic current density, pH of electrolyte).

Yue[10] has invented a way of transforming a porous silicon layer into a field-emission cathode. Following fabrication of a porous silicon layer, it is oxidized by heating in an oxygen atmosphere. The porous layer has an immense surface area, and oxidizes to completion very rapidly, leaving the bulk silicon substrate unoxidized. The resulting material consists of a pattern of channels imbedded in a dielectric matrix, with a conducting substrate exposed at the bottom of each channel. The silicon substrate forms a serrate surface at the base of each channel, and is observed to produce copious field-emission (20 A/cm^2 with 10 V modulation) with very low effective work function.

Stripline knife-edge cathode

The stripline knife-edge cathode design is motivated by the possibility of providing a larger surface density of emitting regions (see above and ref.[9]) than is possible with a tip array. In the stripline knife-edge geometry, the gap between knife-edge cathode and gate can be reduced to g∼500 Å. Following Hermannsfeldt's analysis[9], we would expect that microemitting regions would form on a spacing along the knife-edge comparable to this gap. For a gap of 500 Å, and a spacing of 5 μm between adjacent knife-edges, the emitter density should be $\sim 5 \times 10^7 cm^{-2}$. By comparison, the tip spacing of 9 μm for the tip arrays of Ref. 4 corresponds to an emitter density $\sim 10^6 cm^{-2}$; more recently Spindt has achieved $1.5 \cdot 10^7 cm^{-2}$ [11] tip density. The surface electric field at the knife edge is however reduced by a factor of $ln(g/a) \sim 3$ for a given modulation voltage compared to that in a tip geometry. This rescaling is reflected in the (estimated) coefficient a·b for the stripline knife-edge case in Table 1.

It is one thing to postulate an idealized stripline knife-edge cathode structure, and quite another to build it.[12] We have recently succeeded in building it. Orientation-dependent etching is used to produce an array of tall, rectangular blades on a silicon wafer. Dash etching is then used to sharpen the top edge of the wafer to a radius of about 500 Å. The etched edge is then oxidized in an oxygen-flow oven to diffuse oxide into the surface. The native silicon beneath develops a contour which is even sharper, with an edge radius of 50-200 Å. Once the oxide is removed by a final etch step (done after deposition of gate dielectric and metalization), the emitter edge is exposed. Figure 2 shows the array of sharpened knife-edges before application of dielectric and metalization layers. The gate/base dielectric is formed using a spin-on polyimide. Following planarization, the polyimide film is hard-baked and then plasma-etched to just expose the SiO_2-coated knife-edges.

The gate metalization is then applied using evaporation. The metalization forms an elevated ridge over each exposed knife-edge. The metalization is plasma-etched to just expose the SiO_2-coated knife-edge. A liquid-phase SiO_2 etch is then used to remove the SiO_2 layer, exposing the sharp Si knife edge and creating a narrow vacuum gap between the emitter edge and the gate metalization. The gap is controlled by the oxide thickness, and can be adjusted in the range 500–1000 Å. The polyimide dielectric separating the gate and base layers can be fabricated at any desired thickness up to ∼ 10 μm.

Conclusion

We have succeeded for the first time in demonstrating two viable procedures by which to produces all of the features which are key to cathode performance:

- large emitter density $\sim 10^8$-10^{10} cm−2.
- small emitter/gate spacing ∼ 500 Å.
- large gate/base spacing ∼ 6 μm.

Cathode performance to date produces 20 A/cm^2 with 10 V modulation, which would provide a gain-bandwidth product of 500 THz in an ideal gigatron. During the coming year we plan to evaluate 1 mm^2 knife-edge cathodes under modulation up to 3 GHz.

Acknowledgements

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