PULSED-LINAC SYNCHRONIZATION USING AN EMBEDDED MICRO-CONTROLLER

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Abstract

A Master Timing Generator (MTG) was developed using a single Motorola MC68332 embedded micro-controller. The MTG produces electrical synchronization pulses that coordinate the action of all pulsed subsystems and the acquisition of pulsed data. Pulse width and delay-offset of each of the 13 output channels can be changed on-line. The MTG is interfaced with a GE Series-Six Programmable Logic Controller (PLC), which coordinates overall control of the IMPELA™ linac. Serial communications are used between the PLC and the MTG. The PLC needs only transmit data to define the pulse repetition rate, the beam pulse width, and the subsystems that should be active. The MTG determines the widths and relative delays required to achieve the requested beam pulse-width. Changes in width and repetition rate are effected using a smooth ramp to avoid power-demand transients. All MTG timing requirements are met with the current implementation, having the following characteristics: 1 Hz ≤ repetition rate ≤ 500 Hz with ±1% resolution, 12 μs ≤ width ≤ 1000 μs in 1 μs steps, and a delay-offset range of 4.5 ms in 1 μs steps.

Introduction

Pulsed linacs require synchronization of the electron gun, the HV power supply modulator, the rf drive and the data collection electronics. In the IMPELA™‡ industrial application,[1,2] the synchronization implementation must meet the potentially conflicting demands of flexibility, cost-competitiveness and operational simplicity. These demands have been met using a micro-controller that integrates a multi-channel "timing engine", a CPU, serial communications modules, as well as other processor support functions.

Synchronization of IMPELA is achieved using an MTG (Master Timing Generator) that is interfaced with an industrial PLC (Programmable Logic Controller). The MTG consists of the above-mentioned micro-controller, line drivers, and a circuit card that permits on-site, non-volatile adjustment of timing parameters.

Following an overview of timing requirements, the MTG design and operating experience are outlined.

Requirements

The MTG was developed for the 10 MeV, 50 kW (avg.) member of the IMPELA family. However, broader requirements were called for to meet the demands of future IMPELA linacs, covering 5 to 18 MeV and 20 to 250 kW (avg.). Basic requirements are:

- 1 Hz ≤ PRF ≤ 500 Hz (Pulse Repetition Frequency) with 5% or better resolution (1% achieved).
- 12 μs ≤ pulse width ≤ 1000 μs with 1 μs resolution.
- pulse positioning (delay) range of ≥ 4.5 ms with 1 μs resolution.

On-line changes are possible for: PRF, pulse width, delay, and pulse enable/disable. Supervisory control is realized over a serial communications link, using the CCM* protocol. A set of switches provides in-field timing adjustment by unskilled operators.

Nine separate timing signals are required. Most are required in two locations, thereby requiring fan-out. In addition, an output at 10·PRF, 50% duty-factor, is provided for monitoring.

Example Pulse Sequence

Another MTG responsibility is pulse positioning as a function of beam width. The PLC command need only specify the desired beam width and PRF. The MTG must determine the required timing. Fig. 1 illustrates a long and short width case.

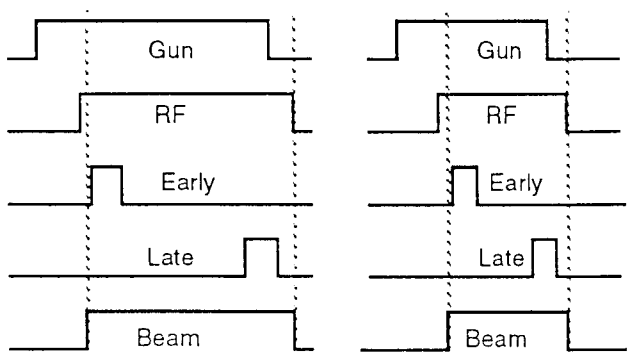

Fig. 1 Example Pulse-Timing Relationships

The gun and rf pulse widths exceed the beam width by a fixed amount. These pulses must also precede the beam by a fixed amount. The early and late pulses are data sampling triggers. The early pulse is positioned a fixed time into the beam, while the late pulse is positioned a fixed time before the end of the beam pulse.

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‡ Industrial Materials Processing Electron Linear Accelerator

* Communications Control Module protocol is a simple packet-based protocol typically used to connect a PLC with a display station or another PLC.

MC68332 Features

The development of the MC68332 was a joint effort of Motorola and Delco, the latter for automotive applications. It incorporates a 16 MHz, 32 bit CPU (68020-based), a System Integration Module[3] (SIM), serial communications hardware, a 16 channel synchronous Timing Processor Unit[4] (TPU) with 250 ns resolution and 2 kB of on-chip RAM. In the MTG, the CPU manages the serial link with the PLC. It interprets the commands, then sets TPU registers appropriately. The SIM manages pin function assignment (e.g., chip select range) and support functions, such as a watchdog; hence, very little support circuitry is required.

A MC68332 "Business Card Computer" (BCC) further reduces design effort. This BCC circuit card holds a MC68332, 128 kB EPROM (with debugging monitor), 64 kB RAM, serial drivers, clock circuitry, and two 64-pin connectors/headers. The BCC can be plugged into an evaluation/development system for code development, and then transferred to the target hardware. The headers permit attachment of a breakpoint computer or other debugging aid. The convenience of the BCC has been applied elsewhere in the construction of "smart" data acquisition and control electronics for a pulsed linac.[5]

MTG Structure

Hardware

A VME (3U x 84 hp x 160 mm) chassis houses the MTG cards and two power supplies. One card consists of 8 bytes of memory-mapped DIP switches, providing 16 µs width and delay adjustment to each channel. Baud rate and device identity are also set on this card.

The controller card is shown in Fig. 2. Due to the high level of integration on the BCC, the support electronics on the controller card consist simply of: RS-422 transceiver, EPROM, watchdog alarm buffering, and key-switch access to the BCC debug EPROM via a front-panel RS-232 port.

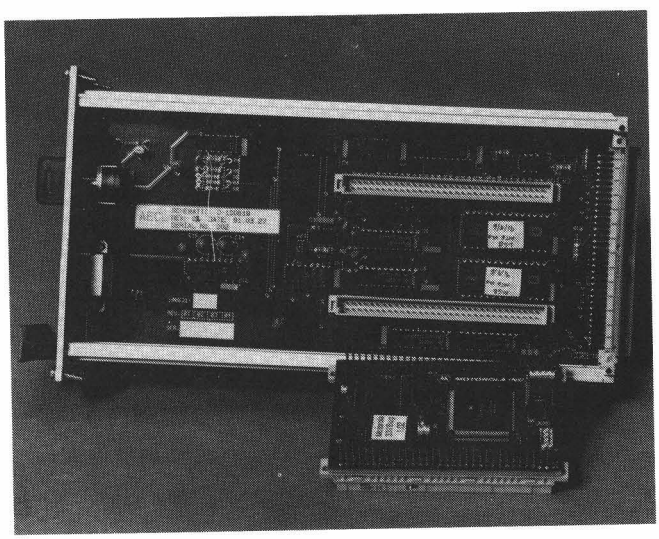

Fig. 2 Controller Card, BCC Extracted

One chassis supports eight line driver cards, delivering a total of 32 electrically-isolated, differentially-driven pulses. Any timing channel may be selected for output by appropriate jumper selection. Outputs are buffered for front-panel monitoring with an oscilloscope. A front-panel LED for each output line is also provided. These LEDs indicate whether the lines are adequately loaded, thus providing a means of broken line detection.

Timing Software

CPU The CPU code was written in 'C' language using a PC-based compiler. A skeleton of this code is shown in Fig. 3. An infinite loop services the watchdog, monitors communication activity and updates timing parameters during width or PRF ramps. Once PLC communication has been interpreted as a valid CCM packet, the command is extracted and checked against limits in PRF, width, duty factor, etc. Valid commands are used to generate a new set of timing parameters for use by the TPU.

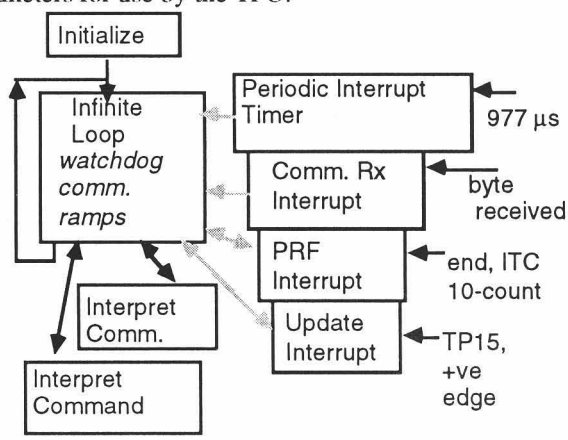

Fig. 3 Software Structure

Parameters are written into the TPU during service of TPU-generated interrupts. One TPU interrupt is used for updating the PRF and the other is used for updating the width and delay of all output channels.

Interrupt service routines are also used for each byte received from the PLC, and for an internal real-time clock that is used to time CCM protocol events.

TPU By manipulating TPU control registers, the CPU can configure a TPU channel to perform one of 16 functions programmed in TPU ROM. The ROM functions are not capable of simultaneously meeting the low PRF and 1 µs width/delay specifications. Custom TPU functions can be stored in the on-chip 2 kB RAM, which can be configured to replace TPU ROM.

A custom Synchronized One Shot (SOS) function was created by extracting the TPU ROM, using in-house programs to disassemble the code, and then manually programming the bit patterns for the SOS function in place of an unused function. The SOS function begins with a TPU-internal interrupt (link). Following a programmed delay, the voltage on the channel's

upon the cycle completes and the channel remains inactive until the next link.

Application of the 16 channels is shown in Fig. 4. A Pulse Width Modulation (PWM) function produces a 50% duty factor signal at 10·PRF. Generation of this signal is based on Timing Control Register 1 (TCR1), which increments on a 3.8141 μs interval. Two Input Transition Counters (ITC) divide the 10·PRF signal to produce links at the PRF. Two ITC channels are required, due to a link-limit of 8 channels. The first ITC interrupts the CPU on each 10-count, so that the PRF can be updated. This interrupt also notifies the CPU of each pulse trigger; thus, the CPU can implement single-pulse events.

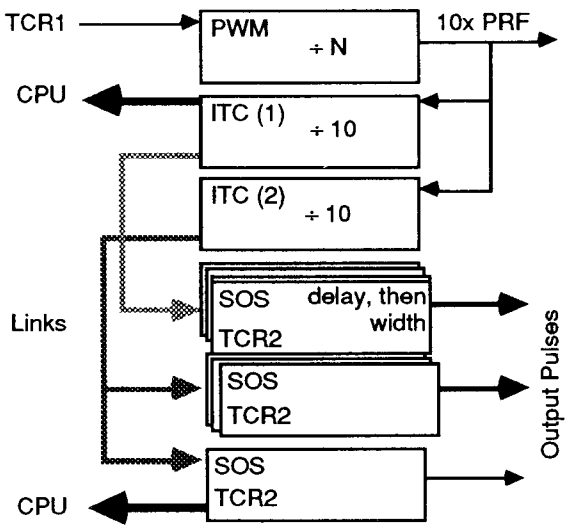

Fig. 4 TPU Configuration

SOS channels base their pulse delays and widths on TCR2, which counts on a 476.8 ns interval. The last SOS channel must be configured such that its pulse rising edge follows the rising edge of all other SOS pulses. The rising edge of this last pulse interrupts the CPU, allowing the synchronous update of all widths and delays.

Jitter between SOS channels is 80 ns. For the IMPELA 10/50, the minimum beam pulse length is 50 μs; hence, the jitter contributes < ±0.1% to beam current variability.

Communications

The MTG implements the slave portion of the CCM multidrop master-slave protocol. This protocol contains a Q (for Quick) and N (for normal) message type. The Q-message is used for status polling, while the N-message performs more substantial data transfer. The Q-message, issued typically every 100 ms, is responded to with a read-back of the current PRF and beam width. A single byte gives the operating status.

In this application, N-message transfers are limited to those originating with the PLC. The first byte of the 16 byte packet defines the command. The remaining 15 bytes carry command parameters such as PRF, width and/or a list of channels to be disabled/enabled.

The original design called for a continuous background of Q-messages, with N-messages issued only when a change was requested. It was assumed that the error detection and retransmission features of the CCM protocol would ensure reliable communication. While a reliable implementation of this design has been achieved, considerably more PLC code is required than was anticipated. One example of the problems encountered is the determination of when the MTG has received an N-message. The PLC buffer for the N-message must not be overwritten until the MTG has received the message. Despite explicit message-complete acknowledgement within the CCM protocol, no reliable means of obtaining this information was found at the PLC ladder-logic level. Hence, an additional status code was added to the Q-message response to synchronize PLC transmissions.

A simpler communications scheme is planned, whereby the PLC will maintain a setpoint area in memory that the MTG will read. The MTG then will write a complete status report back into PLC memory. PLC access to these memory areas would be asynchronous with MTG access.

Conclusions

The high degree of integration provided by the MC68332 and the BCC, coupled with the inexpensive PC-based development tools, permitted cost-effective development of a flexible, custom MTG.

An MTG has been in continuous service since 1991 August. Following the correction of subtle errors in the PLC communications code, service has been error-free. The on-line capability to adjust both pulse widths and PRF has proven useful during rf conditioning, and offers a simple means of extending the range of average beam power.

References

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[3] MC68332 SIM User's Manual, Motorola Inc. (1989).

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[5] S. Shtibu, R.W. Goodwin, E.S. M^{c}Crory, M.F. Shea, "Smart Rack Monitor for the Linac Control System", Proc. IEEE Part. Accel. Conf., San Francisco, 1991 May, pp. 1484-1486.