

# A NEW RF SYSTEM FOR THE CEBAF NORMAL CONDUCTING CAVITIES\*

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## Abstract

The CEBAF Accelerator at Jefferson Lab is a 6 GeV five pass electron accelerator consisting of two superconducting linacs joined by independent magnetic transport arcs. CEBAF also has numerous normal conducting cavities for beam conditioning in the injector and for RF extraction to the experimental halls. The RF systems that presently control these cavities are becoming expensive to maintain, therefore a replacement RF control system is now being developed. For the new RF system, cavity field control is maintained digitally using an FPGA which contains the feedback algorithm. The system incorporates digital down conversion, using quadrature under-sampling at an IF frequency of 70 MHz. The VXI bus-crate was chosen as the operating platform because of its excellent RFI/EMI properties and its compatibility with the EPICS control system. The normal conducting cavities operate at both the 1497 MHz accelerating frequency and the sub-harmonic frequency of 499 MHz. To accommodate this, the new design will use different receiver-transmitter daughter cards for each frequency. This paper discusses the development of the new RF system and reports on initial results.

## RF SYSTEM

The chopper and separator cavities are both beam deflecting cavities. In the case of the chopping cavities two orthogonal modes ( $Q_L$  11,000) are excited in a single copper structure, with mode isolation being greater than 40 dB. The electron beam is chopped and then “de-chopped” after the beam has been modified. The separator cavities use a TEM dipole mode ( $Q_L$  2500) that can deflect multiple beams [1]. The field control requirement for these cavities is relatively undemanding at 1% and 1 ps rms amplitude and phase control. In the case of the chopping cavities, the amplitude is rarely changed, but in the case of the separator, amplitude is adjusted to reflect the deflection needed for different beam energies. In both cases phase is adjusted upon initial start up of the accelerator and then tweaked as needed. Therefore the RF system can be rather simple.

Figure 1 shows a block diagram of the low level RF control system (LLRF). This architecture has become the common model for single cavity control LLRF systems, with 4 RF inputs and 2 RF outputs utilizing a modern large field programmable gate array (FPGA). We have chosen the VXI platform for both convenience and its RFI/EMI properties. The system utilizes a mother - daughter board with the FPGA on the motherboard and

the daughterboard hosting the RF hardware and analog to digital converters (ADC) and digital to analog converters (DAC) for both the receiver and transmitter. The motherboard will also be used in other applications at CEBAF such as a cavity BPM [2].

The RF system down converts the cavity frequencies (499 MHz and 1497 MHz) to an IF of 70 MHz. This allows us to use the local oscillator (LO) and IF signals that are already distributed around CEBAF. The receiver IF signals are then quadrature demodulated using harmonic under sampling (56 MHz clock). The transmitter output is a single IF output at 70 MHz where the quadrature components are digitally recombined inside the FPGA [3]. The signal is then filtered and up converted to the cavity frequency. Both forward and reflected powers are also monitored. The control system is a digital generator driven resonator (GDR), using a basic proportional and integral (PI) algorithm for field control [4]. All adjustable parameters such as gain, phase and gradient are embedded in the FPGA.

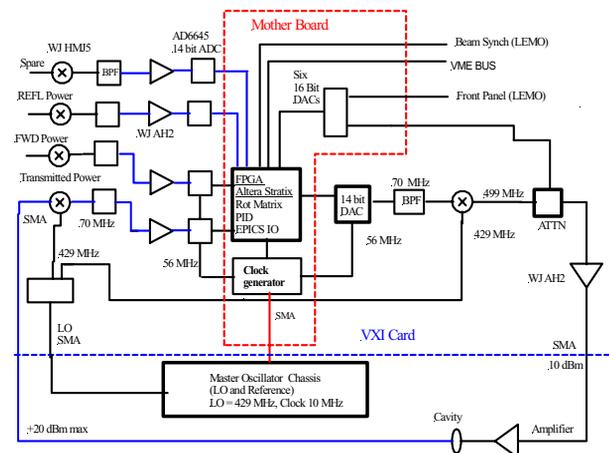


Figure 1: RF system block diagram.

## Receiver/Transmitter

The receiver/transmitter mates as a daughterboard to a VXI motherboard. FET mixers (WJ HMJ5) were chosen because of their linearity ( $IP_3 \sim 40$  dBm) and high dynamic range. To minimize amplitude drifts a product called Thermopads is being considered (an attenuator product with selectable tempcos). This will allow us to offset any temperature induced amplitude drifts in the RF signal path. A commercial IF filter was chosen for its low group delay  $\sim 80$  ns. In addition, a gentle lumped-element band pass filter designed to remove most of the out-of-band noise precedes the ADC. By including this we reclaim 1-2 bits of dynamic range in the ADC. The fast ADCs (AD6645) and a dual DAC (AD 9767) are included on this card. Because isolation between channels is also a

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concern, we have specified this to be 60 dB for the cavity transmitted power and 50 dB for all other channels. We intend to use diode ring mixer for the transmitter since the IP3 requirements are not as stringent.

The receiver has been modeled and tested in a variety of ways. First a simple spreadsheet was used to look statically at the systems gains, IP3 and SNR. If system properties such as saturations and/or any other non-linearity's appear normal, we then model the system with SystemView (a commercial software for receiver and RF design). This allows for dynamic modeling of the chosen components. Following this, bench testing commenced (IMD, dynamic range, tangential sensitivity etc.) on selected parts and any unknown data is fed back into the receiver model. In addition critical parts have been tested in an environmental chamber to measure temperature induced phase drifts. This design process has produced an extremely linear receiver. A complete receiver (2-channel) is presently being assembled for testing and evaluation.

**VXI Motherboard**

The VXI motherboard contains the digital electronics necessary to process digital signals to and from the daughterboard, interface to the VXI bus, and 10/100 Ethernet. As shown in Figure 2, the board features one Altera Stratix FPGA, 64Kx16 DPRAM, 1Mx32 RAM, 1Mx32 FLASH, Phase Lock Loop (PLL), six 16-bit 500K-sample DACs, 10/100 Ethernet, general purpose digital IO, and infrared input and output. The motherboard uses two 100-pin and two 20-pin stackable connectors to support daughter board(s). Each 100 pin connector has 70 digital I/O, PLL clock output, FPGA clock input, and digital powers. Each 20 pin connector provides VXI analog powers (+/-12V, +/-24V).

We chose an Altera Stratix FPGA with 18,000 to 25,000 logic elements (LE are the basic electronics building blocks), 80 eight-bit multiplier/ accumulators, and can support both hard coding and a soft microprocessor core (NIOS) simultaneously. Various operating systems including Linux can be loaded, and with its Ethernet support, the board can communicate with EPICS directly, thus bypassing the traditional EPICS IOC. We plan to use the NIOS processor as an EPICS IOC for future designs, migrating out of the VXI environment.

Care was taken in the design of the clock PLL to achieve a jitter of less than one ps. The PLL takes in an analog (or digital) signal from a front panel SMA connector and generates a square wave that is phase locked to the input. The clock signal is double buffered and distributed to the FPGA and to both 100-pin connectors. The signal from the SMA connector is buffered and distributed to both 20-pin connectors.

As shown in Figure 3, the connectors (100 and 20 pin) are situated on the board to support either one or two separate daughterboards. The 100-pin connectors provide the digital interface and the 20-pin connectors provide clean analog power. In addition, 16 digital IO (TTL)

points are available on an internal connector. Two digital inputs are available via the front LEMO connectors. These inputs are clamped to 4.7V and buffered with JFET. Infrared input and output are Agilent HFBR-241X and HFBR-141X respectively. Six analog outputs are available at the front panel LEMO connectors. Their magnitude and polarity are configurable from -14V to +14V.

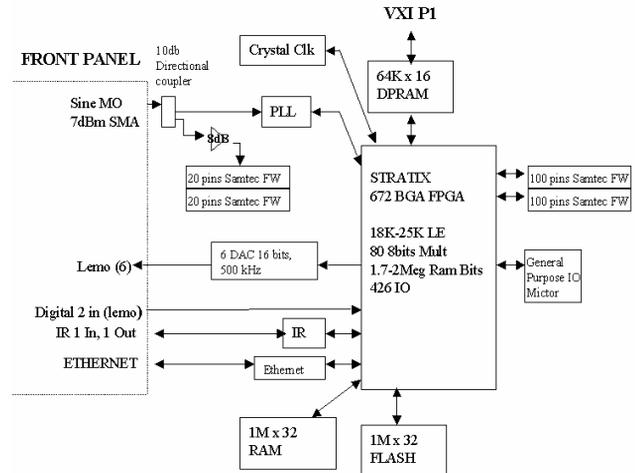


Figure 2: Motherboard Components.

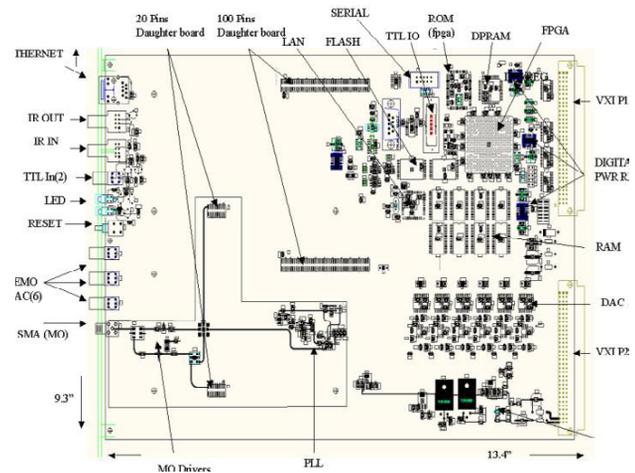


Figure 3: VXI Motherboard.

**MODEL & SYSTEM CONTROL**

System control was modeled and tested for a variety of cavity scenarios. The separator cavities and chopper cavities have much different  $Q_L$ 's (2500 vs. 10000). This ultimately affects the loop bandwidth and hence the gain parameters of the LLRF system. In the case of the chopping cavities the loop bandwidth is set by the cavity at ~25 kHz. This gives us adequate margin for Proportional (P) gain. Not so for the case of the separator cavity since it has a bandwidth of ~ 100 kHz. For the separator P gains < 3 are expected (limited by system delay). System delays have been measured in the evaluation system and we have settled on ~ 1.0  $\mu$ sec total

delay (the latency from ADC to DAC was measured to be  $\sim 0.5 \mu\text{sec}$ ).

We did investigate lowering the loop pole digitally with an IIR filter, but because of high clock frequencies, 56 MHz, and low loop filters needed  $\sim 1 \text{ kHz}$ , realization of these filters was not easily implemented [5]. The filter poles land very close to the stability circle on the z plane, and when programmed into the evaluation system, the loop tended to oscillate. It may have been possible to decimate down and implement the IIR filters at a lower frequency but we did not investigate this.

**Model Results**

Jefferson Lab uses Matlab and Simulink to model the response of its low level RF control systems [6]. The models for the warm RF cavities contain the basic elements of the two systems: a controller, a cavity, and cable and digital processor delays. While integral to the systems as a whole, the RF power amplifier and its effects are neglected in this initial set of models and will be included in subsequent versions. The controller consists of a 28 MHz sampling mechanism and PI controller. The cavity is modeled by its fundamental mode using the resonant cavity equivalent circuit equations, and the cable and digital processor delays are lumped together into one delay that feeds into the controller. Figure 4 along with Table 1 show the model and relevant modeling parameters.

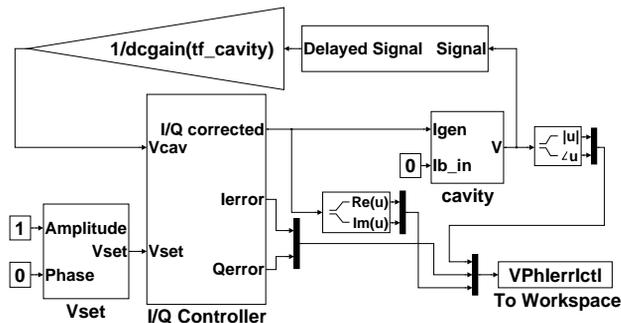


Figure 4: Simulink Model for 499 MHz cavity simulations.

Table 1: Cavity Characteristics used in Cavity Model

	Chopper	Separator
$f_0$	499 MHz	499 MHz
$r/Q$	14.4 $\Omega$	44.7k $\Omega$ /m $\times$ 0.3m = 13410 $\Omega$
$Q_L$	10000	2500
Bandwidth	24.95 kHz	99.8 kHz
Transfer Function	$\frac{2.257 \times 10^{10}}{s + 1.568 \times 10^5}$	$\frac{2.102 \times 10^{13}}{s + 6.271 \times 10^5}$

The cavity models were used to explore the P and I gain space to find a suitable integral gain and corresponding range of proportional gains that allowed the system to run without a loop filter. Simulations indicate that with an integral gain of 10000, the proportional gain can vary between 1 and 9 for the

chopper system and between 1 and 2.5 for the separator system. Figure 5 shows two cases for each system. The baseline case for each system has the integral gain set to zero and the proportional gain set to one which results in a negative feedback system with unity gain. The other case represents the maximum proportional gain for the integral gain that gives the least overshoot with the quickest settling time.

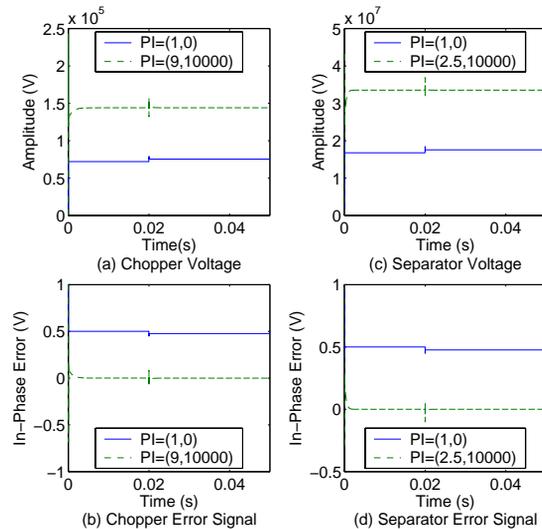


Figure 5: Simulation results for the chopper and separator cavities. Plots (a) and (c) show the amplitude of the cavity voltage for the baseline and maximum gain cases. Plots (b) and (d) show the in-phase component of the cavity voltage error signal for the baseline and maximum gain cases.

**SUMMARY**

Many of the major parts of the system have been tested on an evaluation platform (ADC, FPGA, DAC, control system firmware) using a simple cavity simulator. The motherboard has been designed and is undergoing tests. The receiver/transmitter card should follow shortly. The next step is to verify the model vs. the final hardware. We intend to install the new system in the spring and summer of 2005.

**REFERENCES**

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