Development of a New Interlock and Data Acquisition for the RF System at HEPS

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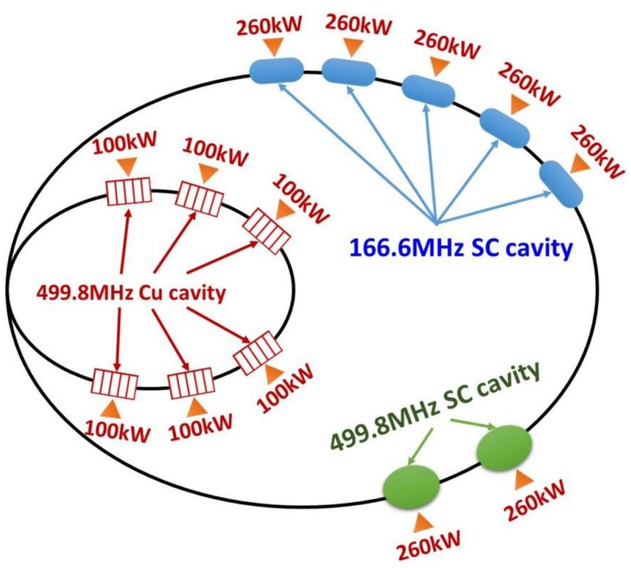
Abstract

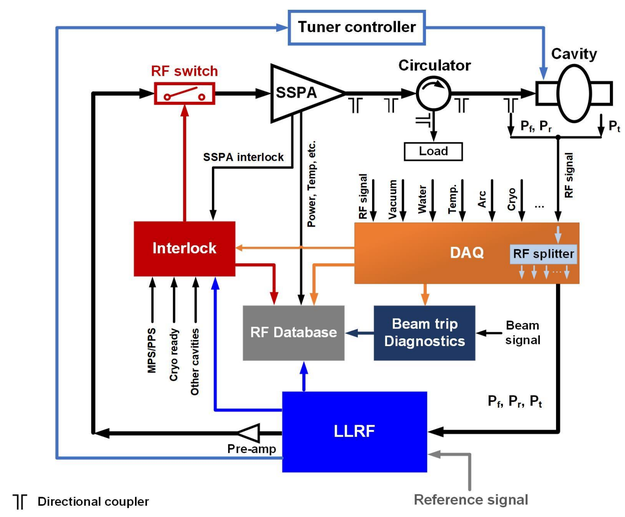
A new interlock and data acquisition (DAQ) system is being developed for the RF system at High Energy Photon Source (HEPS) to protect essential devices as well as to locate the fault. Various signals are collected and preprocessed by the DAQ system and individual interlock signals from the solid-state power amplifier, low-level RF, arc detector, etc. are sent to the interlock system for logical decision to control the RF switch. The programmable logic controller (PLC) is used to collect slow signals like temperature, water flow rate, etc., while fast acquisition for RF signals is realized by dedicated boards with down-conversion front-end and digital signal processing board. In order to improve the response time, field programmable gate array (FPGA) has been used for interlock logic implementation with an embedded experimental physics and industrial control system (EPICS). Data storage is managed by using EPICS archiver appliance and an operator interface (OPI) is developed by using control system studio (CSS) running on a standalone computer. This paper presents the design and the first test of the new interlock and DAQ for HEPS RF system.

1. High Energy Photon Source



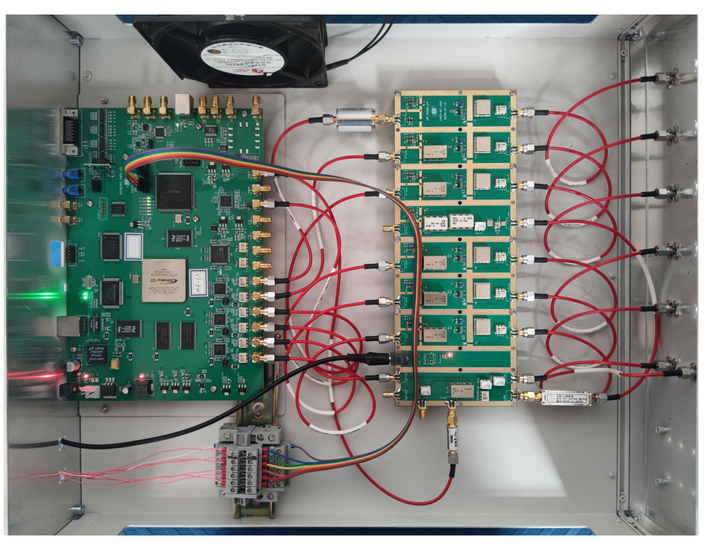
Booster	
Frequency	499.8 MHz
Cavity type	Normal conducting
Number of cavities	6
Storage ring	
Frequency	166.6 MHz
Cavity type	Superconducting
Number of cavities	5
Frequency	499.8 MHz
Cavity type	Superconducting
Number of cavities	2

2. RF system at HEPS

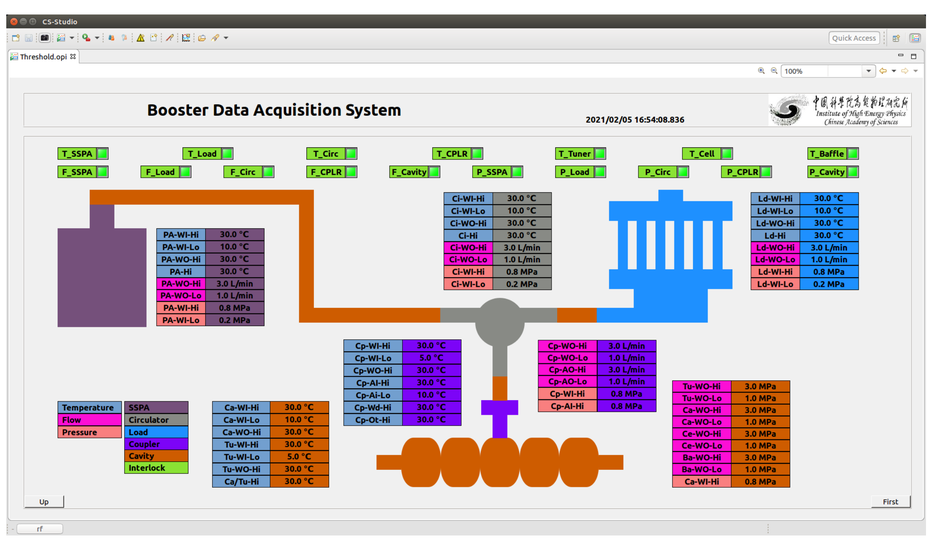


3. Data acquisition system

Slow signal acquisition system



RF signal acquisition system



Operator interface

4. Interlock system

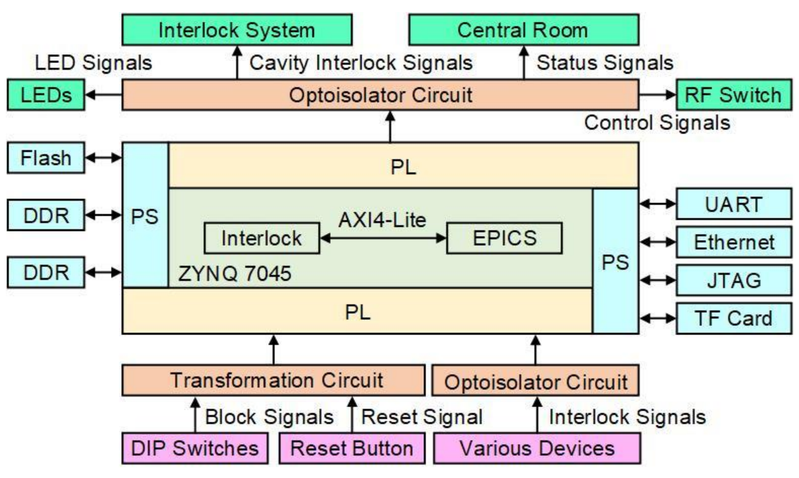
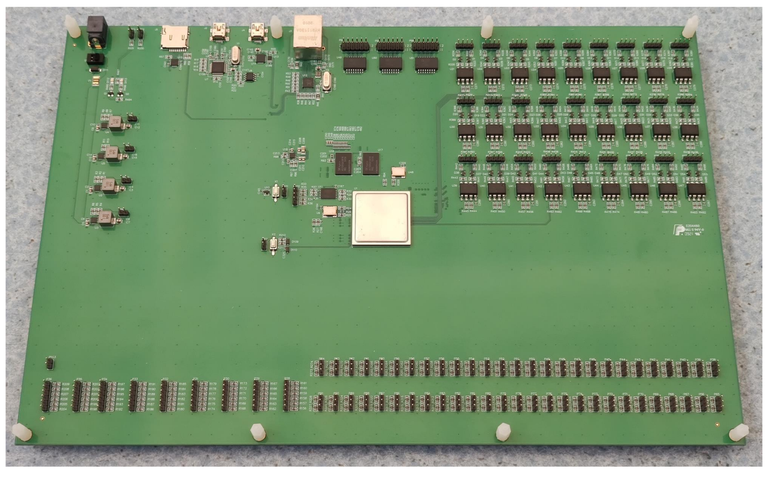


Diagram of the designed interlock board



Picture of the interlock board

Final remarks

The development of the data acquisition system was accomplished. Each data can be collected normally.

The design and fabrication of the first edition interlock board was accomplished. The first test of the interlock board was completed, and some problem was solved.

The control system based on the EPICS was completed, all data can be displayed and stored as expected.