WEPAB322

Status of Digital BPM Signal Processor for SHINE

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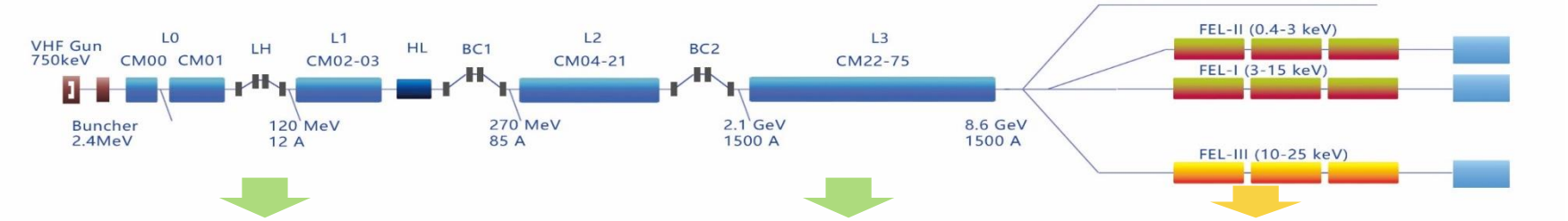
BPM system for SHINE

- SHINE is a 3km long hard x-ray FEL facility locates at Shanghai. The beam repetition rate is 1MHz.
- BPM electronics including independent RF front-end module. Developing common Digital BPM Signal Processor for all BPM types.
- The relative resolution of the processor should better than 0.10%.

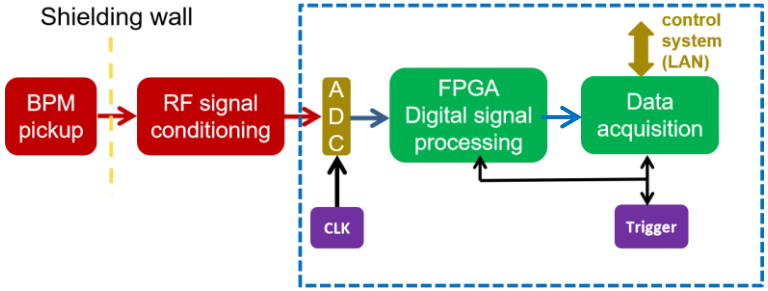


Injector, Chicane
Stripline BPM
Res.: 10 μm@100 pC;
100 μm@10 pC

LINAC
Cold-BPM
Res.: 50 μm@100 pC;
200 μm@10 pC

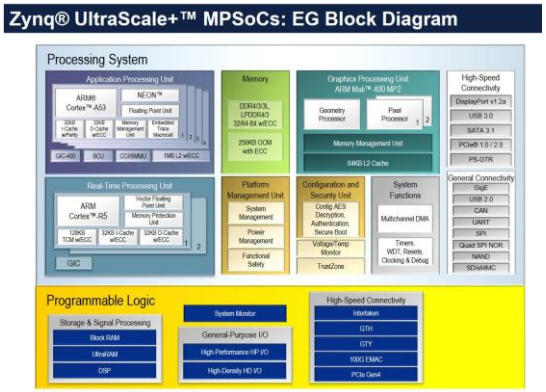
Distributor, FEL
Cavity BPM
Res.: 200 nm@100 pC;
10 μm@10 pC

Development plan



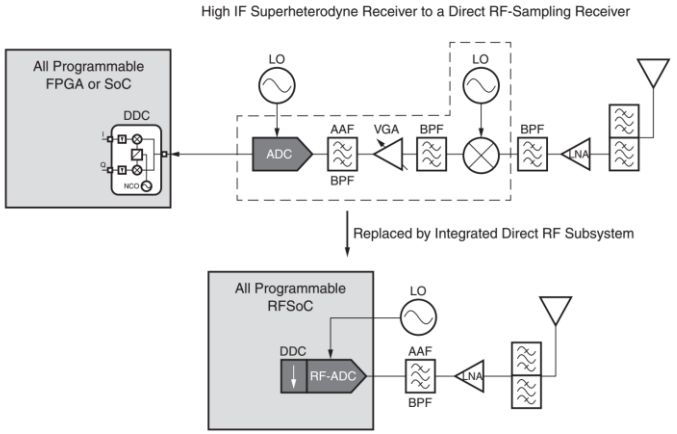
Digital BPM Signal Processor

- 1U height, seperated ADC board and FPGA board connected through FMC connector. WRN FMC.
- MPSoC FPGA(including hard Arm core) applied for compact design.



Two types are developed

- 1, Intermediate Frequency(IF) processor: sampling rate higher than 500MHz, 4 channels ADC bits ≥ 12, band width > 500MHz. Domestic and abroad ADCs are applied.
- 2,Direct-RF sampling processor for C band caivity BPM: sampling higher than 1.5GHz, 4 channels ADC bits ≥ 12, band width > 6GHz



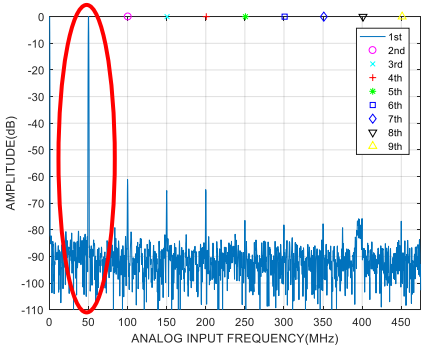
Direct RF sampling

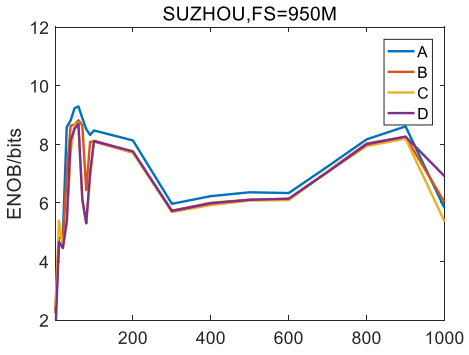
SHINE

Lab evaluation of IF ADC

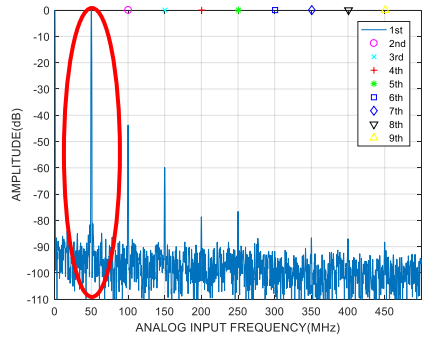
- Domestic ADCs and abroad ADCs are used for performance evaluation and comparison. FPGA platform is ZCU102 Ultrascale+ MPSoC evaluation board.
- The signal source test results shows the their performance are comparable.

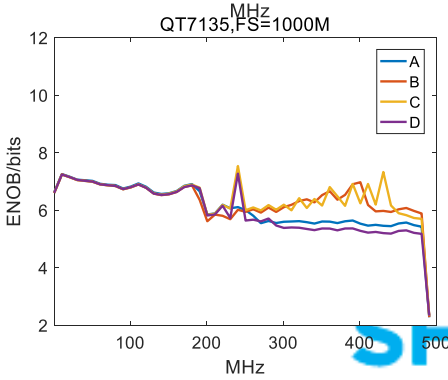
Domestic ADC boards





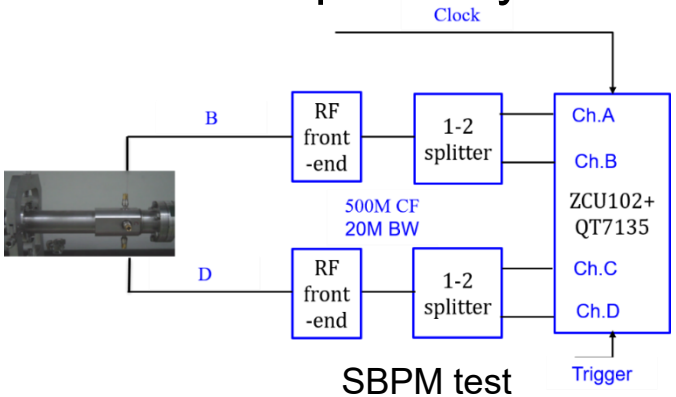
Abroad ADC boards



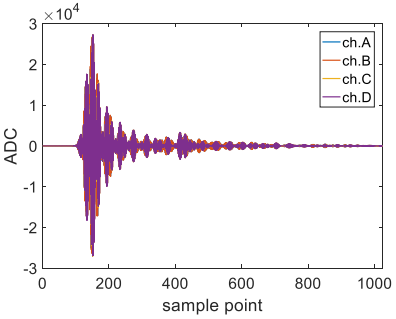


SXFEL beam tests of IF ADC

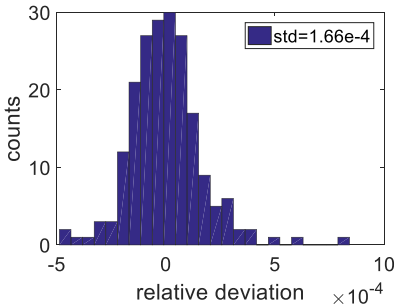
- The relative resolution evaluation of the IF processor is carried on SXFEL stripline BPM and cavity BPM.
- The relative resolution of SBPM and CBPM test is 0.016% and 0.029% respectively.



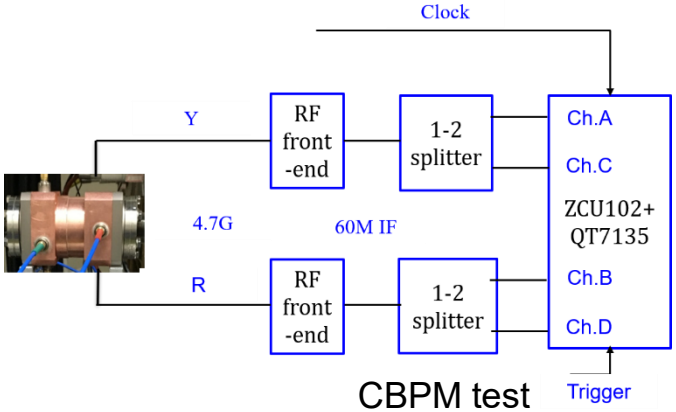
SBPM test



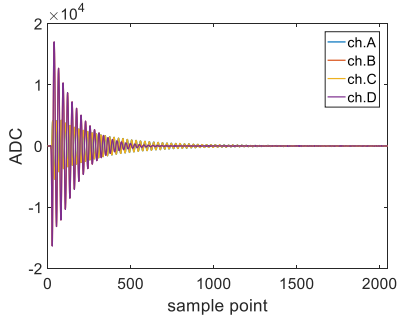
SBPM fs=952MHz



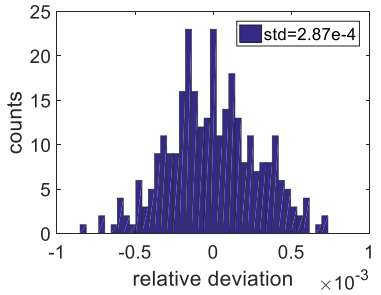
relative RMS



CBPM test



CBPM fs=952MHz

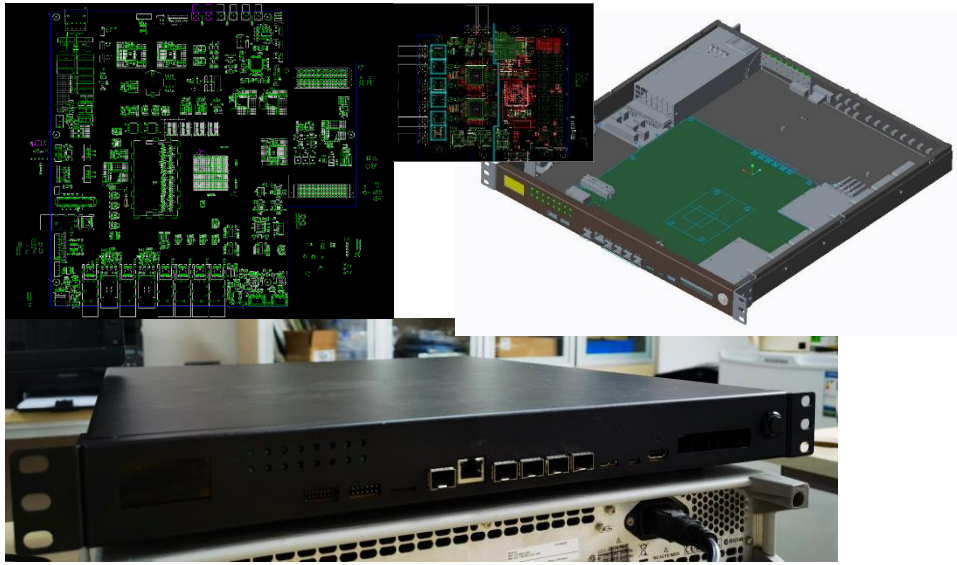


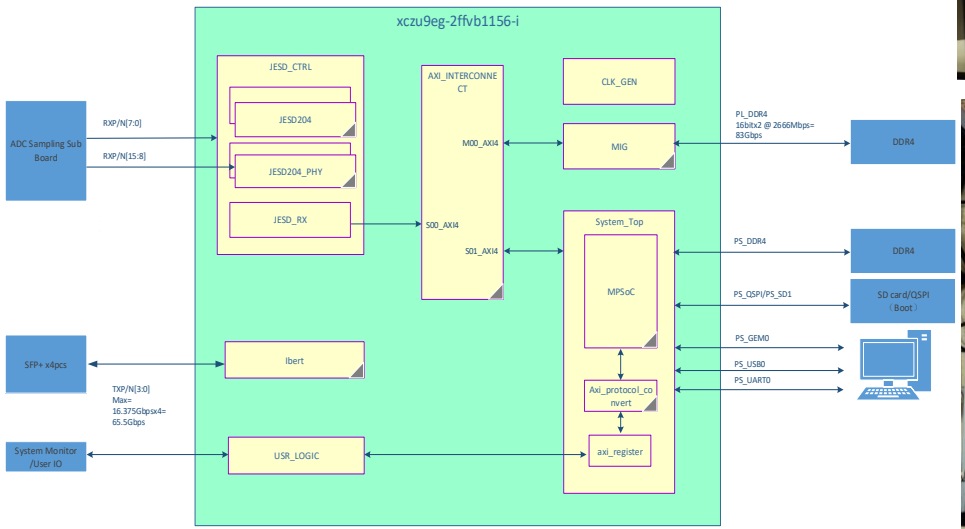
relative RMS

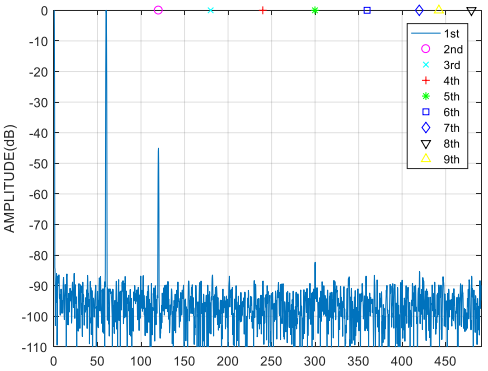
SHINE

New designed IF processor

- A new IF processor is developed.
- Zynq Ultrascale+ MPSoC FPGA, 4*1GHz ADC, 1 FMC for WRN, 4*SFP, Ethernet, interlock, trigger, clock, GPIO...



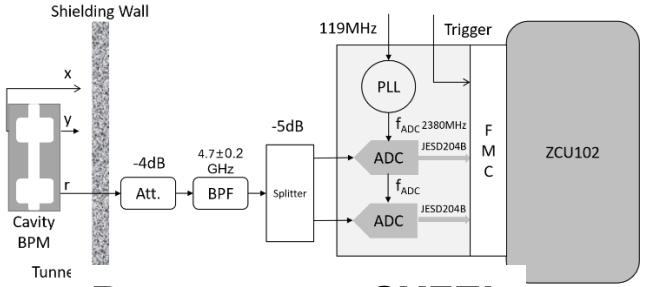




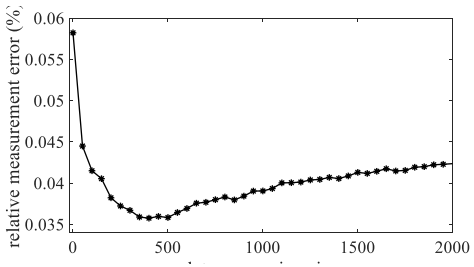
60MHz signal source

Direct RF sampling processor

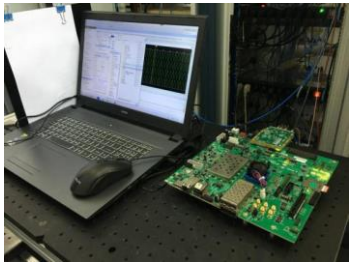
- A 2 channels direct RF sampling ADC FMC board is used for CBPM signal processing evaluation. The bandwidth is 8GHz and maximum sampling rate is 3.2 GSPS. The relative resolution is better than 0.040%.
- An dedicated RF processor is under development and almost done.

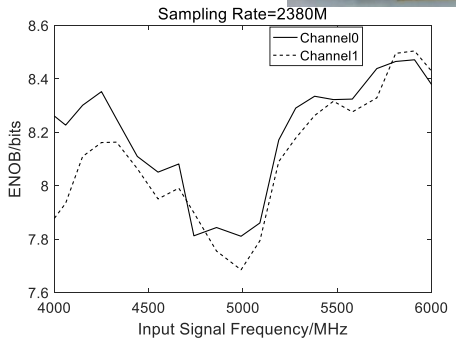


Beam test on SXFEL

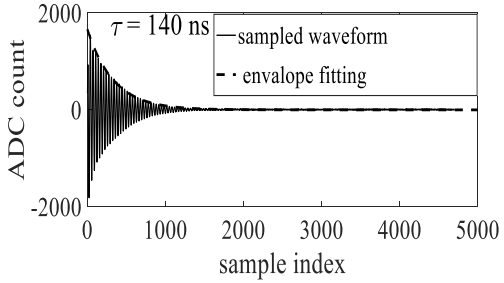


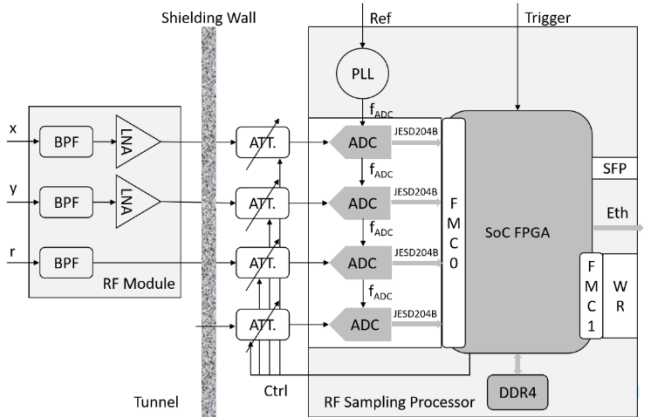
Relative resolution





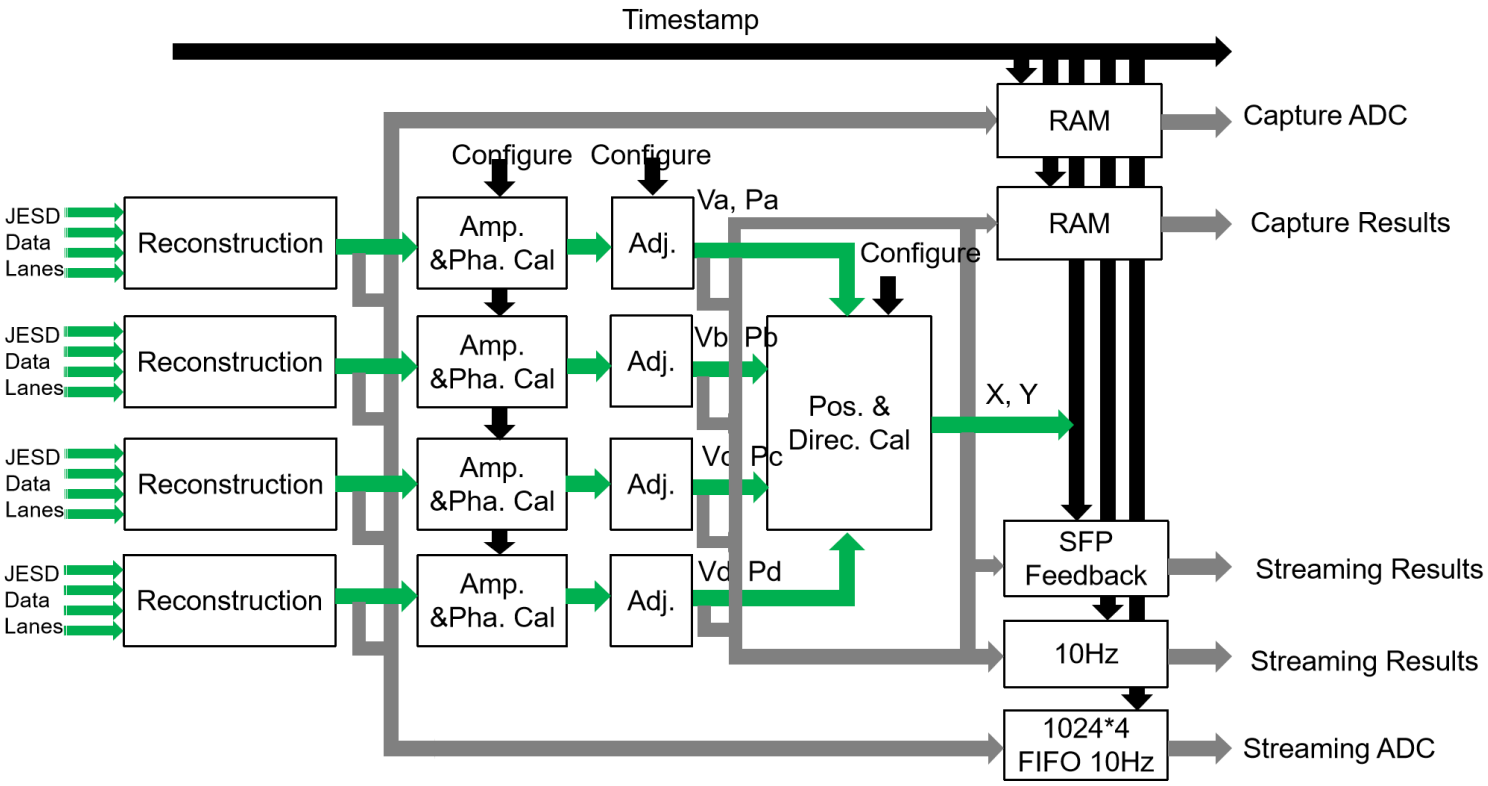
ENBO





Dedicated RF processor

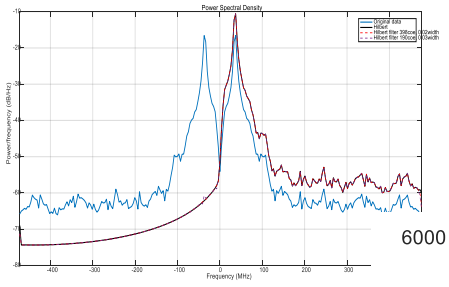
Digital signal processing in FPGA



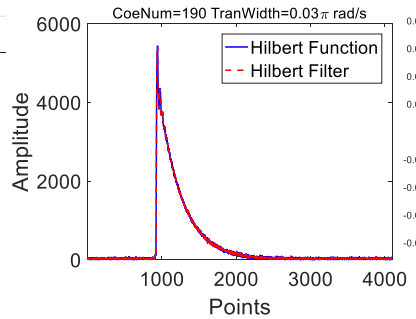
SHINE

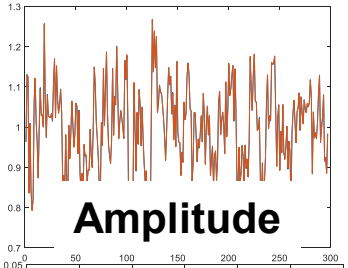
Hilbert computation in FPGA

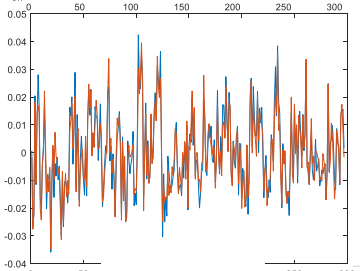
- Spectrum analyzing(FFT) is always used in the cavity BPM signal processing. FFT computing is time-consuming and resource-intensive in FPGAs and does not meet the 1MHz repetition rate in SHINE.
- Hilbert transform can be used to get the envelop and phase of the cavity BPM signal. But it is complexing and not suitable for FPGA implementation. Fortunately, Hilbert filter can be used to approximating Hilbert transform with reasonable number of taps.
- Pipeline structure can be used in filter design. Results can be get at each clock period after system latency. 1MHz rate calculation is entirely possible.



Comparison between FFT and Hilber filter







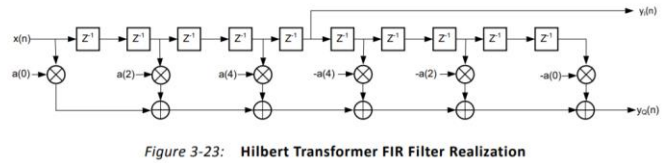


Figure 3-23: **Hilbert Transformer FIR Filter Realization**

Figure 3-24 shows the architecture for a Hilbert transformer that exploits both the zero-valued and the negative symmetry characteristics of the impulse response.

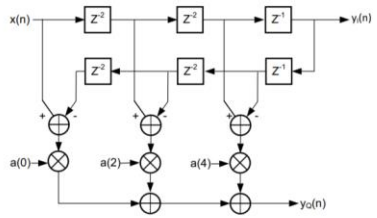


Figure 3-24: Hilbe... Negative Symmetry

Pipeline structure

Summary

- Two types of processor prototypes are developed for SHINE, including IF processor and direct RF sampling processor.
- Domestic and abroad 1GSPS ADCs are evaluated in lab and SXFEL. Both relative resolution is better than 0.1%(SBPM 0.016%, CBPM 0.029%). New designed IF processor is ready.
- The relative resolution of direct RF sampling ADC is better than 0.040%, and can be used for CBPM RF signal sampling. The development of a new direct RF processor is almost done.
- Digital beam signal processing algorithm is studied. Hilbert filter can be used for 1MHz beam repetition rate calculation.