Tuned Delay Unit for a Stochastic Cooling System at NICA Project

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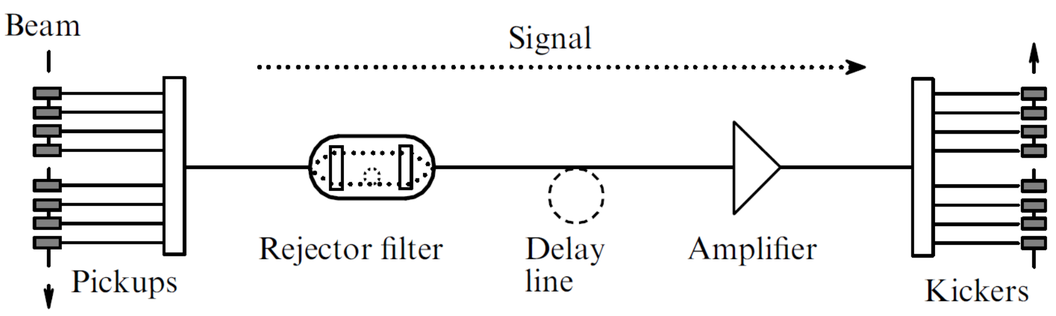
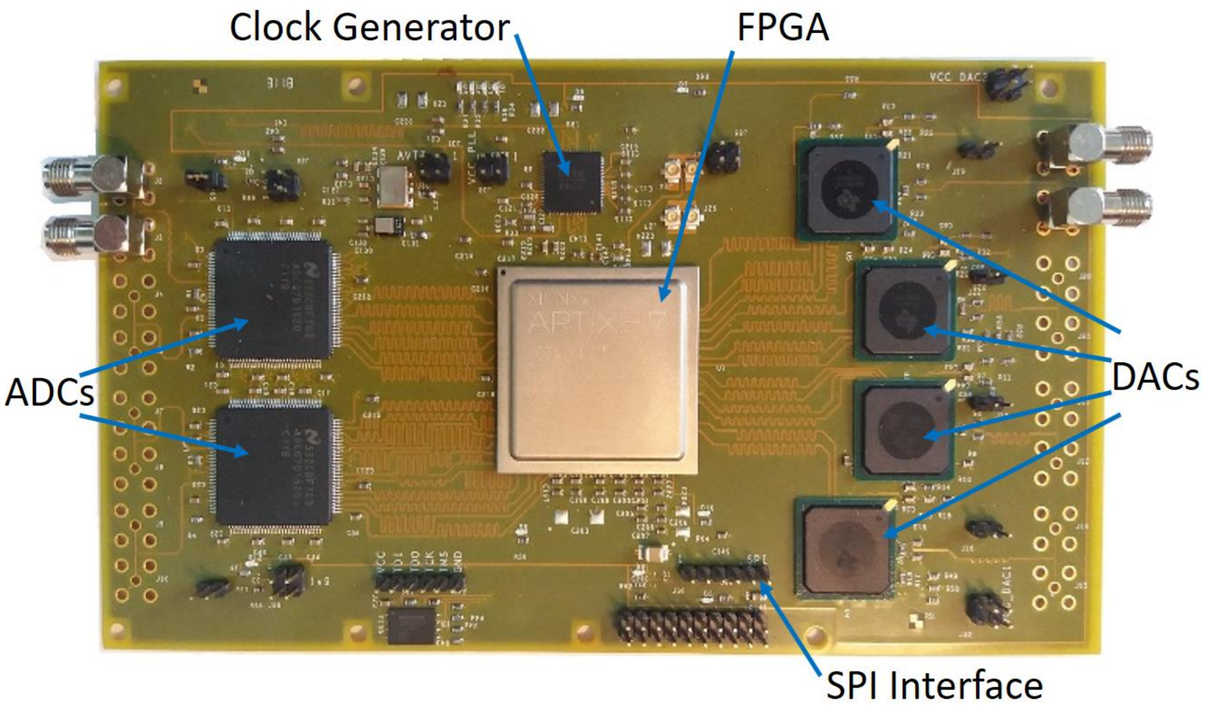
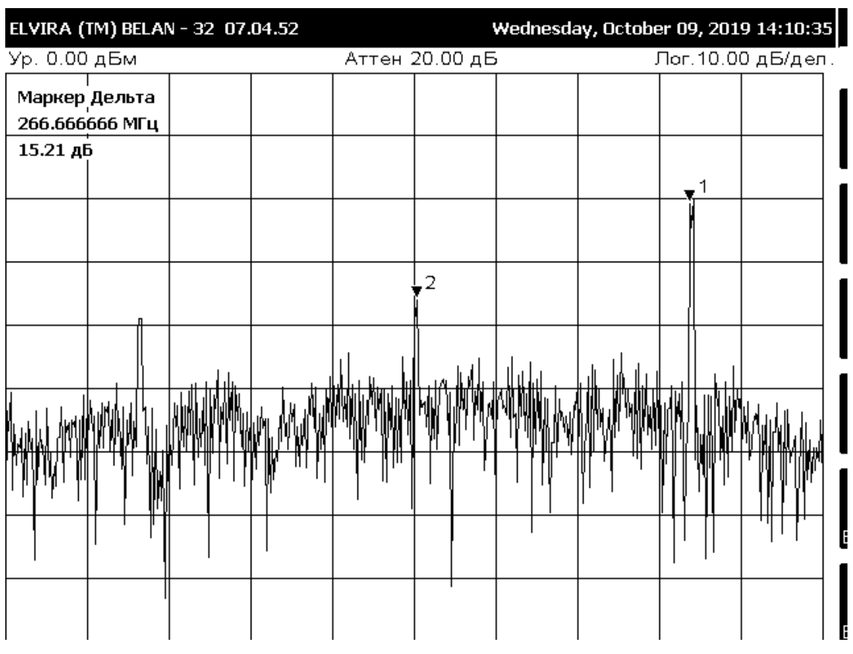


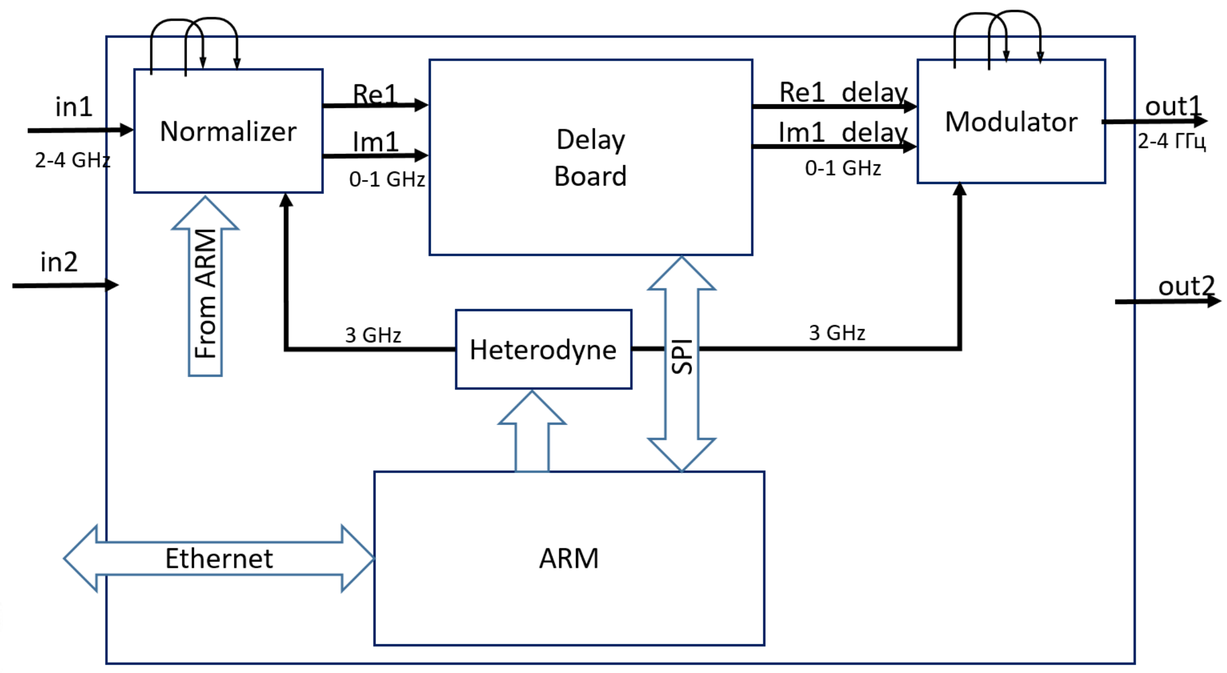
The digital delay unit consists of: a signal normalizer, which contains 3-stage 60 dB wide range amplifier, an attenuator of 0÷31 dB, additional 20 dB amplifier and a quadrature demodulator-based downconverter; a digital delay module with two 2-channel ADCs, an FPGA, four DACs and a HMC7044 dual-loop clock frequency generator; and quadrature modulator, which produce output signal with required frequency range.
Additional infrastructure modules of the unit are: 2-channel 3 GHz heterodyne generator; 12 channel power supply; and a microcontroller board, which is used as an interface and configuration module of the unit.



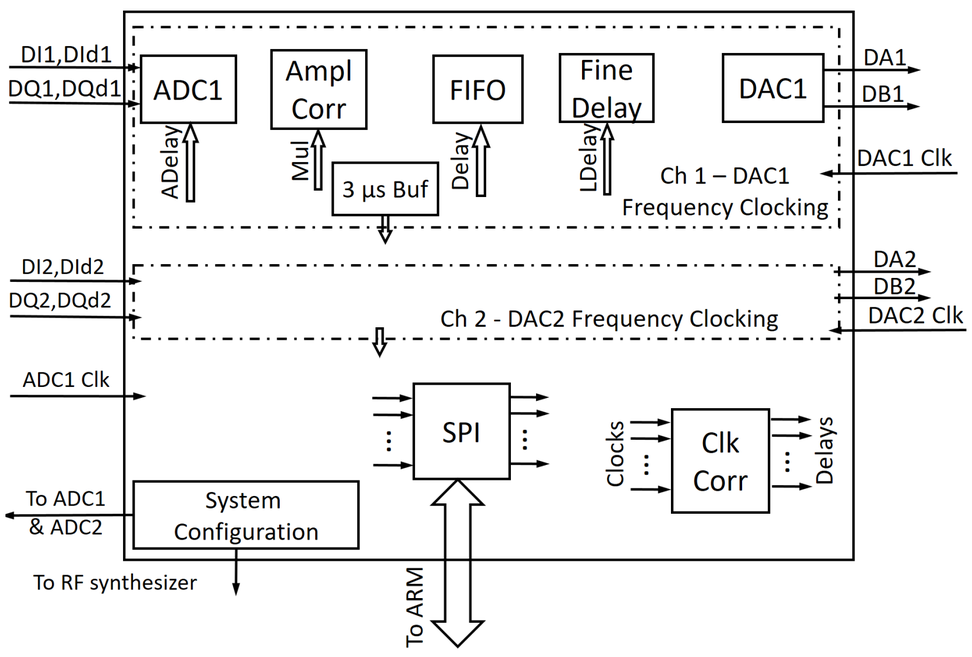
Test sequence produced with PC-based control program. That include: the delay of the output sinusoidal signal with a constant frequency, the amplitude-frequency, phase-frequency, and step response of the delay line, the group delay of the module, as well as the spectra of the sinusoidal signal from an external generator were measured. Final on-table test optimize worked signal amplitude related to a certain set of intermodulation spectral components on full frequency range.



Stochastic cooling is one of the crucial NICA (Nuclotron-based Ion Collider fAcility) subsystems. This system requires fine tuning of the response delay to the kicker, for both longitudinal and transverse stochastic cooling systems. The use of a digital delay line allows to add additional features such as a frequency dependent group velocity correction.
At the first stage of research, it was decided to implement stochastic cooling in the longitudinal phase space by mean of the notch filter method, as it is the least critical to the quality of the accelerator tuning.



For the prototype, the operating mode with the maxi-mum possible bandwidth with 2.4 GSPS sampling rate is selected. In this mode, each ADC transmits a digitized signal over four 7-bit data buses clocked at 300 MHz. Within FPGA, this traffic is packed into an 8x7-bit frame clocked at 300 MHz frequency, normalize signal amplitudes, stored in 3 μs buffer, 2-stage delayed with ~52 ps step, and output to the DACs over two 14-bit buses at 600 MHz. A separate task in the FPGA module is to automatically adjust the phase of clock signals to various modules involved in the wiring of the digitized ADC signals.



The digital implementation of the delay module allows us to add a phase response correction. Basically, the constant phase response of an RF line can be corrected by measuring the phase response of the delay line and generating a phase-correcting FIR or IIR filter. Later, the phase response can be adjusted automatically.