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DIGITAL LOW LEVEL RADIO FREQUENCY SYSTEM FOR THE BOOSTER RING OF THE TAIWAN PHOTON SOURCE

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Abstract

The purpose of a Low-Level Radio Frequency (LLRF) system is to control the accelerating cavity field amplitude and phase. For the Taiwan Photon Source (TPS) at NSRRC, the currently operating LLRF systems are based on analog technology. To have better RF field stability, precise control and high noise reduction, a digital LLRF control systems based on Field Programmable Gate Arrays (FPGA) was developed. We replaced the analog LLRF system with the digital version for the TPS booster ring at the beginning of 2018, and we will replace those in the storage rings in the future. Test results and operational performance of the TPS booster DLLRF system are reported here.

INTRODUCTION

The Taiwan Photon Source (TPS) at NSRRC is a third generation light source operating at 3 GeV electron energy [1]. The TPS Low Level Radio Frequency (LLRF) system, whose purpose is to control the amplitude and phase of the field in the accelerating cavity, is presently based on analog technology [2]. To have better RF field stability, precise control and high noise reduction, a digital LLRF (DLLRF) control system based on Field Programmable Gate Arrays (FPGA) was developed. The RMS errors in the DLLRF prototype controller for the accelerating voltage amplitude and phase can be contained within about 0.2% and 0.2 degree, respectively. The sidebands of the 60 Hz noise and its harmonics can be suppressed down to -70 dBc as well [3]. We replaced the analog LLRF system with this digital version for the TPS booster ring on February 2018 and enjoyed successful operation. The analog LLRF systems of the storage rings will be replaced in the future.

The detail of the design, the implementation and test results of the DLLRF prototype controller including its IO interface can be found in [3-5]. The hardware architecture, test results and operation performance of the DLLRF system for the booster ring of the TPS are reported in the following sections.

HARDWARE ARCHITECTURE

The LLRF system consists of three feedback loops for the TPS booster ring: the amplitude, the phase and the tuner loop. The interlock protection function is included in the LLRF system as well. In the analog design, all of these functions are controlled by a Programmable Logic Controller (PLC). The current design of the DLLRF system, includes only functions of amplitude and phase control. To keep the tuner loop and the interlock protection system, the PLC is still contained in the DLLRF system. We only replaced the modules in the RF path for the digital system, as shown in the Fig. 1. Tuner loop and interlock protection will be included in the DLLRF controller later.

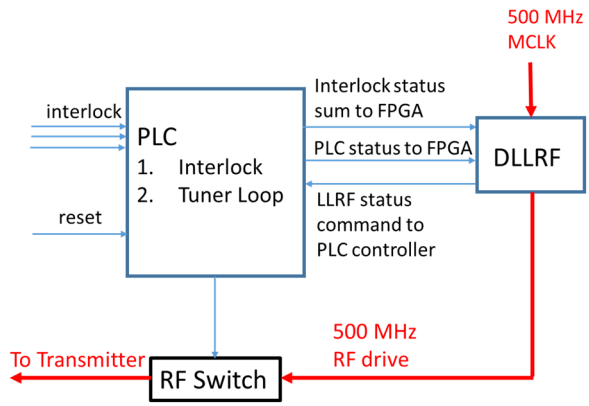

Figure 1: Hardware architecture of the DLLRF system.

There are three modes for the operation: off mode (RF off), tune mode (feedback off) and operation mode (feedback on). The DLLRF controller receives commands from local or remote users and its operation status would be send to the PLC. The operation status of the PLC switch is based on these commands from the DLLRF controller and then sent by control signals to the tuner control module for the tuner loop. The operation status of the PLC is monitored by the DLLRF controller. The status of the DLLRF controller changes according to the PLC status as well, because the PLC may have its status changed unexpectedly such as due to a tuner scan fault. The PLC receives the interlock signals and then activates a RF switch based on these signals. There is an interlock sum signal to the DLLRF controller, which would switch the status of DLLRF controller to the off mode.

A Raspberry Pi (RPi) [6] is chosen for the IO controller of the DLLRF system and utilizes GPIO pins for communications with the FPGA [4]. Application programs can be developed with python and remote operation, data acquisition and monitoring can be implemented through the EPICS package [7, 8] easily. During 90 days long term test with uninterrupted communications, the RPi IO controller works well. It shows that the RPi has good reliability and stability as an IO controller for the DLLRF system. Figure 2 shows photos of the DLLRF system with an RPi IO controller inside the DLLRF controller and its display would show up on the monitor. The clock needed for the DLLRF is generated by a frequency standard module [3]. The cavity simulator is for the functional test of the DLLRF controller. All modules are integrated into a 19-inch cabinet rack.

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BASIC FUNCTION

Figure 3 shows the booster RF graphical user interface (GUI) for the local operation. To be an easy and simple user-friendly interface, only the basic functions and indicators are shown on the panel. All additional functions such as the ramping waveform generator, cavity voltage calibration, PI control gain adjustment and transient data recorder can be called from the menu bar. In addition, the function of energy savings which has been realized in the analog LLRF system [9] is implemented in the TPS booster DLLRF system as well. It can save about 78% of the electric power consumption for the RF system in the Taiwan Light Source [10]. Test results of these functionalities are given in the following.

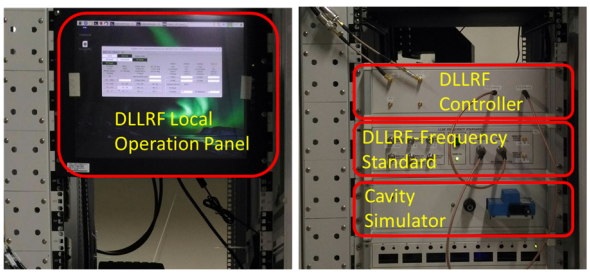

Figure 2: Photos of the DLLRF system. Upper (left) and bottom (right) layers of the rack.

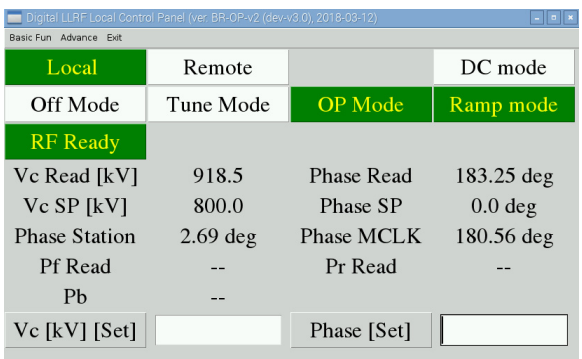

Figure 3: The booster RF GUI for the local operation.

The raw input signal for the cavity amplitude is in terms of ADC counts and needs to be converted into the real cavity voltage. A third order polynomial fitting is performed to the conversion curve, as shown in the Fig. 4. The relationship between the read value in the DLLRF GUI and the real cavity voltage becomes linear. The PI gains are tuned by a function, based on a feed forward table, that can add an arbitrary waveform to the output signal. The optimal PI gain is selected according to the behaviour of the cavity voltage signal with a pulse waveform added in the operation mode. Figure 5 shows the cavity field spectrum at the operation mode with cavity voltage of 950 kV before and after the DLLRF system installed. The PI gain is optimized. The sidebands of the 60 Hz noise and its harmonics can be improved by about 20 dB with DLLRF system.

The TPS booster injection repetition rate is 3 Hz. To generate the ramping waveform, a 1024-point ramping table is written into Random Access Memories (RAMs) in the FPGA via an IO controller. The corresponding time interval for these 1024 points is 1/3 second. The set points of the cavity voltage are changed to fit the ramping waveform in a particular ramping mode. Figure 6 shows the cavity voltage amplitude and phase during routine operation of the TPS booster RF measured by the analog and digital LLRF systems. The difference between set points and measured values during routine operation for the DLLRF can be controlled within 0.32 ± 0.52 % and 0.01 ± 0.13 degrees for the cavity voltage amplitude and phase, respectively.

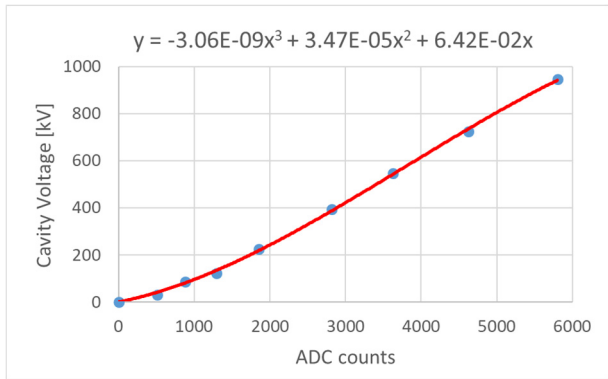

Figure 4: A 3th order polynomial fit for the cavity voltage calibration.

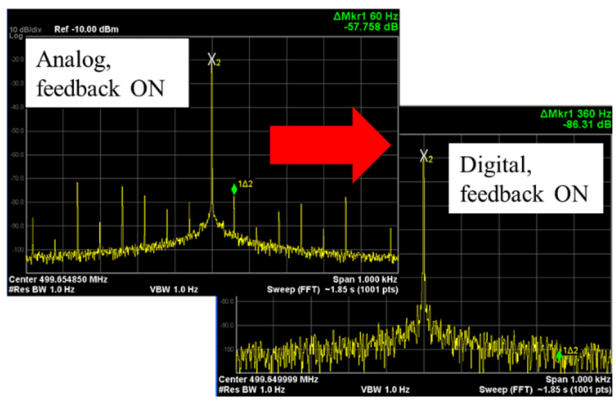

Figure 5: The cavity field spectrum at the operation mode with cavity voltage of 950 kV before (left) and after the DLLRF system (right) installed.

Energy savings of the booster RF system are realized by controlling the klystron cathode current and cavity voltage according to the injection timing signal [9]. In the energy savings mode, the klystron cathode current and the cavity voltage are operated at the lowest values. When the injection timing signals occur, the RF system is switched to injection mode and the klystron cathode current increases to provide about 40 kW output RF power while the cavity voltage starts to ramp. To have a stable operation, the timing for the klystron cathode current increases and the cavity voltage ramping proceeds as follow: when the injection timing signal occurs, the klystron cathode current rises up at the first 3 Hz clock while the cavity voltage starts to ramp at the second 3 Hz clock. The klystron cathode current is controlled by an energy savings module and the

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ramping is controlled by the DLLRF controller, both of them monitoring the same 3 Hz clock and the injection timing signal. Figure 7 shows the related signals in the DLLRF controller recorded from the transient data recorder for the energy savings function using test signals. During the test all timing signals worked as designed.

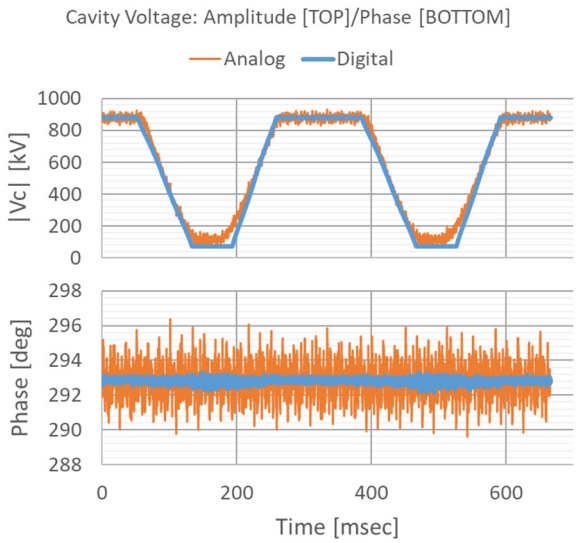

Figure 6: Cavity voltage amplitude and phase during routine operations of the TPS booster RF measured by the analog and digital LLRF systems.

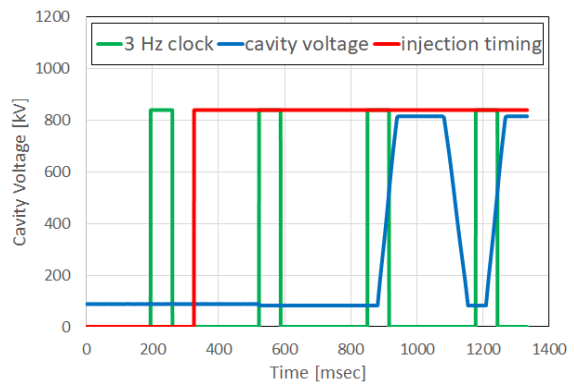

Figure 7: Related signals as obtained from the transient data recorder in the energy savings mode using a test signal.

ADVANCED FUNCTION

An advanced function of a dynamic signal analyser (DSA) is developed in the DLLRF controller, and its design details and the test results can be found in [5]. A small amplitude modulation signal is added to the output signal of the DLLRF controller, and then the variation of the amplitude and phase of the input signal for the DLLRF controller is detected. Therefore, the frequency response of the device can be measured. This measurement can be performed in either tune or operation mode. Figure 8 shows the DSA measurement of the TPS booster RF in the tune mode, which corresponds to the open loop transfer function for all components on the RF path except for the controller itself. The ability of noise suppression for different frequencies can be measured quickly by performing the DSA measurement in operation mode.

To have a better understanding of the performance of the DLLRF controller and its effects on the stability of the RF system under beam loading, a model for the interaction between the LLRF loops and the beam-cavity system can be used [11]. The parameters of the LLRF control loops are necessary in this model. An approach to measure the closed loop transfer function has been implemented into the DLLRF controller as well. Combining with the results from DSA measurements, one can obtain the parameters of the transfer function for the DLLRF controller. The function of the stability analyser will be implemented in the DLLRF controllers used for the storage rings in the future.

CONCLUSION

A DLLRF controller with better RF field stability, precise control and high noise reduction has been developed at the NSRRC. The analog LLRF system for the TPS booster ring was replaced by this DLLRF system in February 2018. All functions including cavity voltage ramping and energy savings were tested. The operation of the TPS booster ring with the DLLRF system is successful and the present storage ring analog LLRF systems will be replaced in the future.

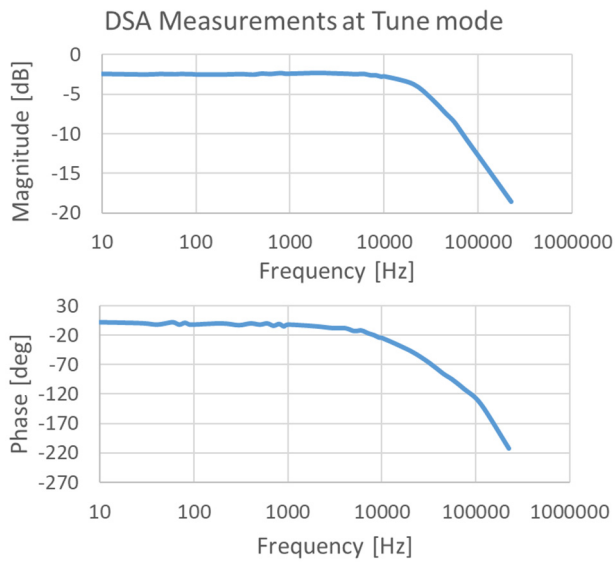

Figure 8: DSA measurements of the TPS booster RF in tune mode with a cavity voltage of 650 kV.

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