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RF INTERLOCK IMPLEMENTATION USING DIGITAL LLRF SYSTEM FOR 100 MeV PROTON LINAC AT KOMAC*

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Abstract

KOMAC (Korea Multi-purpose Accelerator Complex) already has operated 100 MeV proton linear accelerator with high availability since 2013. This accelerator is com-posed of Ion source, LEBT, RFQ and DTL systems to transport proton particles to the target. Total 9 klystrons with 1.6 MW peak power and 10% duty cycle are used to provide the controlled high power RF to the accelerator cavities with 350 MHz of operating frequency. These klys-trons are driven by LLRF systems that the LLRF systems should control the RF and protect the amplifiers and cavi-ties from the abnormal RF. In this article, the RF interlock using cavity pickup signal introduced. When the cavity pickup amplitude breaks away from the adjustable upper or lower limit window, the digital LLRF system interrupts the LLRF output. These implementations were conducted by upgrading the FPGA (Field Programmable Gate Array) logics of the existing digital LLRF system.

INTRODUCTION

The Low-Level RF (LLRF) control system of KOMAC 100 MeV proton linear accelerator already applied digital board to control the 350 MHz frequency RF [1, 2]. Figure 1 shows simplified block diagram of this LLRF system. The LLRF system drives the Solid State Amplifier (SSA) which is preamplifier of 1.6 MW klystron. So that, 1.6 MW, 350 MHz RF forward power is inserted to the RFQ and DTL cavity and the 350 MHz pickup signal of these cavities returns to the LLRF system for controlling the RF. Thereby, the RF in the cavity can be controlled less than 1 % error of the amplitude and phase.

Because 1.6 MW RF power is high that the RF interlock is critical issue to accomplish high availability of the RF station and accelerator. For protecting the accelerator cav-ities and RF systems including the klystrons, circulators and the RF windows, the initial analogue RF interlock board was developed and applied as shown in the Ref. [2].

This analogue RF interlock board turns off the RF drive signal of SSA by turning off the RF switch in the RF ana-logue box when the local arc detector detects the arcing that comes from the klystron window, circulator and the RF window. Also, excessive reverse power that comes from the cavity was interlocked in the analogue RF interlock board by calculating the Voltage Standing Wave Ratio (VSWR).

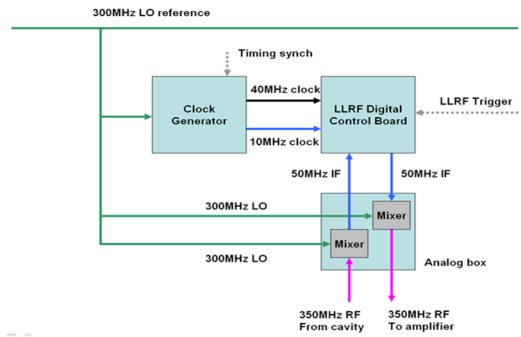

Figure 1: 100 MeV LLRF block diagram.

Although existing analogue RF interlock board works well and has significance in our linac, we need more flexible platform and method were composed of the digital component. For that, the cavity pickup RF was used to protect the cavity and RF systems because the digital LLRF system already monitors and controls the cavity pickup RF through the FPGA.

For turning off the cavity pickup RF when abnormal RF detected, the pickup RF should be monitored and compared with predefined interlock levels as shown in the Fig. 2. For monitoring and comparing the pickup RF, the amplitude of pickup RF was calculated instead of using the In-phase, Quadrature (I, Q) values as it is because the RF phase scanning procedure may occurs when the accelerator needs the phase tuning. Also, the I or Q values may be very small when the pickup RF phase is 0 degree or ±180 degree, so that the accelerator operator cannot define the RF interlock levels exactly. For these reasons, the amplitude of cavity pickup RF was used for monitoring and interlocking.

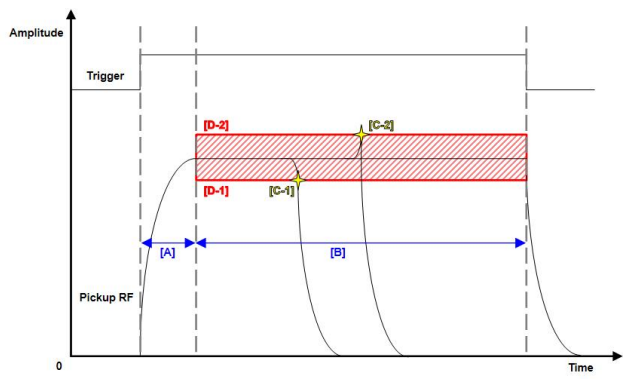

Figure 2: Abnormal pickup RF interlocked (A: cavity filing time, B: interlock activated time zone, C-1, 2: interlock latched when the amplitude breaks away from the lower or upper limit, D-1, 2: defined lower and upper limits).

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INTERLOCK LOGICS OVERVIEW

To apply the digital RF interlock using the digital LLRF system, the additional FPGA logics were upgraded. The Fig. 3 shows how can the digital LLRF turn off the pickup RF signal with the FPGA. The each part of logics introduced below.

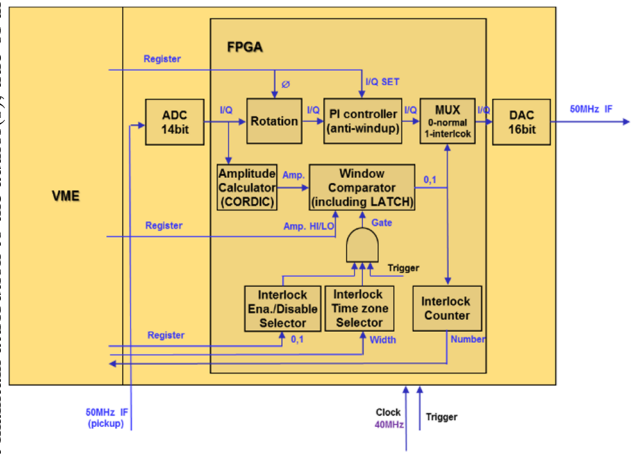

Figure 3: Digital RF interlock logics in the FPGA.

Monitoring the Amplitude of Pickup RF

The I, Q values were already monitored by the FPGA for controlling the pickup RF with the PI controller. For calculating the amplitude of this pickup RF signal, the I and Q values are transferred to the CORDIC IP core. After getting the amplitude, this value transferred to the window comparator for comparing with the predefined high and low interlock levels.

Defining the Interlock Activated Time Zone

As shown in Fig. 2, the cavity pickup RF has the rising time. To avoid from this rising time, the interlock activated time zone starts after the rising time from the changing point of the trigger signal. The rising time is defined by counting the number of the clock rising edge. This counting number is proportionate to the rising time. Also, the RF interlock activated time zone finishes when the trigger changed to low. However, this time zone is activated only when the interlock enable status is high.

Comparing with Predefined Interlock Levels

The window comparator compares the amplitude of the pickup RF with the high and low interlock levels which is defined by the operator through the register. When the amplitude is larger than the high interlock level, the comparator transfers the interlock flag to the blocking switch. In the same way, when the amplitude is smaller than the low interlock level, the comparator also transfers the interlock flag to this switch.

However, the critical point is that the RF interlock should be latched in pulse when the interlock flag status is changed. So that, the additional damage on the cavity and the RF system can be suspended in the same pulse duration. Also, before the next trigger, the RF interlock should be reset automatically for enabling the high power RF.

Interlock Counting and Alarming

For alarming the RF interlock status to the operators in the control room, the digital LLRF system interworks with the EPICS alarm system through the VME platform. The RF interlock alarming was done by adding the LLRF alarm window to the existing 100 MeV linac machine alarming system [3]. In addition, the interlock flag is counted by the counter for the operator to know how many times the RF interlock happens for protecting the cavity and RF system.

DIGITAL RF INTERLOCK TEST

Test Setup

To test the performance of digital RF interlock logic, the test bench was configured as shown in Fig. 4. The timing system (Micro Research Finland, VME-EVR-230RF, [4]) supplies the trigger signal and 40 MHz clock signal to the digital LLRF system. And the signal generator (Agilent, N5181A) was used as a frequency source of 300 MHz LO of this RF system. The other signal generator (Agilent, N5181A) was used as a RF de-tuner operating at 350 MHz frequency. The SSA (mini circuits, TIA-1000-1R8-2) was used as a DAC output signal's amplifier to supply sufficient 350 MHz RF power to the dummy cavity which has 3120 unloaded Q-factor.

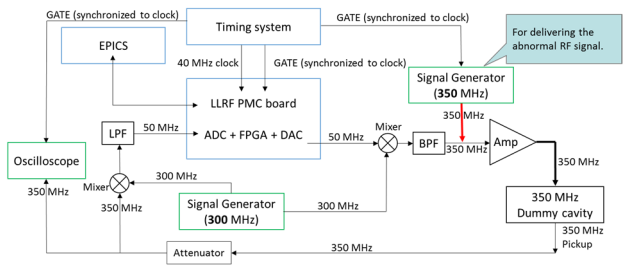

Figure 4: Test bench for testing the RF interlock logic.

Performance of the Digital RF Interlock Logic

To verify the digital RF interlock's performance, the test was conducted by detuning the 350 MHz RF signal using the signal generator as shown in Fig. 4. The upper picture of Fig. 5 shows that the RF interlock was disabled even though the pickup RF was detuned in the cavity. By contrast, the lower picture of Fig. 5 shows that the pickup RF was turned off when the detuning field was detected. This test confirms that 1us of detuning field width can be interlocked by the digital RF interlock logic.

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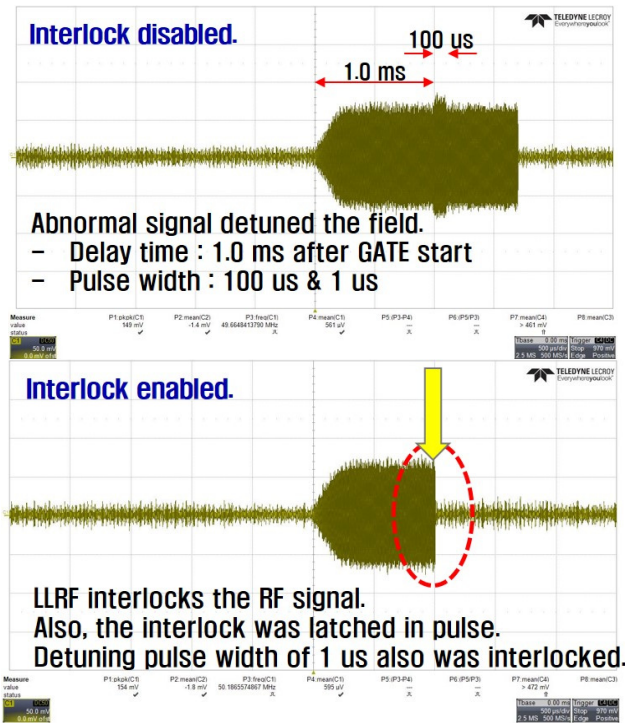

Figure 5: Test result of digital RF interlock logic. (upper) RF interlock disabled. (lower) RF interlock enabled.

FUTURE WORKS

For alarming the RF interlock status to the operator, this must be linked to the existing 100 MeV linac machine alarming system. By so doing, the more detailed strategies can be applied to the circumstances where the alarm system should sounds the warning. When the interlock flag is generated intermittently, the alarm sound should not work. To implement this concept, the interlock flag must be stored in the array or the buffer in the FPGA. As a future work, this logic will be implemented in the FPGA and the RF interlock alarming system will sound at various conditions set by the engineer or operator.

CONCLUSION

The digital RF interlock logic was uploaded to the existing digital LLRF FPGA of the 100 MeV proton linac. So that, all 9 klystrons can be driven by the interlock upgraded digital LLRF system. As a result, the accelerator cavities and RF systems can be protected from the high power RF. In addition, the operator can recognize the RF interlock status and quickly defines the interlock levels through the user friendly EPICS interface.

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