ISBN: 978-3-95450-184-7 doi:10.18429/JACoW-IPAC2018-WEPAF073

ULTRA-WIDEBAND TRANSVERSE INTRA-BUNCH FEEDBACK: BEGINNING DEVELOPMENT OF A NEXT GENERATION 8GSa/s SYSTEM

J. E. Dusatko†, J. D. Fox, SLAC National Accelerator Laboratory, Menlo Park, California, USA

Abstract

Building on the success of our 4GSa/s wideband transverse feedback system, we have begun development of a next generation ultra-wideband feedback processor which doubles the effective sampling rate to 8GSa/s. This higher sampling rate and proportional increase in analog bandwidth enable enhanced flexibility and diagnostics for accelerator transverse feedback such as control of higher-order modes, more detailed diagnostic information, improved SNR and two channel processing of total charge and orbit signals, with multiple pickups. Though targeted for ongoing transverse intra-bunch instability studies at the CERN SPS with a 1.7ns bunch length, the increased performance paves the way for instability control and diagnostics applications for other machines such as the HL-LHC and FCC. This paper discusses the beginning development process including an evaluation of the highest speed AtoD and DtoA data converter devices at time of this writing and selection of the devices used in our design. It then describes the architecture of the full 8GSa/s prototype feedback processor and the design approach, which involves using both custom and commercial components enabling rapid and flexible development.

INTRODUCTION

We have previously constructed and successfully operated a 4 GSa/a wideband transverse intrabunch feedback instability control system [1...4]. This system has demonstrated control of modes 0…2 TMCI and electron cloud induced intra-bunch instability oscillations at the CERN SPS. The high sampling rate is required in order to extract vertical particle motion from within the 1.7ns long SPS proton bunch at injection. Running at a slightly lower rate of 3.2GSa/s for simplified timing synchronization with the SPS, as well as the practical bandwidth of the 500MHz stripline kickers, the system takes 16 samples across the bunch, providing a 5ns sample window. High speed, wide bandwidth data converters, coupled with an FPGA-based reconfigurable digital signal processor, and RF analog front- and back-ends, offer a very flexible solution for accelerator bunch feedback and diagnostics.

MOTIVATION

Increasing the effective sampling rate increases the bandwidth of information that can be obtained from the bunch and that driven onto the beam. While greater bandwidth is necessary to sense high intra-bunch modes, this increased sampling can also provide increased dynamic resolution of bunch motion for diagnostic and control purposes. This further enables us to do things such as measure and control higher order oscillation modes, and observe more detailed beam behaviour. In addition, the higher sampling rate allows us to operate on shorter bunch lengths in machines such as the LHC and FCC. As an added advantage, the increased sampling rate gives a higher signal-to-noise ratio (SNR) within a fixed operating bandwidth.

DESIGN APPROACH

We seek to first rapidly develop a proof-of-concept prototype. Similar to our previous system, we choose to use a mixture of commercial and custom components. Purchasing what we can and building the remainder provides a cost-effective and expedient solution. For the data converters, a full or semi-custom ASIC is not considered due to time, budget and resource constraints. Therefore, commercial solutions were sought, and candidate devices were identified, selected and evaluated. The design evolved around the data converters. At the time of evalua-tion, no mainstream manufacturer was offering an 8GSa/s ADC solution; therefore time-interleaving multiple lowe sampling rate ADCs is used. Beyond the data converters and signal processor are the analog front- (AFE) and back-ends (ABE) which are required to have wide band-width and low noise to preserve the system SNR and dynamic range (8- to 10-bits is useful for our system). The AFE and ABE designs are not discussed in this work.

COMPONENT SELECTION

The major subsystem components (ADC, DAC, FPGA board) were selected, with an eye towards performance requirements and ease of prototyping.

DAC Selection

Our system requires a Digital-to-Analog Converter (DAC) with sufficient full-power bandwidth over the frequency range of interest (4GHz). A survey of available high speed DACs was performed and at that time (beyond more exotic or ASIC core offerings) only one manufacturer offered a device that matched our requirements. The Euvis, Inc. MD662H 8GSa/s, 12-bit DAC. The manufacturer claims that the part will run up to 10GSa/s [5]. Since this time, other semiconductor companies have released equivalent or even higher sampling rate devices (e.g Analog Devices AD916x/917x and TI DAC32RF8x/9x families of components) which look quite interesting. In many

* Work supported by the U.S. Department of Energy under contract DE-AC02-76SF00515, and the US-Japan Cooperative Program in High Energy Physics.
† jedu@slac.stanford.edu

ISBN: 978-3-95450-184-7 doi:10.18429/JACoW-IPAC2018-WEPAF073

of these later devices, a complete digital RF upconverter signal chain is provided which is not compatible with our needs (though some devices offer the ability to bypass these). The MD662H was selected. It offers a parallel digital interface, with an internal 4:1 multiplexer, which simplifies the interface logic design at the cost of a larger number of physical differential signal wires. Euvis offers an evaluation module in a single-wide FMC (FPGA Mez-zanine Card) format with sample FPGA code, easing development. This board is shown in Fig. 1.

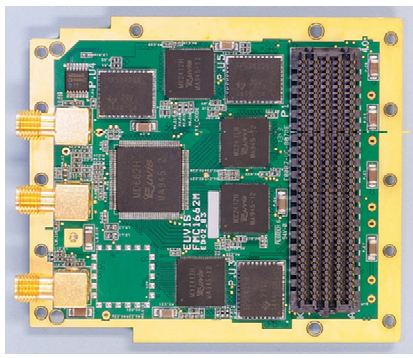

Figure 1: Euvis MD662H Eval Board.

ADC Selection

A survey of commercially available ADC devices (excluding exotic types) showed sampling rates in the realm of half of our required 8GSa/s; leading us to resort to time-interleaving methods [6] to increase the effective sampling rate. Two candidates were identified: the TI ADC12J4000 (4GSa/s, 12b) [7] and the Teledyne/e2v EV10AQ190A (5GSa/s, 10b) [8]. Both devices have a similar full power analog bandwidth of 3.2GHz.

The EV10AQ190A was selected based on its slightly higher sampling rate and the fact that it had a parallel digital interface (as opposed to the JESD204B serial interface of the ADC12J4000, which requires a large amount of FPGA logic overhead), simplifying the digital interface and interleaving synchronization logic design between the two EV10AQ190A devices. Since the time of selection, another device, the TI ADC08J3200, had been released, an 8b converter at 6.4GSa/s sampling rate and an impressive 8.1GHz full-power bandwidth. This device (operating with two interleaved) may be worth considering for a later version of our system. E2v offers a double-wide FMC ADC evaluation board with a local sampling clock synthesizer built in. The board is shown in Fig. 2.

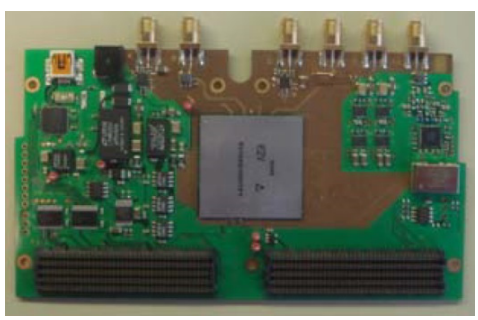

Figure 2: e2v EV10AQ190A Eval Board.

FPGA Board Selection

The choice of FPGA board is largely driven by the amount of available I/O lines. Both ADC and DAC eval boards use industry standard FMC interfaces compatible with a wide variety of FPGA boards. In selecting the particular FPGA device to use, we chose to remain with the Xilinx Virtex (and derivative generations) family since our generation system used a Virtex-6 device which had adequate performance, despite being resource limited (in DSP blocks). In addition, porting over the FPGA code is relatively seamless, aside from needing to regenerate device-specific IP cores. The FPGA board selected is the High-Tech Global (San Jose, CA) HTG-700 board [9], which contains a Virtex-7 XC7VX690T FPGA (693K logic cells, 3600 DSP slices) and three fully utilizable FMC HPC (High Pin Count) connectors. The board has a PCIe formfactor and also supports USB 2.0 and Gigabit Ethernet interfaces. The board is shown in Fig. 3.

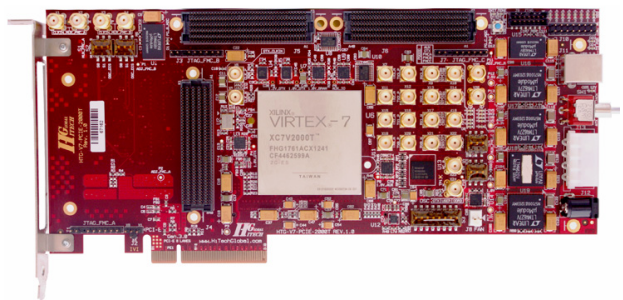

Figure 3: HTG-700 Virtex-7 FPGA Board.

The selected FPGA contains enough resources to implement feedback control for the full SPS 288 bunch LHC fill beam using the existing diagonal FIR controllers. In addition, this FPGA could also implement a model based controller on a subset of the full SPS ring [10].

Data Converter Evaluation

The fundamental tests for evaluating the data converter performance are now in process. The DAC is tested for its rise/fall and settling times as well as frequency characteristics (THD, SNR, SFDR, etc.). The ADC is evaluated using the standard tests: SFDR, ENOB, sinewave histogram, harmonic generation, etc.

8 GSa/s SYSTEM ARCHITECTURE

With the major components selected, we turn to the architecture of the overall 8 GSs/s ultrawideband feedback processor. With the data converters chosen the system has the potential of running up to 10GSa/s. A block diagram of the system topology is show in Fig. 4. The signal flow follows that of a standard digital signal processing system and the overall system can be considered yet another application of this ubiquitous technology, albeit with several application-specific features.

The two ADCs are time-interleaved via splitting and time-delaying one leg of the input by an amount equal to one half of the full sample clock period.

ISBN: 978-3-95450-184-7 doi:10.18429/JACoW-IPAC2018-WEPAF073

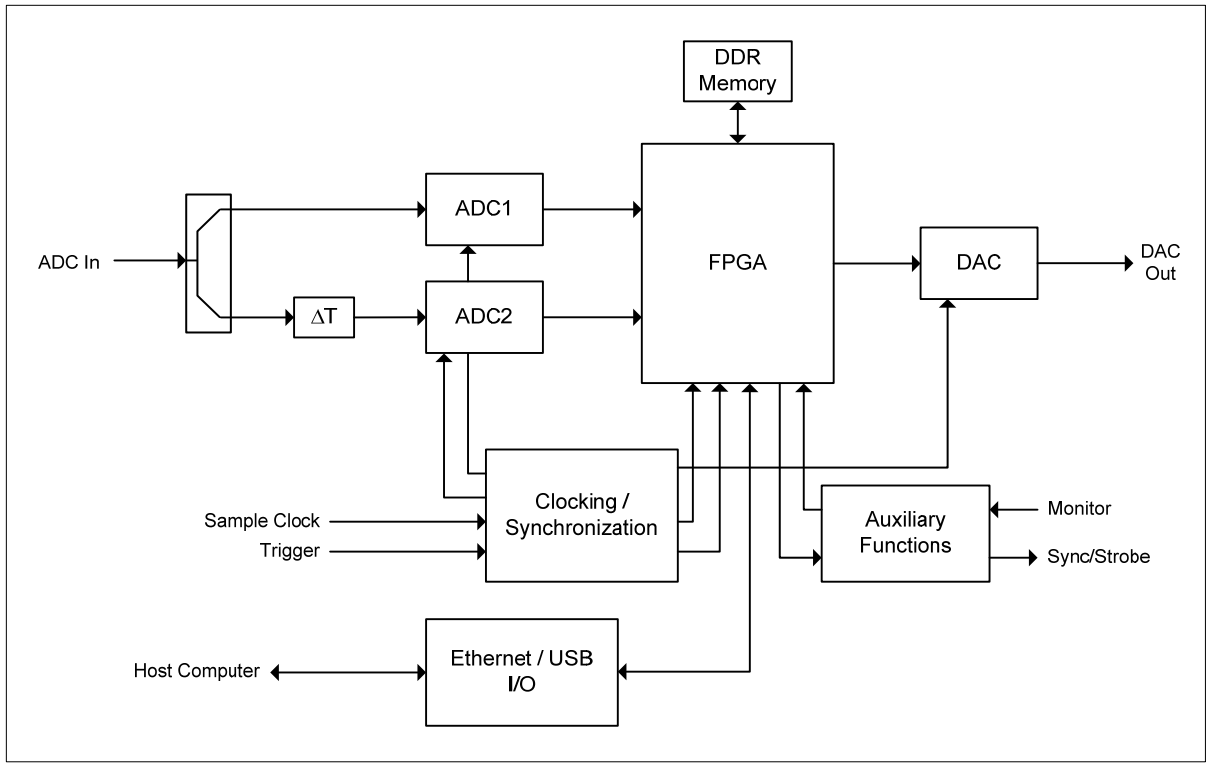

Figure 4: The Architecture of the 8GSa/s Ultrawideband Feedback Processor.

The FPGA ties everything together: handling the interfacing and data mapping between the converters, performing the signal
processing, synchronizing operations between subsystems, and implementing various support functions, overall system control and communication with the host system. The FPGA also interfaces to the on-board Double Data Rate (DDR) memory which is used for storage of ADC sample data and output waveform generation data.

The Clocking and Synchronization block handles generation and processing of the system sample clock using a PLL synthesizer (both ADC & DAC receive the sample clock at one half the sample rate, running on both clock edges), which must be very low phase noise to reduce aperture jitter. Trigger inputs are sensed using high speed comparators and resynchronized to the sample clock. This block also generates the reset synchronization signal for time-aligning the ADC data paths from each converter into the FPGA. The auxiliary functions include output synchronization and strobe signals, general-purpose digital I/O and a slow ADC (for system parameter monitoring) and DAC (for trigger comparator thresholds).

Implementation

The feedback processor will be implemented using the FPGA and data converter evaluation boards. A custom board, the ADC interface board, has been developed to connect the ADCs to the FPGA board as well as implement some of clocking/synchronization (sample clock receiver and ADC reset circuit), auxiliary functions (genera-purpose digital I/O) and the Ethernet interface. A separate custom board, the auxiliary support board, will connect to the ADC interface board and implement all of the remaining support functions (slow ADC, DAC, trigger comparators, etc.).

STATUS

The selected ADC, DAC and FPGA board components have been purchased and received. Dynamic performance evaluation of the ADC and DAC devices has begun, using the same evaluation boards that will become part of the final prototype system design. The ADC interface board has been designed, fabricated and assembled.

Remaining work includes development of the auxiliary support board, development of the clocking and synchronization subsystem, and integration and bring-up of components and subsystems. Development of the FPGA code, which involves both new design and reuse (with some porting) of the previous system's code is ongoing. Finally, we will fully leverage reuse of the Visual Basic control software and offline Matlab applications developed for the first-generation system.

ACKNOWLEGEMENTS

We gratefully acknowledge the US-Japan Cooperative Program in High Energy Physics which has the recognized the importance of and has provided funding for this work, and Dr. Makoto Tobiyama of the KEK Laboratory, Tsukuba, Japan for his ongoing support and advocacy of this work.

ISBN: 978-3-95450-184-7 doi:10.18429/JACoW-IPAC2018-WEPAF073

REFERENCES

[1] J. Dusatko et.al., "The Hardware Implementation of the CERN SPS Ultrafast Feedback Processor Demonstrator" IBIC2013, Oxford, UK, paper MOPC28, pp. 124-127.

[2] J. Dusatko et.al., "The SPS Wideband Feedback Processor: A Flexible FPGA-Based Digital Signal Processing Demonstration Platform for Intra-Bunch Beam Stability Studies" IBIC2017, Grand Rapids, MI, USA, paper WE1AB1.

[3] J. D. Fox et.al., "Control of Intra-Bunch Vertical Instabilities at the SPS-Measurements and Technology Demonstration", IPAC2017, Copenhagen Denmark, paper TUPIK119.

[4] J. D. Fox et.al., "Control of Intra-Bunch Vertical Motion in the SPS with GHZ Feedback", IPAC2018, Vancouver, BC, paper WEPAL079.

[5] *MD662H High-Speed > 8Gsps MUXDAC*, Component Data sheet, Ver. 0, 9/8/08, Euvis, Inc. Simi Valley, CA, USA

[6] S. Louwsma, E. van Tuijl, B. Nauta, "Time-Interleaved Analog-to-Digital Converters", Dordrecht, Netherlands: Springer-Verlag, 2011.

[7] *ADC12J4000 12-Bit, 4-GSPS ADC With Integrated DDC*, component data sheet, SLAS989D-January 2014-Revised October 2017, Texas Instruments, Inc. Dallas, TX, USA

[8] *EV10AQ190A Low power QUAD 10-bit 1.25Gsps ADC Operating up to 5 Gsps Quadruple Analog to Digital Converter*, component data sheet, 1070B0BDC005/13, e2v Semiconductors SAS Grenoble, France

[9] Xilinx Virtex 7 V2000T Development Board http://www.hitechglobal.com/boards/virtex7_v2000t.htm

[10] O. Turgut et.al., "Identification of Intra-Bunch Transverse for Model-Based Control Purposes at CERN Super Proton Synchrotron", IPAC2016, Busan, South Korea, paper THOAA01.