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RF CONTROLS FOR HIGH-Q_L CAVITIES FOR THE LCLS-II*

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Abstract

The SLAC National Accelerator Laboratory is building LCLS-II [1], a new 4 GeV CW superconducting (SCRF) Linac as a major upgrade of the existing LCLS. The LCLS-II Low-Level Radio Frequency (LLRF) collaboration [2] is a multi-lab effort within the Department of Energy (DOE) accelerator complex. The necessity of high longitudinal beam stability of LCLS-II imposes tight amplitude and phase stability requirements on the LLRF system (up to 0.01% in amplitude and 0.01° in phase RMS) [3]. This is the first time such requirements are expected of superconducting cavities operating in continuous-wave (CW) mode. Initial measurements on the Cryomodule test stands at partner labs have shown that the early production units are able to meet the extrapolated hardware requirements to achieve such levels of performance [4]. A large effort is currently underway for system integration, Experimental Physics and Industrial Control System (EPICS) controls, transfer of knowledge from the partner labs to SLAC and the production and testing of 76 racks of LLRF equipment.

INTRODUCTION

The LCLS-II LLRF project is a multi-lab collaboration leveraging LLRF and controls expertise across the DOE accelerator complex. The end result is the production of 76 racks of LLRF equipment, loaded with Field-Programmable Gate Array (FPGA) logic to apply real-time feedback and covered with layers of software to interact with the LCLS-II EPICS control system.

The hardware design is now frozen and the production is well under way at SLAC. Gateware and software development is still in progress at the partner labs. Several test stands are currently in use to gain experience on the system in preparation for commissioning of the Linac in late 2019. The Gun and buncher LLRF systems [5] are now ready for commissioning as part of the Early Injector Commissiong (EIC) at SLAC and development will continue over the course of FY18 and FY19.

Several aspects of the LCLS-II LLRF system have been presented in previous conferences: These include the motivation behind a hardware-centric design [6], challenges related to high-precision controls of SRF cavities [7], etc.

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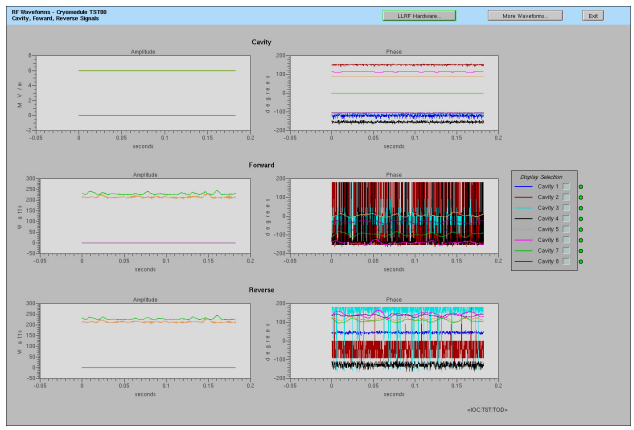

Figure 1: EPICS cryomodule-level monitoring of cavity, forward and reverse signals.

This paper focuses on the current state of affairs, in particular EPICS controls and results obtained in the cryomdoule test stands both at FNAL and JLab.

EPICS CONTROLS

All the sub-components of the LLRF system (Precision Receiver Chassis, RF Station, Resonance & Interlocks control Chassis) [2] are based on a common FPGA carrier board and share a common communication interface with the control system. Each FPGA implementation contains an in-fabric Ethernet core [8] and is connected to the LCLS-II EPICS LLRF Input-Output Controller (IOC) via optical fiber. The low-level communication protocol and the common features to all sub-components are covered by a device support driver in the EPICS IOC, on which controls applications are built to provide functions specific to each sub-component. EPICS controls are used for monitoring and configuration purposes (see Fig. 1) and all real-time features are performed purely in hardware, with dedicated point-to-point bi-directional fiber links between hardware chassis with deterministic latencies.

LLRF EPICS Architecture

The LLRF controls for a single cryomodule comprises eight LLRF chassis and one Linux CPU (see Fig. 2). The CPU is located physically near the LLRF equipment and hosts an EPICS IOC which communicates with the chassis over a dedicated fiber switch. The LLRF IOC is in turn

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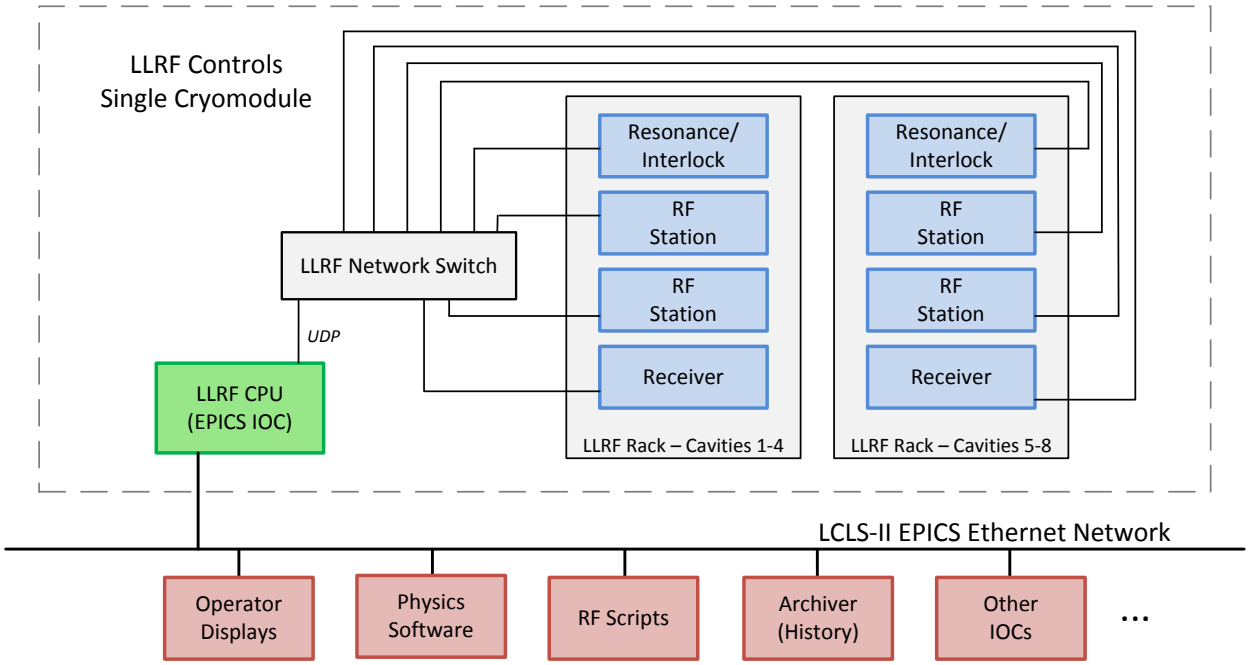

Figure 2: LCLS-II LLRF EPICS controls architecture.

connected to the rest of the LCLS-II EPICS network on a separate network interface, therefore serving as a gateway between the specialized LLRF hardware and the global EPICS control system.

Device Support

The device support driver provides FPGA register read and write access as well as extraction of waveform signals. Being agnostic to the semantics of particular registers it conserves the modularity of the IOC design. It implements the low-level UDP-based communication protocol with the hardware, socket binding and waveform handling functions while maintaining a connection state machine for each device.

The FPGA design flow includes the parsing of the Verilog modules at compile time and the extraction of the register map information from the source code itself. The register map for each FPGA build is then automatically generated and expressed in JavaScript Object Notation (JSON) format. Each register has an entry in the JSON file with attributes such as register size, data format, and the mapping of a symbolic name to the numeric address(es) used on the wire. The register map-along with other information such as the Git commit ID of the firmware build-is compressed and stored in binary format in non-volatile memory inside the FPGA. The IOC can then query the FPGA for its register map every time the communication link between the FPGA and the IOC is established. This places the register space definition centralized in the Verilog source itself and limits the amount of static configuration which must be placed in EPICS process database records to only register names.

FPGA read/write requests are inserted in the payload of the UDP packets sent to the FPGA. The IOC driver optimizes the transactions to minimize overhead by querying requests while processing of previous transactions are being processed. It also allows for several packets to be in-flight at a given moment to minimize latency. The driver then exposes the FPGA register space in the form of PVs to the IOC applications and the rest of the control system via Channel Access. Measurements of the performance of this process shows an update rate that can query signals from the FPGA and update PVs at around 90% of the Gigabit Ethernet (GbE) line rate.

RF Controls Application

The RF controls application covers the functionality specific to the RF controller. This includes signal monitoring (i.e. cavity, forward, reverse, detuning and loopback signals) and the implementation of specific functions related to the RF controls. In particular the user can perform tasks like turning the RF on and off, control the RF controller mode (individual of amplitude and phase lock and the combinations thereof), set amplitude and phase set-points, etc.

The combination of user screens and automation scripts allows for in-situ controls by operators and LLRF engineers as well as the ability to automate certain tuning processes such as the turn on a cavity from an unknown state or measuring piezo to cavity detuning transfer functions for resonance controls configuration. The automation scripts are currently implemented in Python and set a good base for the automation processes that will be used during the commissioning of the LCLS-II Linac.

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TEST STANDS AT PARTNER LABS

The cryomodule production for the LCLS-II Linac is shared between FNAL [9] and JLab. Each of them has a cryomodule test stand that the LLRF team used to gain experience of cold cavity operation using the LCLS-II system. The cryomodule prototyping and production stages started before the LCLS-II LLRF system was mature enough to be used in the cryomodule validation process. Both FNAL and JLab test stands started these processes with in-house LLRF systems. This approach has proven to optimize the cryomodule validation process at the partner labs, which could operate on known in-house equipment while the LCLS-II LLRF system attained the appropriate level of maturity. The LLRF system at FNAL working in parallel to the LCLS-II system has allowed for out-of-loop measurements of the LCLS-II LLRF performance.

The FNAL test stand has been used for all the LCLS-II LLRF testing to date(see Fig. 3) and the JLab test stand will provide a more complete framework (it has capacity for two connected cryomodules) for the next stages of the LLRF system development. This new framework is expected to start operations in the summer of 2018 and will provide the closest operational environment of LCLS-II RF controls (for both low and higher level applications) prior to commissioning of the LCLS-II Linac at SLAC.

CMTS at FNAL

The Cryomodule Test Stand (CMTS) at Fermilab allows for single cryomodule testing with a large capacity cryoplant [9]. The test stand is currently configured for 8 cavities with a 1.3 GHz drive. Future plans will use the same test cave for the 3.9 GHz cryomodule testing. The facility has been used as a testbed for RF controls and control system development, as well as for resonance control and noise suppression techniques.

Nine LCLS-II cryomodules have been tested at CMTS to date, with varying degrees of RF and cryogenic performance. The latest findings are presented at this conference [10]. The test stand has been designed and tuned for low mechanical vibrations and highly stable cryogenic flows in the test cave, allowing for precision measurements of cryomodule performance. In addition, the Fermilab RF controls allows for synchronized capture of all 8 cavities; feature that the LCLS-II LLRF system will provide when used in conjunction with the LCLS-II timing system.

LERF at JLAB

A third cryomodule test facility (Low Energy Recirculating Facility or LERF) at Jefferson Lab will allow the project to have an additional area to develop low and high level LLRF applications. The LERF will have two full cryomodules under test using production LCLS-II LLRF systems and EPICS software to commission the cryomodules. The installed hardware (includes solid state amplifiers, cryogenic and vacuum controls) and software is identical to the L1 section of the LCLS-II Linac, essentially it goes beyond a

Figure 3: Cryomodule at the Fermilab CMTF (courtesy of FNAL).

cryomodule test facility and becomes a development platform for the LCLS-II Linac. Hardware is being installed now and the first cryomodules are planned to be cooled down in July 2018. Cryomodule testing and LLRF development will begin once they are cold. Tested cryomodules will be removed and new ones installed during breaks in the CEBAF accelerator operation, about every three months. This gives the LLRF team a great place to work out control and operation issues before the actual commissioning of the LCLS-II Linac.

Test Stands at SLAC & LBNL

Test stands are also available at SLAC and LBNL. While not operating on cold cavities, crystal-based resonators provide cavity-like band-pass characteristics and serve as cavity emulators. Despite the obvious difference in Q_L with respect to the cold cavities, a lot of the firmware, software and rack-level integration developments can be tested while waiting for cold cavity time to be made available at the FNAL and JLab test stands.

The test stand at SLAC has been particularly valuable transferring ownership of the collaboration developed LLRF system to SLAC staff. These test stands have been used

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Figure 4: Fully integrated LLRF rack at the SLAC test stand.

as models for the final physical design of the system, and have enabled SLAC engineers to prepare for building and commissioning the full 76 racks needed for LCLS-II. Four racks have been built and tested at SLAC in preparation for validation at the JLAB LERF facility (see Fig. 4).

In addition, to rack hardware production, software is being developed at these test stands and validated on production LLRF hardware. Because access to the test stands is available at any time at SLAC, they have proved useful for developing control screens and higher level software in advance of validation at a full cryomodule test stand.

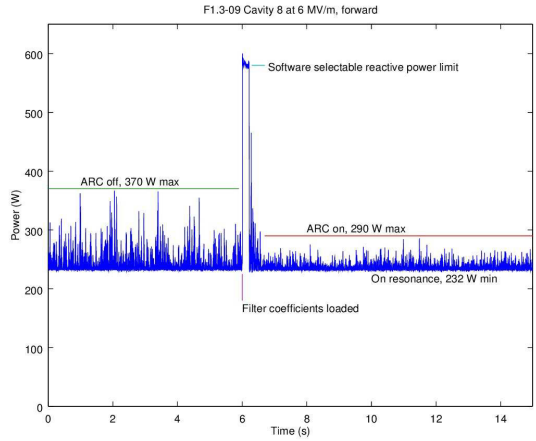

Figure 5: Reduction of reactive amplifier power after a application of Active Resonance Controls (ARC). The LLRF system provides software selection of the reactive power limit, which was achieved in the OFF-ON transition of ARC.

TEST RESULTS

The operation of eight cavities simultaneously at the design operational gradient of 16 MV/m has been achieved at the FNAL cryomodule test stand using the LCLS-II LLRF system. An automated cavity turn-on process brought up all eight cavities to gradient in a matter of minutes. The system is capable of characterizing the cavity characteristics during the automated turn-on process (this process takes about 30 seconds from an system-ignorant state and can be sped up), bring cavities up to a configurable gradient (takes around 0.5 seconds and can be slowed down), control cavity field amplitude and phase within specifications, measure cavity detuning on CW operation and use that information to close a resonance controls (see Fig. 5) loop using piezo actuators. The resonance controls system is now fully integrated with the LCLS-II LLRF system and is capable of keeping cavity detuning below the 10 Hz peak specification [10]. Tuning of the resonance controls loop relies on the piezo to detuning transfer function measurements, which is also performed using a Python-based automated process.

The LLRF system is currently also capable of several system characterization functions: measuring SSA saturation curves (see Fig. 6) and providing preliminary linearization functions (currently applying a correction factor to estimated gradient settings, live FPGA linearization is not yet implemented) and finding $8\pi/9$ mode and applying a configurable notch filter digitally in the FPGA to suppress it. Rack-level self-checks are also automated and provide information about the rack health including integrity checks on inter-chassis fiber high-speed serial links, voltage, current and temperature measurements at various locations in the FPGA and auxiliary boards, etc.

Tasks related to RF controls were fully operated using EPICS for the first time in March 2018 at the FNAL CMTS. The cavity turn-on scripts are implemented in Python and

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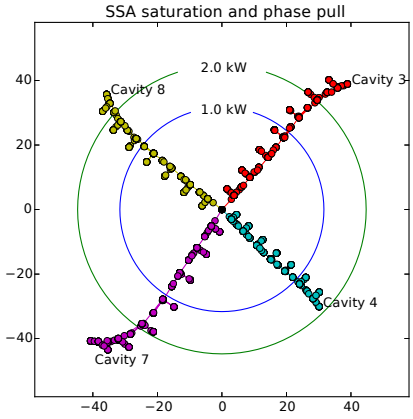

Figure 6: Solid State Amplifier (SSA) saturation curves as measured at the FNAL CMTF as part of an automated process used to characterize the RF system.

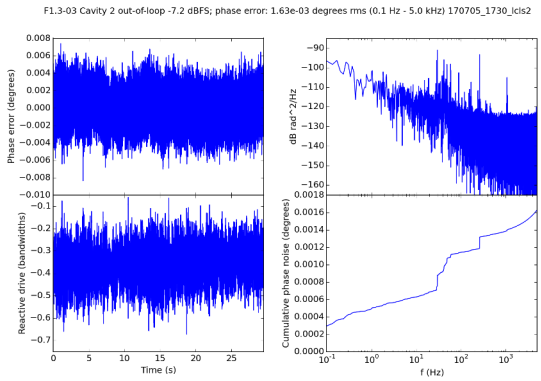

Figure 7: Out-of-loop measurements at the FNAL CMTF show a phase error of 1.63×10^{-3} degrees RMS from 0.1 Hz to 5 kHz. This result provides confidence that the hardware will provide tight field regulation in the LCLS-II tunnel, where other noise contributions will be present.

interact with the hardware through Channel Access. Start, stop and status monitoring functions of the Python scripts are provided by the EPICS drivers and are also accessible through CA.

CONCLUSIONS

Initial measurements on the Cryomodule test stands at partner labs have shown that the early production units of the LCLS-II LLRF system are able to meet the requirements to achieve tight levels of cavity stability (up to 0.01% in amplitude and 0.01° in phase), see Fig. 7. This is a multi-DOE-lab collaboration and a considerable effort is currently underway for system integration, EPICS controls, transfer of knowledge from the partner labs to SLAC and the production and testing of 76 racks of LLRF equipment.

The use of test stands at partner labs has proven to be of great benefit in order to build experience with the system and validate the hardware designs. These test stands will continue serve as a development platform. The production of 76 racks of LLRF equipment is well underway at SLAC, with a progressive development of gateware and software controls that will complete with Linac commissioning in late 2019.

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REFERENCES

[1] P. Emma, *et al.* “Linear Accelerator Design for the LCLS-II FEL Facility” in *Proceedings of FEL2014*, Basel, Switzerland

[2] C. Hovater, *et al.* “The LCLS-II LLRF System,” in *Proceeding of IPAC2015*, Richmond, VA, USA, 2015.

[3] P. Emma “LCLS-II Physics Requirement Document: Linac Requirements,” LCLSII-2.4-PR-0041-R2.

[4] C. Serrano, *et al.* “Design and Implementation of the LLRF for LCLS-II” in *Proceedings of ICALEPCS17*, Barcelona, Spain, October 2017.

[5] G. Huang, *et al.* “LCLS-II Gun/Buncher LLRF Design,” in *Proceeding of IPAC2018*, Vancouver, BC, Canada, April 2018.

[6] L. Doolittle, “Analog-centered LLRF System Design for LCLS-II,” in *Low Level RF workshop 2015*, Shanghai, China, October 2015.

[7] C. Serrano, L. Doolittle, *et al.* “LLRF Control of High Q_L Cavities for the LCLS-II,” in *Proceedings of IPAC2016*, Busan, Korea, 2016.

[8] L. Doolittle, C. Serrano “FPGA Communications based on Gigabit Ethernet”, in *Proceedings of ICALEPCS11*, Grenoble, France, October 2011.

[9] E. R. Harms *et al.* “Commissioning and first results from the Fermilab cryomodule test stand,” in *LINAC 2016*, East Lansing, MI, USA, September 2016.

[10] J. P. Holzbauer, *et al.* “Active Microphonics Compensation for LCLS-II”, in *Proceeding of IPAC2018*, Vancouver, BC, Canada, April 2018.