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PROGRESS ON 1.5 GHz MULTI-kW CW AMPLIFIER*

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Abstract

JLab upgrade program foresees new CW amplifiers operating at 1497 MHz and significantly increased efficiency vs. existing VKL-7811 klystron. One of possibilities for the replacement is usage of high electron mobility packaged GaN transistors applied in array of highly efficient amplifiers using precise in-phase, low-loss combiners-dividers. We present here performance of novel, compact 300 W pallets developed at Microsemi specifically for this project including their new GaN transistor, as well as significantly upgraded divider and combiner. Design features and challenges related to amplifier modules (pallets), broadband 21-way dividers/combiners, as well construction and assembling of the entire system are discussed including measurements.

INTRODUCTION

The original RF power system at the Thomas Jefferson National Accelerator Facility (JLab) operates at 1497 MHz frequency and consists of 340 klystrons (model VKL7811). The VKL7811 klystron upgrade proposed by CPI foresees adding a solenoid magnet and its power supply, making the system so large that it will not fit in existing locations. Inductive Output Tubes (IOT) were considered as a replacement [1]. However, IOTs are not available at 1.5 GHz, would need to be redesigned to avoid solenoid coils, and require a booster (preamp driver) as they have ~15 dB lower gain than a klystron.

Besides, a multi-kW solid state power amplifier (SSPA) could be a building block for RF power system for the Jefferson Lab Electron Ion Collider (JLEIC). Increasing the bandwidth of the system, reduction of power consumption, and overall operating efficiency will be very important for JLEIC.

SSPA SYSTEM DESIGN

The SSPA construction is shown in Fig. 1. The system architecture is a single stage variant of the previous design using 21-way divider and combiner [2,3]. The complete system consists of 22 identical power modules (pallets): one for pre-amplifier and 21 between divider and combiner.

The heart of the system is the completely new, CW-specialized ~ 300W 65010GN GaN MOSFET developed by Microsemi team specifically for this project.

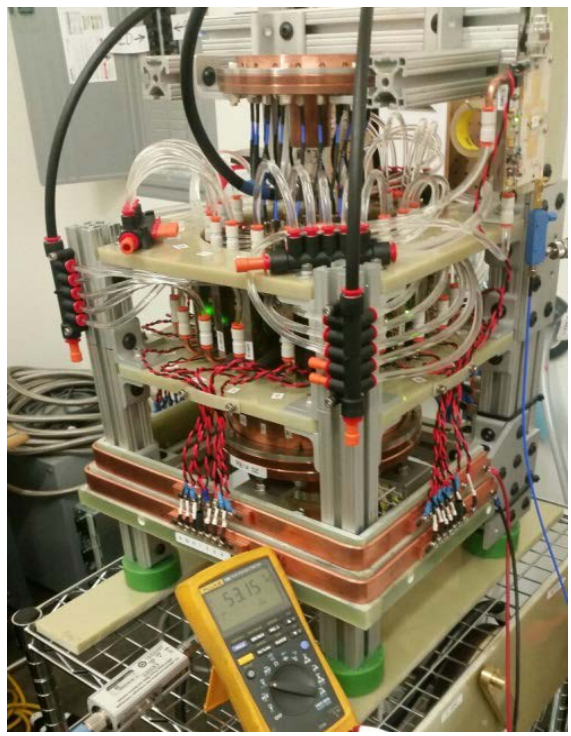

Figure 1: 6 kW SSPA system under test.

Design of the 65010GN GaN MOSFET compactly integrates thermal and RF matching. That matching has been implemented in special fabrication process developed at Microsemi. In particular that enabled significant reduction of thermal impedance vs. other power transistors we tested. The RF design of the pallet use subsequent RF matching of input and output circuitry optimized to maximize efficiency in a frequency range centred at 1.5 GHz sufficiently wide for other power saving applications. That enabled to develop a relatively compact pallet shown in Fig. 2. Note, the sequencer built into the pallet enabled to eliminate external control circuitry for gate biasing as well as protect the MOSFET by means of IGBT integrated with drain circuit and very careful selection of time delays for the turn-on and turn-off sequencing. As a matter of fact the sequencer turned the pallets into plug and play devices and significantly simplified the system architecture and operation.

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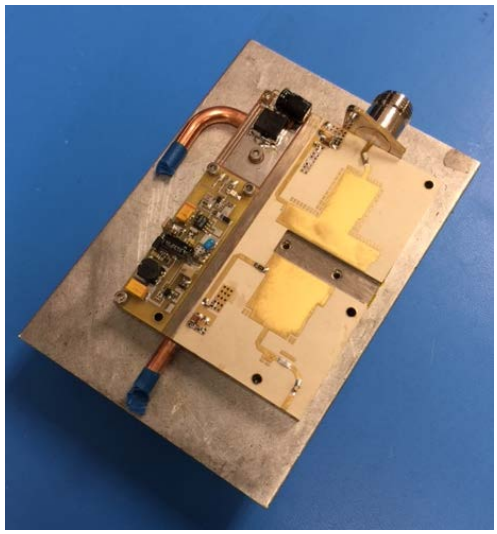

Figure 2: Photo of the 65010GNP pallet with built-in sequencer (both for gate and drain). Pallet dimensions 0.4"×3"×4".

DIVIDER AND COMBINER MEASUREMENTS

Both divider and combiner are radial reactive type. The divider was reengineered to reduce inhomogeneity for peripheral ports and reduce insertion loss.

The combiner has been completely re-designed to reduce dimensions and avoid using of any dielectrics (with exception of connectors). The "wiggling" design [4] and transmission simulation results are shown in Fig. 3. One can see the novel design is also capable of very wide bandwidth and ultralow minimal losses (lower than that in divider), which is confirmed in Fig. 4 with measurements.

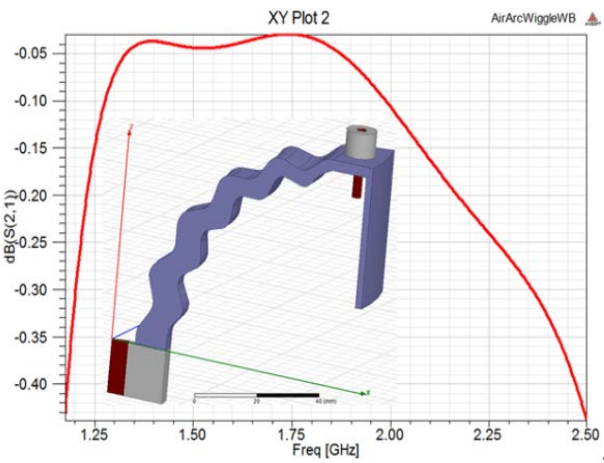

Figure 3: DC power consumption measured as a function of input RF power.

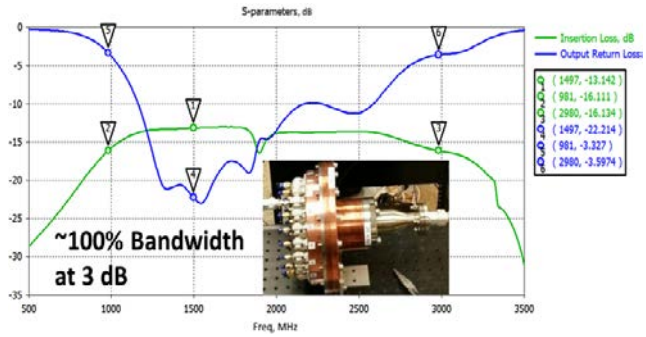

Figure 4: Insertion and return losses measured for the combiner.

The measurement results of the modified divider and novel combiner are summarized in Table 1. Combination of ultra-low losses and low way-to-way spread of transmission and phase offers low combining losses.

Table 1: Summary on Calibrated VNA Measurements at 1.497 GHz for 21-way Divider and Combiner

Device	Insertion loss, dB	Return loss, dB	Isolation, dB, Max/min	Way-to-way rms spread for power, % (phase, °)
Divider	0.082	-21	26.8/22.5	1.5(0.37)
Combiner	0.091	-22.3	24.9/10.5	1.45(0.52)

We also performed calibrated VNA measurements for back-to-back combiner-divider assembly (see Fig. 5 and Fig. 6).

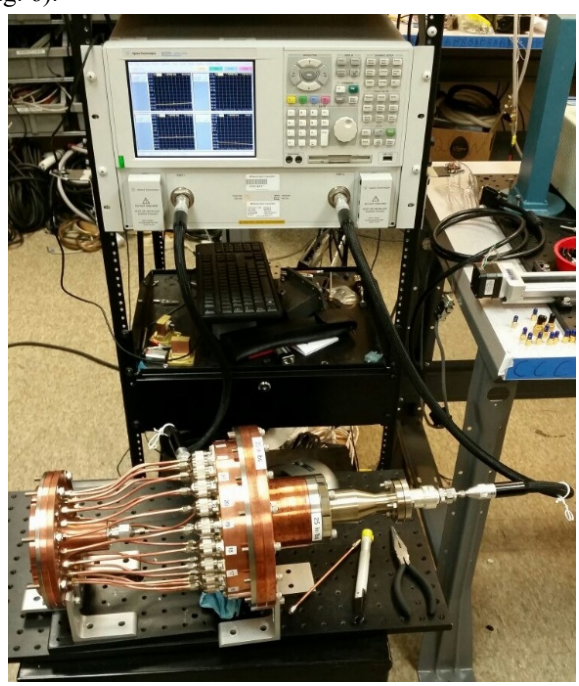

Figure 5: Back-to-back divider-combiner assembly under test.

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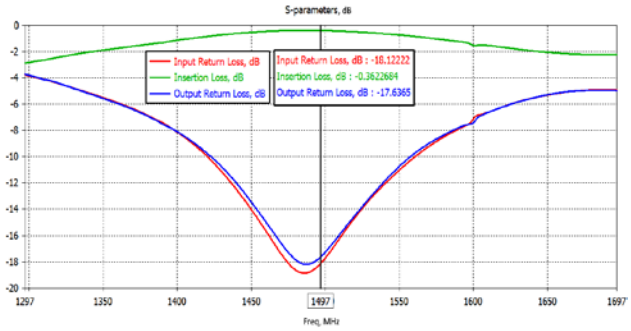

Figure 6: Broadband transmission (green) and return loss measured for the back-to-back assembly.

TESTING OF THE PALLETS AND SSPA

A demo pallet has been fabricated first and tested. High power durability tests demonstrated negligible power droop for >200W CW power, operating for days without measurable degradation in gain or power.

Twenty six pallets have been fabricated next. Every pallet has been tested at two input power levels: 37 and 38 dBm. The combined results indicate averaged power 285 W, averaged gain 17 dB, and averaged drain efficiency 63% with max range (60-66) %. Standard deviation for gain is 0.27 dB, standard deviation for output power is 18.3 W. Such narrow spreads suggest negligible loss for power combining.

Analysis of the pallet measurement results and comparison to our tests performed for other GaN transistors leads us to the following outlines:

- Best long-run CW stability and durability without failures or power droop;
- Lowest quiescent (at no RF) DC power consumption (1.1% vs. >13% for the QPD1016 Qorvo transistor with respect to saturated operation);
- One of the highest power added efficiency (PAE);
- Highest saturated CW gain (17 dB vs. ~11 dB for QPD1016).

Note the quiescent drain current ~100 mA per pallet is more than an order lower than that for COTS demo boards at comparable RF power. Such a low quiescent current indicates that a switching mode operation has been achieved. Since matching was applied to a compact layout shape seen in Fig. 2 without individual matching of higher harmonics, the particular Class of operation is mixed, i.e. a combination of Class F and others. Further studies of drain current and voltage waveforms may clarify the Class type.

RF power of the SSPA system and consumed DC power measured as a function of input power are shown in Fig. 7 and Fig. 8 respectively.

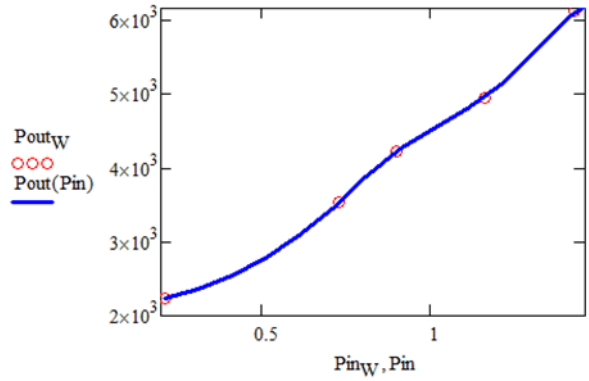

Figure 7: Output power of the SSPA system measured as a function of input RF power [W].

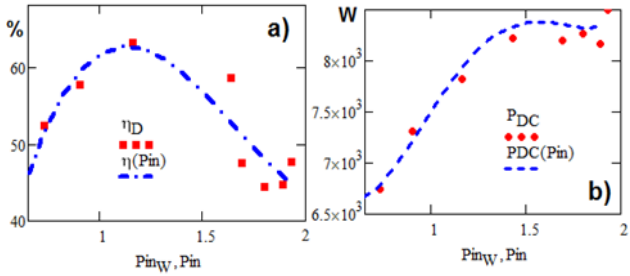

Figure 8: Drain efficiency ([%], (a)) and DC power consumption ([W], (b)) of the SSPA system measured as a function of input RF power [W].

REFERENCES

[1] R. Nelson, "JLAB Update. RF Power Systems", Thomas Jefferson National Accelerator Facility, CWRF08, Mar. 2008.

[2] A. V. Smirnov, R. Agustsson, S. Boucher, D. Gavryushkin, J. J. Hartzell, K. J. Hoyt, A. Murokh, T J. Villabona, R. Branner, K. Yuk, S. Blum, and V. Khodos, "Update on CW 8 kW 1.5 GHz Klystron Replacement", in *Proc. of North-American Particle Accelerator* Conf. *(NAPAC2016)*, Chicago, IL, USA, Oct. 2016, pp. 232-234.

[3] A. V. Smirnov, R. Agustsson, S. Boucher, D. Gavryushkin, J. J. Hartzell, K. J. Hoyt, A. Murokh, and T. J. Villabona, "GaN Class-F Power Amplifier for Klystron Replacement", in *Proc. of Intern. Part. Acc. Conf. (IPAC2016)*, Busan, Korea, Jun. 2016, pp. 583-585.

[4] A. V. Smirnov. "Compact radial combiners for broadband high power applications", *Nucl. Instr. Method in Physics Research*, A 870, 2017, pp. 55–59.