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400MHz FREQUENCY/PHASE DETECTOR AND COUNTER

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Abstract

To enhance the performance and precision of TRIUMF Low-Level RF (LLRF) system, a frequency/phase detector and counter based on FPGA is developed. The frequency/phase detector and the counter is designed as a daughter board in the LLRF control system, and is connected to the motherboard with mixed signal connectors. It sends the frequency error data to the PC through VXI databus, and provides two analog phase errors outputs. In the current design, one single unit supports four channel discriminations of RF frequencies/phases. Preliminary tests show that the phase detector has a bandwidth of 400MHz. A unique implementation of frequency discrimination was carefully carried out to ensure the resolution can reach as high as 1Hz. The phase-frequency detector has been successfully applied to the Accelerator Cryo Module (ACM) system and the requirement of the LLRF control system is satisfied. The stability and reliability of the phase-frequency detector are verified after a long-term operation.

INTRODUCTION

The LLRF system in TRIUMF is a hybrid analog/digital system, as shown in Fig. 1. It takes advantage of the modern digital signal processing technique such as DSP & FPGA and the wide bandwidth analog devices [1, 2]. The LLRF system implements three control loops: amplitude control loop, phase control loop, and tuning control loop [3, 4]. The system can run in two modes: self-excited mode and driven mode. The self-excited mode is for superconducting accelerators, while the driven mode is for debugging. The RF signal is demodulated by amplitude/phase demodulator and modulated by the I/Q modulator [5]. There are two DSPs and two FPGAs in the LLRF system. One of the DSPs reads the amplitude and the phase errors from the ADCs, calculates the amplitude and phase calibration values, and generates the IQ control vectors. The other DSP reads the phase error from the tuning phase detector and controls the tuner. One of the FPGAs is used to implement the VXI interface, which is not shown in the figure. The other FPGA, which is on the daughter board, is comprised of two phase detectors and two frequency counters, as shown in red color in Fig. 1. The work described in this paper is to upgrade the FPGA daughter board.

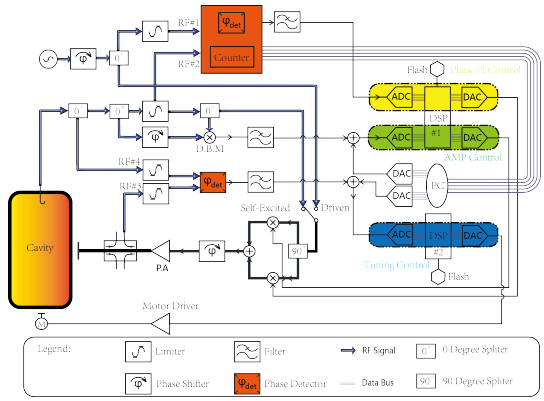

Figure 1: Diagram of LLRF system of TRIUMF.

FREQUENCY/PHASE DETECTORS AND COUNTERS IN TRIUMF LLRF SYSTEM

The startup sequence of LLRF system is: 1. Unlock the limit of the amplitude of IQ modulator to active the self-excited loop; 2. Adjust the phase shifter to change θ_l (the phase shift of the loop) and match ω_l (the frequency of the loop) to ω_c (the eigenfrequency of the cavity). The amplitude of the pickup signal would increase rapidly because of the positive feedback; 3. Close the amplitude control loop; 4. Enable the tuning loop to minimize the reverse power; 5. Adjust the tuner to change ω_c to make ω_l closer to the reference frequency; 6. After the difference between ω_l and the reference frequency is smaller than $10Hz$, close the phase control loop which will modulate θ_l to carry out closed-loop control. The loop then will oscillate at the reference frequency.

During this procedure, the PC software reads the frequency error of ω_l and ω_c from the frequency counter, sets up the tuner offset, and displays the frequency error on the GUI. One DSP inside the LLRF system reads the tuner error from the summation of the tuning phase detector and the tuning offset and carries out closed-loop tuning control. The other DSP inside the LLRF system reads the phase/frequency error of the loop frequency and reference frequency and carries out closed-loop phase control, in parallel.

HARDWARE DESIGN

The new daughter board accepts a maximum of four RF inputs and provides a maximum of four analog phase error outputs and 16-bit digital phase error output. The cycloneIII FPGA from Altera is adopted as the controller. To improve the bandwidth, the RF input signal is converted to LVPECL differential digital square waves by a high-speed comparator,

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and then converted to LVDS signals by a voltage translator to be accepted by FPGA.

To run a NiosII soft core inside the FPGA, a 32MB SDRAM is used as the RAM for the CPU, and an 8MB serial FLASH is used to store the configure information of FPGA and the software of NiosII.

The outputs of digital phase detectors inside FPGA go through active filters to generate analog outputs. A four-channel operational amplifier is used to build these filters.

All these components are mounted on a four-layer PCB board. To minimize the phase noise caused by the difference in the traces' length, all the traces of the differential digital signals and the output to the filters are the same lengths.

FIRMWARE DESIGN

The FPGA firmware is designed with Verilog and comprised of two phase detectors, frequency counters and the hardware of NiosII.

Digital Phase Detector

As described above, there are two phase detectors in the LLRF system. One is the tuning phase detector while the other one is the loop phase detector.

The output of the tuning phase detector should be proportional to the error of cavity resonation frequency and the loop frequency. The input range of the tuning phase detector should be 2π. In addition, there is no dead zone around zero output which is the tuned point. This design adopts the type 4 edge triggered phase detector as the tuning phase detector. The characteristic curve of the tuning phase detector is symmetric. The phase detection range is $-\pi$ to π, and the gain is $1/\pi$. To eliminate the dead zone, a delay circuit is added to the reset path of the flip-flop, as shown in Fig. 2.

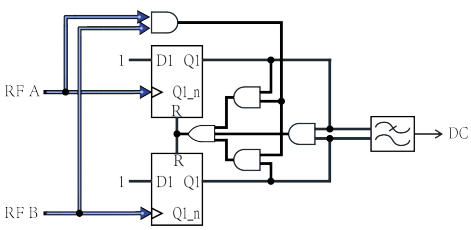

Figure 2: Tuning phase detector

The phase loop is acting like a PLL. The phase detector for the phase loop is different from the tuning phase detector. For the tuning phase detector, the two input signals are always the same frequency, but for the phase loop phase detector, it is acting like a frequency detector more than a phase detector. To speed up the pull-in process, an asymmetric phase detector is used. This phase detector is comprised of a phase detector and a frequency discriminator, as shown in Fig. 3. Away from locking, the phase detector becomes a frequency discriminator and the output of the phase detector is locked to logic high or logic low to pull the loop frequency towards the reference frequency. The timing waveforms are shown in Fig. 4.

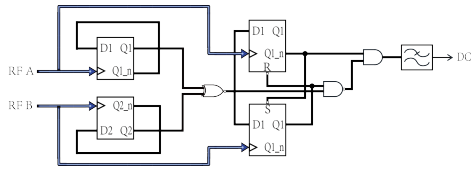

Figure 3: Frequency/phase detector

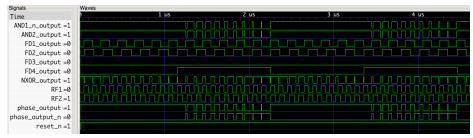

Figure 4: Timing of frequency/phase detector

Frequency Counters

Limited by the narrow band of the cavity, the precision of the frequency counter should be better than 10Hz. The previous design of the frequency counter counts the pulse directly. The accuracy of this kind of counter is related to the input frequency. To improve the performance, two frequency counters based on equal precision measurement method are designed to calculate the reference frequency and the loop frequency independently and then calculate the frequency error. The equal precision measurement uses two counters to count the time base signal and the input signal, as shown in Fig. 5. The two counters are enabled at the same time and the enable gate is controlled by the input signal. If the frequency of time base signal is f_s, the number in counter#1 is N_s, the number in counter#2 is N_x, then the input frequency would be [6]:

$$f_x = N_x * \frac{f_s}{N_s} \tag{1}$$

Eq. (1) indicates that f_x has no relationship with the measurement time T. In the period T, if the error of counter#1 is $|\Delta N_s|$, then it has to be $|\Delta N_s| \leq 1$. From Eq. (1), the another frequency that could be:

$$f_x^{'} = \frac{f_s}{N_s + \Delta N_s} * N_x \tag{2}$$

The measurement error is given by:

$$\Delta f_x = f_x - f_x^{'} = N_x f_s (\frac{1}{N_s} - \frac{1}{N_s + \Delta N_s}) \tag{3}$$

Noticed that $N_x f_s = N_s f_x$, the relative error is given by:

$$\frac{\Delta f_x}{f_x} = \frac{\Delta N_s}{N_s + \Delta N_s} \leq \frac{1}{N_s + 1} < \frac{1}{N_s} = \frac{1}{f_s \cdot T} \tag{4}$$

Eq. (4) indicates that the relative error is inverse proportion to time base frequency and measurement time T. To reduce the relative error, the time base frequency and T should be increased.

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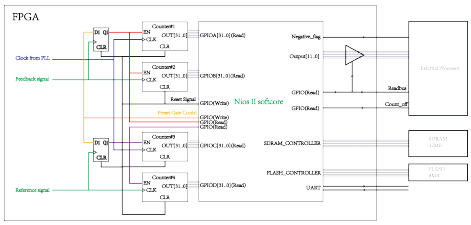

Figure 5: Frequency counters in FPGA

TEST

The frequency/phase detector and the counter board is tested on the test bench of LLRF system. The board is first tested by two signal generator whose 10MHz reference clock is connected together to provide two phase coherent signals. The phase detectors are tested from 5MHz to 500MHz. The results show that the tuning phase detector can run at maximum 220MHz, while the phase loop phase detector can run at maximum 400MHz. The result of the phase detector working on the designed frequency (200MHz) and maximum frequency is shown in Fig. 6 and Fig. 7.

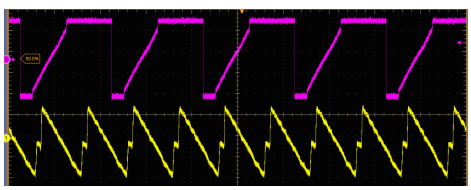

Figure 6: Test result at 200MHz

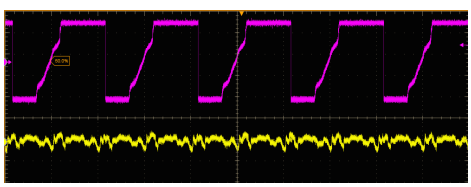

Figure 7: Test result at 400MHz

The frequency discriminator, constituted by the four frequency counters, is also tested on the test bench. Because of the equal precision method, the frequency discriminator can be tested at a lower frequency. The high precision signal generator, whose minimum frequency is 0.001Hz and maximum frequency is 120MHz, is used to test the frequency discriminator. The frequency error of the two signal generator is set to 1Hz. The frequency discriminator has been tested for 24 hours to collect data. During this time, 50000 data is collected by the computer. The statistics of the data shows that 55% of the results is 1Hz, and the other two possibility is 0Hz(25%) and 2Hz(20%), as shown in Fig. 8.

After the bench test, the board is installed on the LLRF system for the ACM system. All the requirement for the

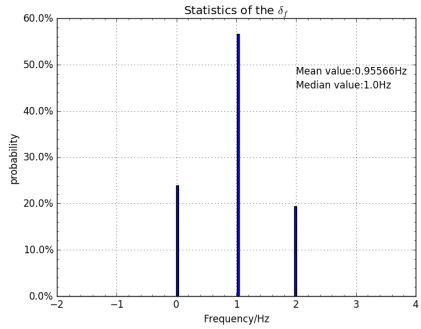

Figure 8: Test result of frequency discriminator

frequency/phase detector and counter of the LLRF system is satisfied by the new daughter board and it can provide higher precision feedback for the system.

CONCLUSION

An FPGA based frequency/phase detector and the counter is developed. This design supports four channel discriminations of RF frequencies/phases. Preliminary tests show that the frequency/phase detector for phase loop has a bandwidth of 400MHz, the tuning phase detector for tuning loop has a bandwidth of 200MHz, and the resolution of the frequency discriminator can reach as high as 1Hz. The phase-frequency detector has been successfully applied to the Accelerator Cryo Module (ACM) system and the requirement of the low-level RF control system has been satisfied.

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