

# A COMPACT 10 kW SOLID-STATE RF POWER AMPLIFIER AT 352 MHz

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## Abstract

A compact 10 kW RF power amplifier at 352 MHz was developed at FREIA for the European Spallation Source, ESS. The specifications of ESS for the conception of amplifiers are related to its pulsed operation: 3.5 ms pulse length and a duty cycle of 5%. The realized amplifier is composed of eight kilowatt level modules, combined using a planar Gysel 8-way combiner. The combiner has a low insertion loss of only 0.2 dB, measured at 10 kW peak power. Each module is built around a commercially available LDMOS transistor in a single-ended architecture. During the final measurements, a total output peak power of 10.5 kW was measured.

## INTRODUCTION

Solid-state RF high power amplifiers (SSA) are increasingly used in a large variety of systems including particle accelerators, such as cyclotrons and LINACs. A pioneering work in using SSA for synchrotron light sources started at SOLEIL [1], with 330 W modules using baluns. The increase in power per transistor allows today more effective designs. The operation in a LINAC using superconducting cavities reduces drastically the bandwidth of operation, which allows narrowband architectures to be implemented and thus simpler designs to be used [2]. In this context, a single-ended architecture has been demonstrated to ensure a high performance for power amplifier at the kilowatt-level [3]. The RF design implements matching networks in a single-ended architecture and avoids the use of baluns. The 50 Ohm input and output impedances are transformed to match the transistor's impedances using wide stepped microstriplines and are fine-tuned using surface mounted capacitors. Note that these impedances are roughly four times smaller than for the push-pull amplifier. DC feed at the drain is realised by connecting the supply voltage via a thick wire air coil and it uses a resistor for biasing at the gate. The kilowatt level module is built around a commercially available LDMOS transistor, the BLF188XR. The measured peak power per module is about 1.25 kW, while operating at 50 V drain voltage with a drain efficiency of 71% [4].

Eight of such modules were combined using a planar 8-way Gysel combiner to achieve above 10 kW output power. A very compact 10 kW amplifier at 352 MHz was realised, see Fig. 1. The 10 kW system consists of three stages, first a commercially available amplifier provides around 100 W with a gain of 50 dB. The second stage is composed of a kilowatt level module with a gain of about 20 dB, providing around 15 W input power to each of the eight modules.

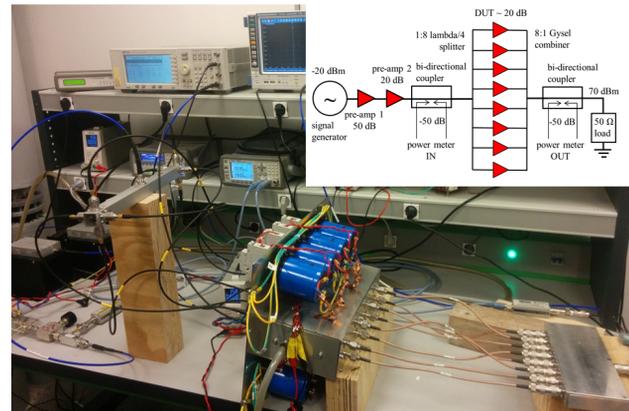


Figure 1: 10 Kilowatt power amplifier at 352 MHz. Inset: electric block diagram.

## KILOWATT LEVEL MODULE

Each module is built around an LDMOS transistor, the BLF188XR. Input and output matching networks implement a single-ended architecture and are realised on Rogers RO3003 substrate ( $\epsilon_r = 3$ ;  $\tan\delta = 0.001$ ; copper thickness,  $\text{Cu} = 35 \mu\text{m}$  and substrate height,  $h = 0.76 \text{ mm}$ ), see Fig. 2. The simulated output power with ADS is about 1.3 kW at 1 dB compression for a gain of 20.5 dB with 70% PAE. This is in good agreement with the measurements in ESS pulsed mode (i.e. duty cycle 5% and pulse duration 3.5 ms) the measured RF output power per module is 1.25 kW with a gain of 19 dB at 1 dB gain compression and a drain efficiency of 71%. Assembled in an aluminium casing, the temperature rises only few degrees, to about 30° C while it is close to 150° C in CW. The heat sink has a water cooling pipe (diameter 10 mm) and a water debit of about 8 l/min is maintained during operation. During CW measurements, the gain compresses by 2.5 dB and the efficiency drops to 61% at 1 kW output power. With improved cooling this amplifier could perform better in CW.



Figure 2: Kilowatt-level power amplifier in a single-ended architecture at 352 MHz.

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The amplifier is operated in Class B, with a quiescent drain current,  $IDq = 0.1$  A and a drain voltage,  $VDS = 50$  V. At nominal output power, the following harmonics levels are monitored: 2nd at -25 dBc, 3rd at -35 dBc, 4th at -44 dBc and 5th < -60 dBc. More information could be found in [3].

The eight amplifier modules were individually fine tuned to achieve a nominal power of 1.25 kW in pulsed mode (5% duty cycle and 3.5 ms pulse). The fine tuning resulted in different values and positions of the output matching capacitors. The phase imbalance among the eight amplifiers is small, it is smaller than  $5^\circ$ , see Fig. 3. The gain imbalance is also small, it is smaller than 0.5 dB at the nominal output power of 1.25 kW, see Fig. 4.

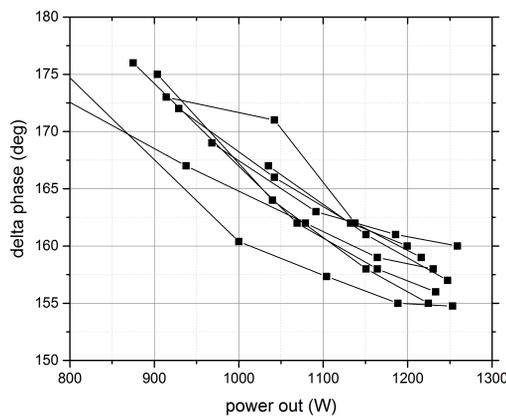


Figure 3: Phase spread of the 8 modules.

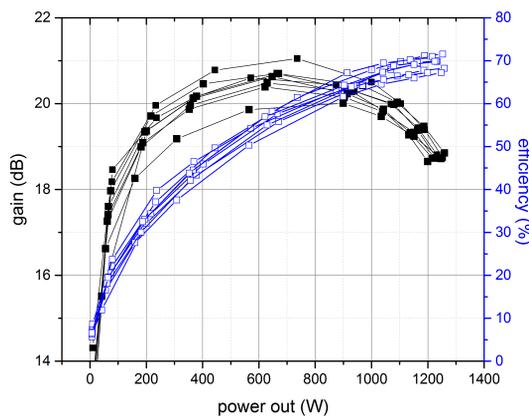


Figure 4: Drain and efficiency spread of the 8 modules.

### PLANAR COMBINER

A compact 8-way combiner has been developed in a planar technology. The combiner allows the combination of eight 1.25 kW modules to a total output power of 10 kW. One of the main challenges in designing a planar combiner for high RF power levels is to ensure that the combiner can dissipate the high power resulting from a mismatch, to avoid dielectric breakdown and to provide a high power combination efficiency.

A topology for power combiners in which the load used to dissipate power in the case of unbalanced inputs was connected directly to ground (unbalanced) instead of between the input lines as is the case of the Wilkinson combiner (balanced) was proposed by Gysel [5]. This architecture removes the restrictions on the electrical length of the load and allows larger loads to be used. By using a single stage 8-1 Gysel type combiner the port to port isolation is maintained, while the total insertion loss is kept low [6].

The proposed design is divided into two separate main boards, see Fig. 5a containing the input port balancing and the dummy loads and Fig. 5b for the output matching and combination stages. Two boards were used in order to enable the mounting of dummy loads on the back of the common section as well as to allow the use of two different board thicknesses. The use of multiple separate substrates was needed in order to accommodate the varying line impedances required to achieve a proper matching of the different combiner stages and is related also to power handling capabilities of the substrates. A Rogers TMM3 5.08 mm substrate is used for the output section while a TMM3 1.27 mm substrate is used for the common point configuration. The Rogers TMM3 substrate provide a low loss ( $\tan\delta = 0.002$ ) and high power handling capabilities, suitable to use in high power combiner designs.

The single stage 8-1 Gysel combiner has been tested up to 10 kW peak output power with no observable performance degradation or arcing. The total insertion loss was measured to be 0.2 dB at nominal power. The performance degradation due to parasitic coupling between adjacent lines in the common point section of the combiner was reduced by the use of weakly coupled stubs between adjacent lines which helps to realign the phase balance between transmission lines.

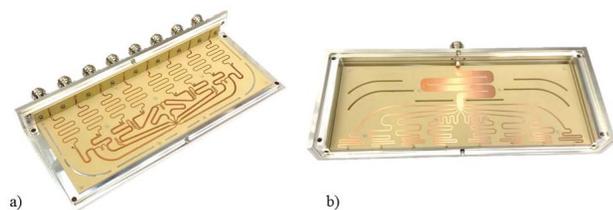


Figure 5: The output board (a) mounted on the lower section of the aluminium casing and the common board (b) mounted on the upper section of the aluminium casing, together with output connectors.

### TIME DOMAIN MEASUREMENTS

For pulsed operation, a large capacitor (68 mF) is used to supply the energy per pulse. The voltage droop is less than 1 V from the drain operating voltage 50 V or 2% of the drain voltage after 3.5 ms, whereas each module delivers 1.25 kW output power. The power supply recharges the capacitor during the silence between pulses, see Fig. 6.

The droop over the pulse is measured around 1 A, see Fig. 7. There is a spread in the current used by each mod-

ule with a maximum current of 42 A and a minimum of 37 A, which reflects into the efficiency per module. The efficiency per module can be evaluated in real time, having available a direct readout of voltage and current per module. Analogue circuits using micro controller (ATmega328P) are implemented to monitor simultaneously all eight drain currents and voltages. Each module is provided with a Hall effect current transducer and drain voltage is also monitored. Time-multiplexed measurements are performed resulting in the measurements of the voltage and current per module.

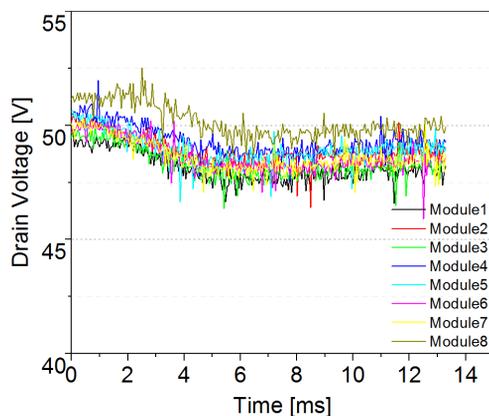


Figure 6: Voltage during pulse for each of the eight modules.

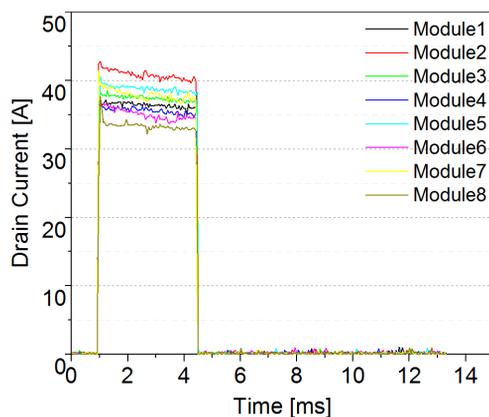


Figure 7: Current during pulse for each of the eight modules.

## TESTING OF AMPLIFIER AT 10 KW

The amplifier is implemented in three gain stages, as shown in the inset of Fig. 1. The amplifier is made to fit a 19-inch (48 cm) standard rack and has a height of 9 rack units (40 cm), comprising the capacitor bank, with a depth of only 20 cm. At the input, a quarter wavelength splitter is used to distribute the input power, around 15 W to each of the eight modules. During few hours of operation, power measurements are performed using the directional couplers at the input and output of the combiners. Combiners and cables losses are small (0.4 dB at the input and 0.32 dB at the output). These are not removed from the gain and output power measurements as presented in Fig. 8.

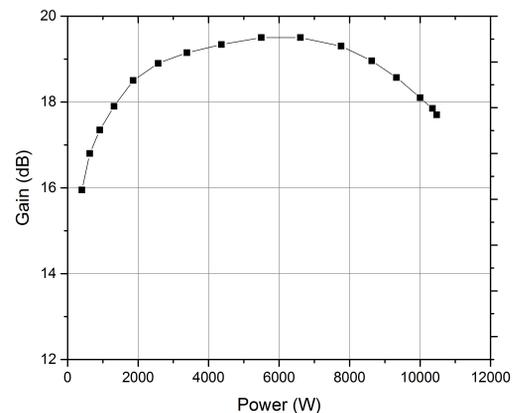


Figure 8: Amplifier gain and output power.

## CONCLUSION

A compact 10 kW pulsed peak power amplifier has been developed at 352 MHz using eight modules in a single ended architecture. The modules are robust, easy to manufacture and show an output power of 1.25 kW with a drain efficiency of 71%. Measurements of the variation among the modules show a small variation within the phases and gains. A single stage 8-way Gysel combiner is also implemented with an insertion loss of 0.2 dB at nominal power, which allows the combination of the modules to a total measured output power of 10.5 kW. Analogue circuits are used to monitor simultaneously all eight drain currents and voltages using microcontroller based time-multiplexed measurements. The amplifier, RF modules, combiners and monitoring circuits were realised in house, at the FREIA laboratory.

## ACKNOWLEDGEMENT

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