LLRF SYSTEM PERFORMANCE DURING SC CAVITY CONDITIONING AT STF KEK

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Abstract

High Energy Accelerator Research Organization (KEK) is now developing a digital low-level radio frequency (LLRF) control system based on digital feedback control at superconducting RF test facility (STF). The goal is to achieve the amplitude and phase stability of the accelerating field in the superconducting accelerator. Testing and evaluation of the digital LLRF system were conducted during the cavity conditioning performed between October and December 2015 to determine the level of performance. To enable cavity signal monitoring, direct sampling system was constructed and evaluated.

INTRODUCTION

The Superconducting RF Test Facility (STF) was built for purposes of research and development related to the International Linear Collider (ILC). The RF is 1.3 GHz with a pulse duration of 1.5 ms and a repetition rate of 5 Hz. RF stabilities of 0.07 % rms in amplitude and 0.24 deg rms in phase are required for the ILC [1].

The STF-2 project [2] is currently underway. The STF-2 accelerator consists of two cryomodules with twelve superconducting cavities. During the cavity conditioning conducted between October and December of 2015, each cavity was conditioned at the maximum gradient before quenching. The average accelerating gradient was 30 MV/m [3]. The cavities each have a loaded Q_L of $5 \cdot 10^6$ and are driven by a 600 kW klystron. In this paper, we report on the evaluation of several different digital low-level radio frequency (LLRF) boards with the goal of determining their performance in terms of amplitude and phase stability.

Table 1: Digital Board Developed for LLRF System in STF

Board	ADC	DAC	Xilinx FPGA
μTCA-1	(4 x 16-bit) LTC2208	(2 x 16-bit) AD9783	XC5FX70T
cPCI	(4 x 16-bit) LTC2208	(2 x 14-bit) AD9764	XC2VP30
FMC	(16 x 16-bit) AD9650	(2 x 16-bit) MAX5888	XC6VLX240T XC6VLX130T
μTCA-2	(2 x 16-bit) AD5474	-	XC5FX70T

DIGITAL LLRF SYSTEM IN STF-KEK

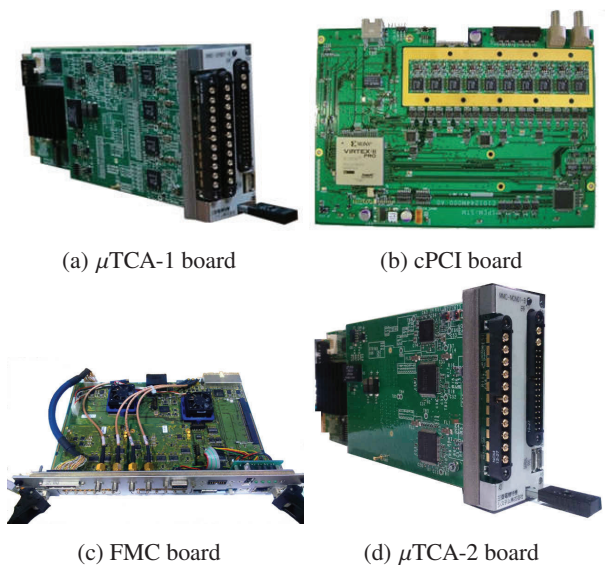
We are still developing the digital LLRF boards for the STF. The first board was cPCI installed in the STF phase 1 project [4,5]. The next board was the μTCA-1, developed for application to the compact energy recovery linac (cERL) at KEK [6, 7]. The most recent development is an FMC board, which will be installed in the STF-2 project. We are also developing a μTCA-2 board for cavity signal monitoring. Four digital LLRF boards installed at the STF-KEK (see Table 1) were tested and evaluated. Photos of all the boards are shown in Figure 1.

RF DETECTION

A simplified diagram of the digital LLRF control system is shown in Figure 2. There are two methods of treating the signal from the cavity. The first method is heterodyne field detection, which requires a down conversion process. The μTCA-1, cPCI, and FMC boards utilize this method. The second method is direct sampling, which does not require any down conversion process [8]. The μTCA-2 board implements this method.

Down Conversion

In the system using the down conversion method, the RF input signal is mixed with the local oscillator (LO) and the output is an intermediate frequency (IF), as shown in Figure 2. In the STF, the IF is 10.16 MHz. This IF signal is then



(a) μTCA-1 board (b) cPCI board

(c) FMC board (d) μTCA-2 board

Figure 1: Digital LLRF board in STF.

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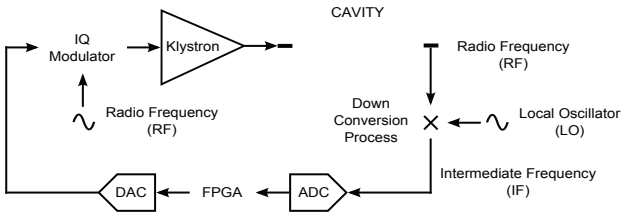

Figure 2: Simplified diagram of digital LLRF system.

fed to ADC. IQ detection and feedback calculation are performed in the field-programmable gate array (FPGA). The output from the FPGA is then converted back to analog by the DAC and used to control the klystron. The ADC sampling clocks for these systems are 81.25 MHz (for the μTCA-1 and FMC boards) and 40.63 MHz (for the cPCI board). These are generated from the master oscillator (f_0 = 1300 MHz) by dividing this frequency by 16 and 32, respectively. For the frequency divider, we use an AD9510 (Analog Devices Inc.). To estimate the amplitude and phase from the RF signal, the ADC input frequency (f_{in}) and sampling clock frequency (f_{s}) must satisfy the relation $L \cdot f_{\text{in}} = N \cdot f_{\text{s}}$ where L and N are integers. This means that L samples are taken during the N period of the f_{in} signal. In a system using the down-conversion method, the parameters are $N = 1$ and $L = 8$ (for $f_{\text{s}} = 81.25$ MHz) or $L = 4$ (for $f_{\text{s}} = 40.63$ MHz). The I and Q component detection can be governed by the following equations:

$$I = \frac{2}{L}\sum_{k=1}^{L} V(k) \cdot \cos\left(2\pi \cdot \frac{N}{L} \cdot k\right) \quad (1)$$

$$Q = \frac{2}{L}\sum_{k=1}^{L} V(k) \cdot \sin\left(2\pi \cdot \frac{N}{L} \cdot k\right) \quad (2)$$

where V is the sampled signal [9].

Direct Sampling

In direct sampling, the down-conversion process is not required and the system becomes simpler. The absence of a down-converter can also minimize the temperature dependency and number of higher-order modes that would be caused by the down-converter. Direct sampling is based on an under-sampling technique in which the sampling frequency is lower than the ADC input frequency. A direct sampling technique with a commercial FPGA board (ML555) and fast ADC (AD5474) have been tested and evaluated in the STF [10, 11].

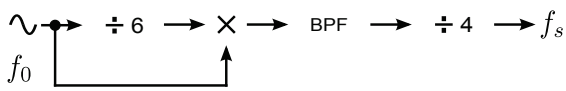

Figure 3: Sampling clock generation for direct sampling. f_0 = 1300 MHz, f_s = 270.83 MHz, BPF with f_{center} = 1083 MHz and BW = 4 MHz.

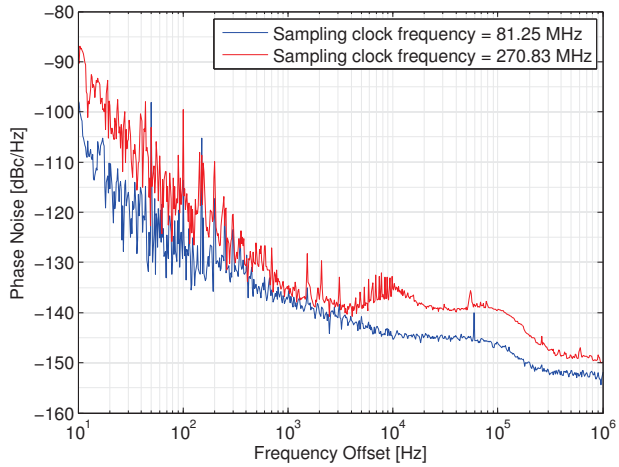

Figure 4: Sampling clock phase noise distribution. (For sampling clock with frequency = 81.25 MHz, the jitter is 109 fs. For sampling clock with frequency = 270.83 MHz, the jitter is 70 fs. Both jitters are calculated with frequency offset ranging from 10 Hz to 1 MHz).

In our case, we choose $L = 5$ and $N = 24$. The ADC input (f_{in}) was 1300 MHz and the sampling frequency (f_{s}) was 270.83 MHz. The sampling clock generation diagram for direct sampling is shown in Figure 3. It is composed of one mixer (Mini-Circuit, ZEM4300), two frequency dividers (Analog Devices, AD9510), and one bandpass filter with f_{center} = 1083 MHz and BW = 4 MHz (Sogo Electronics, Inc.).

We measured the phase noise of the ADC sampling clock for these LLRF systems. Phase noise measurement was performed with an Agilent Technology E5052A signal source analyzer. For a system with a down-conversion process, the ADC sampling clock frequency was 81.25 MHz and its RMS jitter was 109 fs with a frequency offset range of between 10 Hz and 1 MHz. For a system with direct sampling, the ADC sampling clock frequency was 270.83 MHz and its RMS jitter was 70 fs with a frequency offset range of between 10 Hz and 1 MHz. Both phase noise distributions are shown in Figure 4.

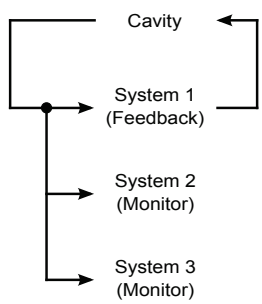

Figure 5: Measurement setup for board comparison.

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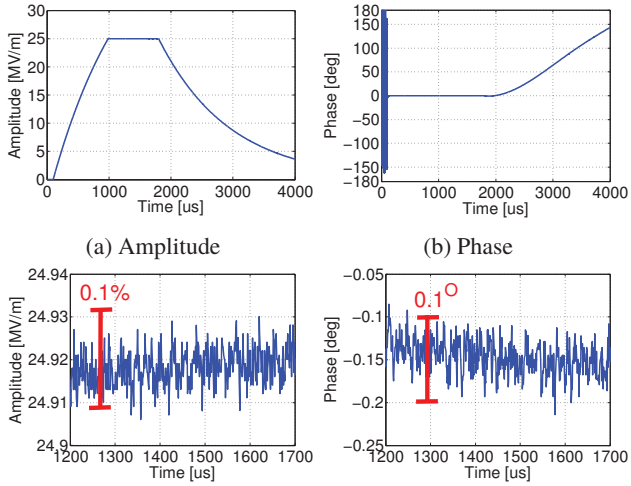
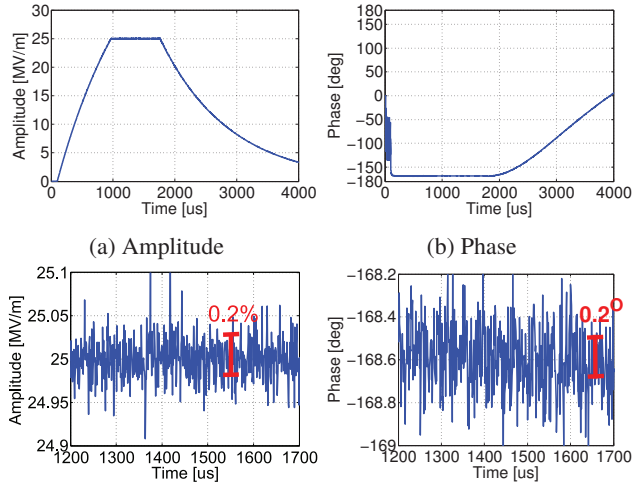


(a) Amplitude (b) Phase

(c) Amplitude flattop (d) Phase flattop

Figure 6: Waveform of amplitude and phase of μTCA-1 board with feedback algorithm.



(a) Amplitude (b) Phase

(c) Amplitude flattop (d) Phase flattop

Figure 7: Waveform of amplitude and phase of μTCA-2 board with direct sampling algorithm.

MEASUREMENT SETUP

For the evaluation, three boards where operated simultaneously. One board was used for feedback control while the other two boards were used to perform monitoring as shown in Figure 5. Using this method, we can compare the performance of two boards in term of amplitude and phase stability.

The μTCA-1 and cPCI boards were evaluated as feedback controllers. The FMC and μTCA-2 boards were only evaluated as signal monitoring boards.

PERFORMANCE OF LLRF SYSTEM

We analyzed the data obtained from each system and compared the amplitude and phase stability at the flattop for each board. Figure 6(a) and 6(b) shows the amplitude and phase waveform, respectively, of the μTCA-1 board under proportional feedback control. Cavity filling starts at 100 μs, flattop starts at 1000 μs, and the RF is turned off at 1800 μs. The amplitude and phase flattop of the μTCA-1 board are shown in Figure 6(c) and 6(d), respectively. The gradient was set to 25 MV/m when the μTCA-1 board was operated as a feedback control and it was set to 20 MV/m when the cPCI board was operated as a feedback control board. Figure 7(a) and 7(b) shows the amplitude and phase waveform for the μTCA-2 board, respectively. The amplitude and phase flattop are shown in Figure 7(c) and 7(d), respectively.

Given that the cavity bandwidth is very narrow (e.g. $f_{1/2} = 130\,\text{Hz}$ at $Q_L = 5 \cdot 10^6$ and $f_0 = 1.3\,\text{GHz}$), the signal fluctuation in the measured data is mainly caused by the front-end performance of the board. Consequently, the stability calculation can represent the board performance. To discard any overshoot at the leading edge of the flattop, only 1200 μs to 1700 μs is considered for the stability calculation.

The boards performances are summarized in Table 2. The best performance is that of the FMC board. A system using a direct-sampling technique has a lower stability than one using down-conversion process. We chose parameter $L = 5$. This means that only five sampled data are used to estimate the I and Q components. The selection of an L parameter with a larger value is expected to improve amplitude and phase stabilities because of the averaging effect. In addition, a digital filter may be implemented to improve the stability.

Table 2: Stability Comparison of Digital LLRF Boards in STF

System	Amp. Stability %.rms	Phase Stability deg.rms
μTCA-1	0.017	0.020
cPCI	0.025	0.024
FMC	0.012	0.020
μTCA-2	0.10	0.15

SUMMARY

Superconducting cavity conditioning was performed at the STF between October and December 2015. The performances of the digital LLRF systems were evaluated and compared. The best result was obtained from the FMC system for which the amplitude and phase stabilities were 0.012 % rms and 0.020 deg rms, respectively. The FMC system has sixteen ADCs. Therefore, it will be implemented for the STF-2 project in which all the twelve superconducting cavities will be operated. A digital LLRF system using a direct-sampling technique has a lower stability than that one which uses a down-conversion process. The larger value of the L parameter and the digital filter implementation are expected to improve the amplitude and phase stabilities.

REFERENCES

[1] "ILC Technical Design Report", http://www.linearcollider.org/ILC/?pid=1000895.

[2] H. Hayano, "Superconducting Accelerator Development at STF for ILC", Proceedings of the 12th Annual Meeting of Particle Accelerator Society of Japan, Tsuruga, Japan, 2015.

[3] Y. Yamamoto et al., "High Gradient Cavity Performance in STF-2 Cryomodule for the ILC at KEK", Proceedings of IPAC'16, Busan, Korea, 2016.

[4] S. Michizono et al., "Digital LLRF System for STF S1 Global", IPAC'10, Kyoto, Japan, 2010.

[5] S. Michizono et al., "Performance of Digital LLRF system for STF in KEK", LINAC'08, Victoria, Canada, 2008.

[6] T. Miura et al., "Low-Level RF System for cERL", IPAC'10, Kyoto, Japan, 2010.

[7] T. Miura et al., "Performance of the μTCA Digital Feedback Board for DRFS Test at KEK-STF", Proceedings of IPAC'11, San Sebastian, Spain, 2011.

[8] Z. Geng et al., "Evaluation of Fast ADCS for Direct Sampling RF Field Detection for the European XFEL and ILC", Proceedings of LINAC'08, Victoria, Canada, 2008.

[9] M. Grecki et al., "Estimation of IQ Vector Components of RF Field", Proc. 12th Int. Conf Mixed Design of Integrated Circuits and Systems, 2005.

[10] H. Katagiri et al., "High Speed Data Acquisition System using FPGA for LLRF Measurement and Control", LINAC'08, Victoria, Canada, 2008.

[11] Y. Okada et al., "Direct Sampling of RF Signal for 1.3 GHz Cavity", PAC'09, Vancouver, Canada, 2009.

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