About the New Linear Accelerator Control System at GSI

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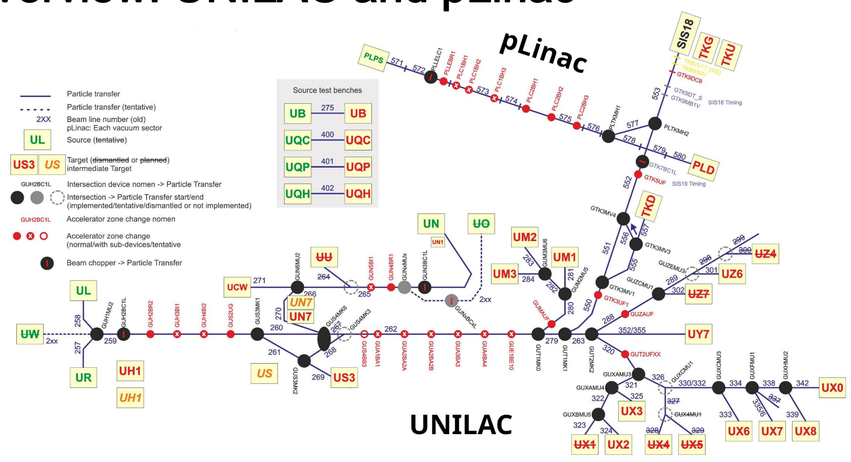
Abstract

The UNILAC is going to be the heavy ion injector linac for FAIR, currently under construction next to GSI, supported by a dedicated proton linac. The current linac control system dates back to the 1990s. It was initiated for SIS18 and ESR, which enlarged GSI at the time, and was retrofitted to the UNILAC. The linear decelerator HITRAP was added in the last decade, while an sc cw linac is under development. Today CRYRING, SIS18 and ESR are already operated by a new system based on the LHC Software Architecture LSA and other developments from CERN, as FAIR will be. In order to replace the outdated linac control system and simplify and unify future operation, a control system on the same basis is being developed for all GSI linacs. Recently the first data supply tests were performed during a dry run.

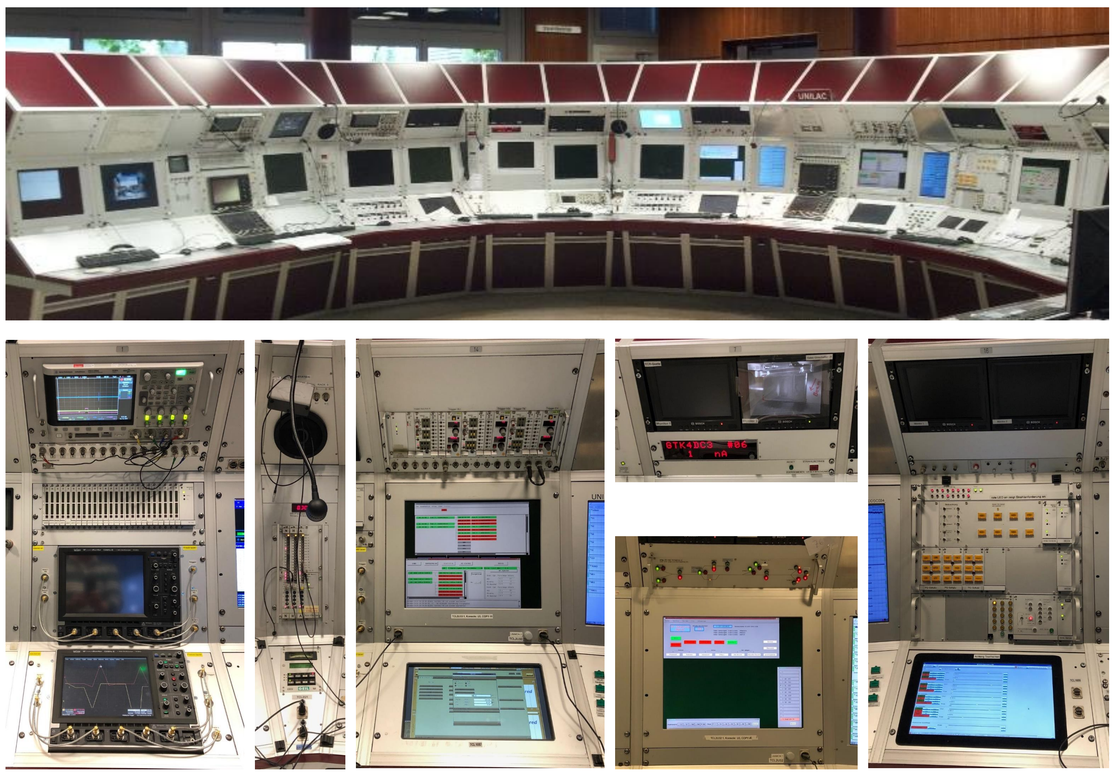
Overview: UNILAC and pLinac

The main linac of the UNILAC, a 108 MHz Alvarez type DTL, in operation since 1975.



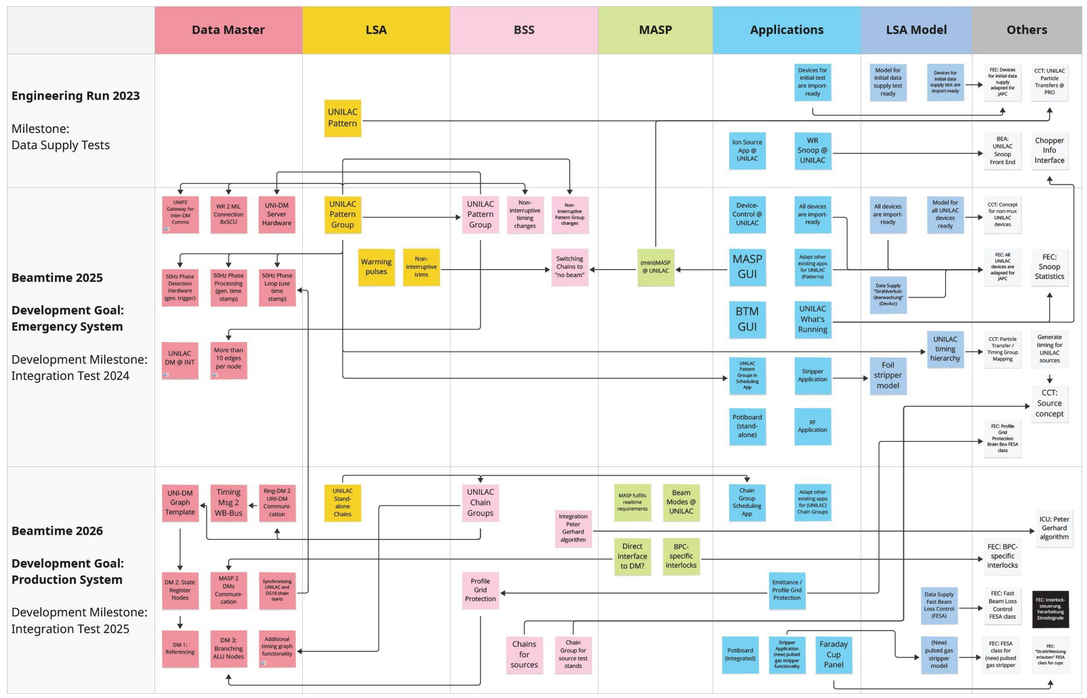
Schematic layout of the UNILAC and pLinac. The UNILAC is mapped to 44 particle transfers (=timing groups), each containing one or more accelerator zones.

Main Control Room Modernization



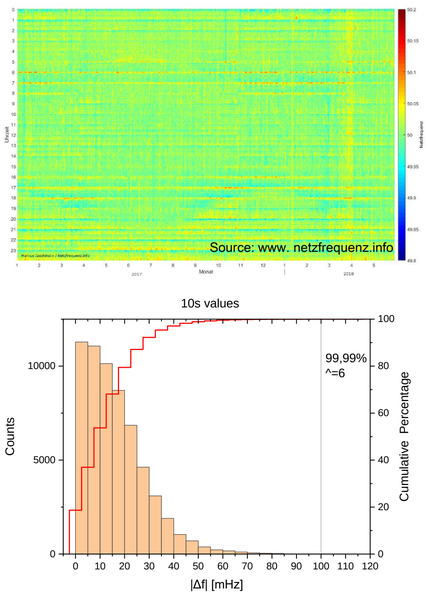
Overview of the UNILAC domain in the current main control room (top), details (bottom, from left): oscilloscopes and beam position monitor; fixed timing interface, pointer instruments; configurable timing interface, legacy consoles; video monitors, numerical display, cup control panel; beam request lights, SEM grid protection switches, interlock and beam loss indicators.

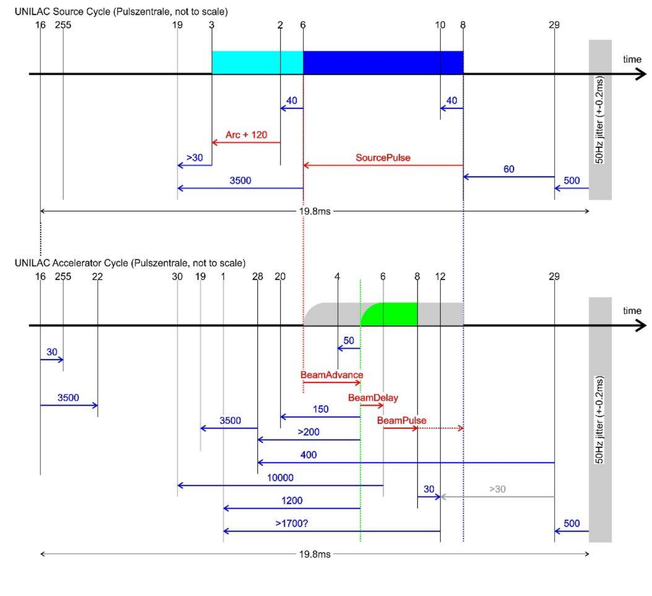
Migration Strategy Roadmap



Overview of the major milestones for the migration of the UNILAC to the new control system. The development efforts are categorized by the main building blocks of the control system (columns). Interdependencies are indicated by arrows. The vertical order renders the timeline, with the major steps *Engineering Run 2023* as the first test with beam, and the *Beamtimes 2025* and *2026*, with the (intermediate) development goals *Emergency* and *Production System*, respectively.

Timing: 50 Hz Synchronization and UNILAC Cycle

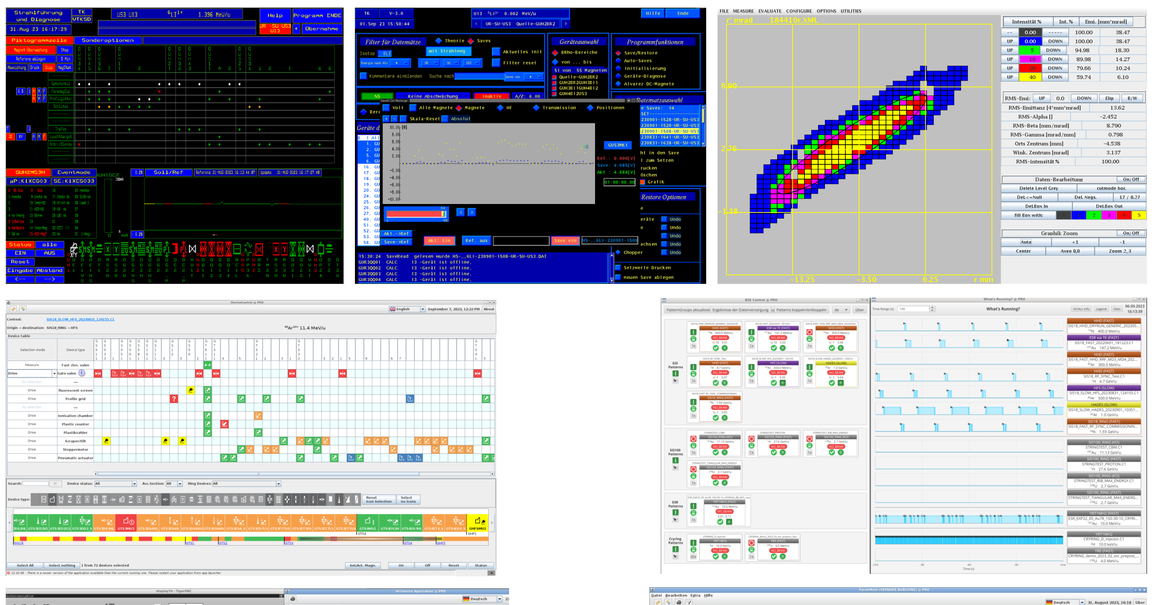


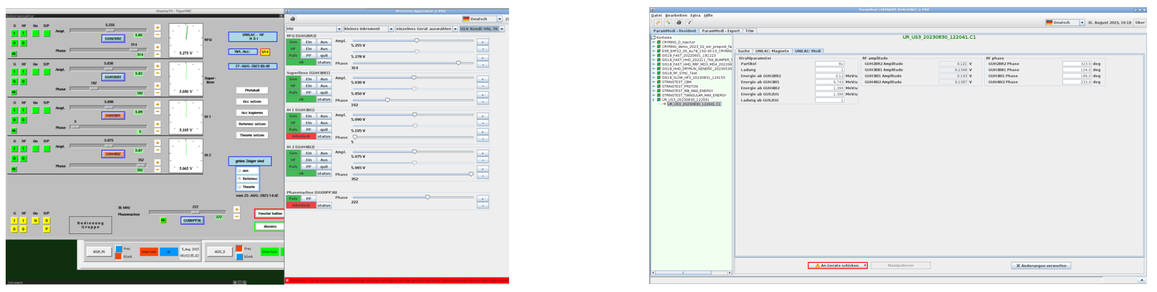


Left: The linac rf operates tube amplifiers in the high power stages. The tube cathodes are heated by ac current. To preserve constant amplification conditions, the pulsed operation of the linac has to be synchronized to the 50 Hz electrical grid. This has consequences for the synchronization of the FAIR facility to the UNILAC. The map (top) shows the variation of the grid frequency, the graph (bottom) shows the corresponding frequency statistics.

Right: The diagrams show the timing event sequences for the ion sources (top) and the accelerator (bottom). The cycle length is limited to 19.8 ms to enable synchronization with the grid.

Operating Applications





Overview of operating applications (clockwise from top left): SD*, IBHS*, ProEmi, BSS control & What's running, ParamModi, RF*, Device Control

*: Legacy control system, RF: left legacy, right new control system

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