



Towards the optimization of the Safety Life-Cycle for Safety Instrumented Systems

(WEBR02)

B. Fernández, G. De Assis, R. Speroni, T. Otto and E. Blanco

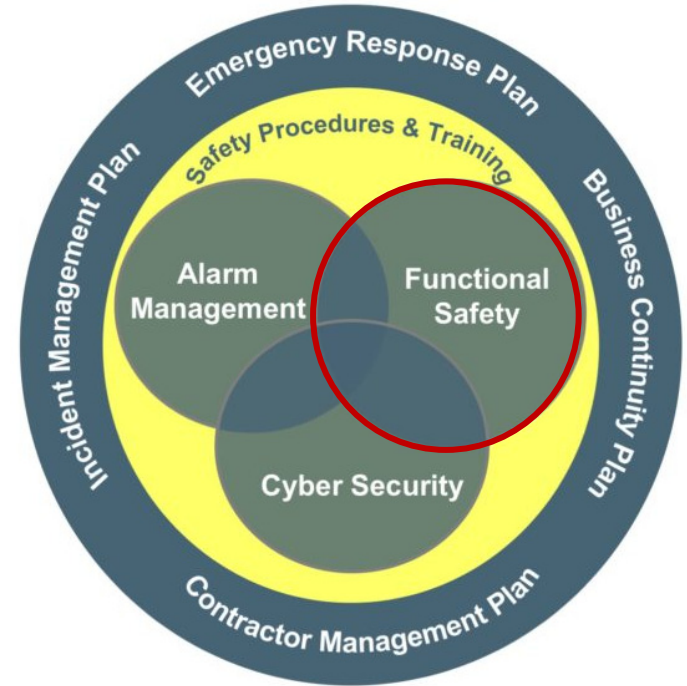
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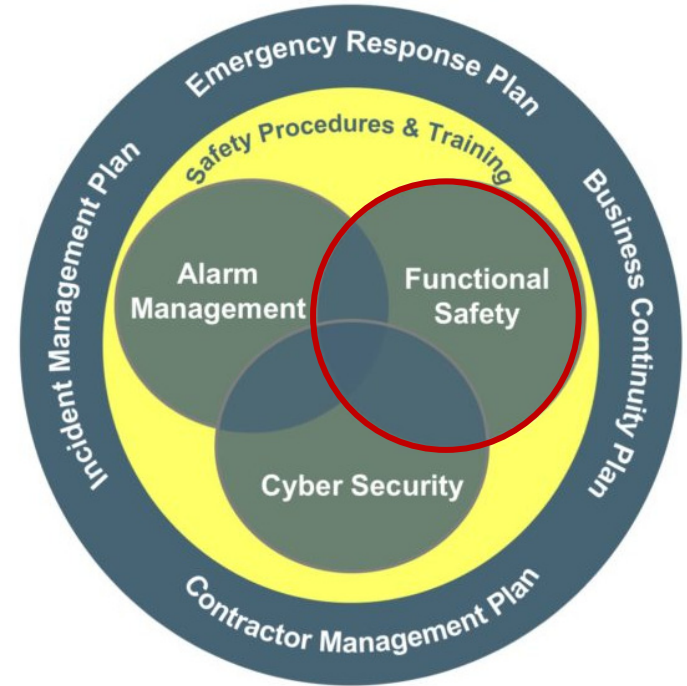
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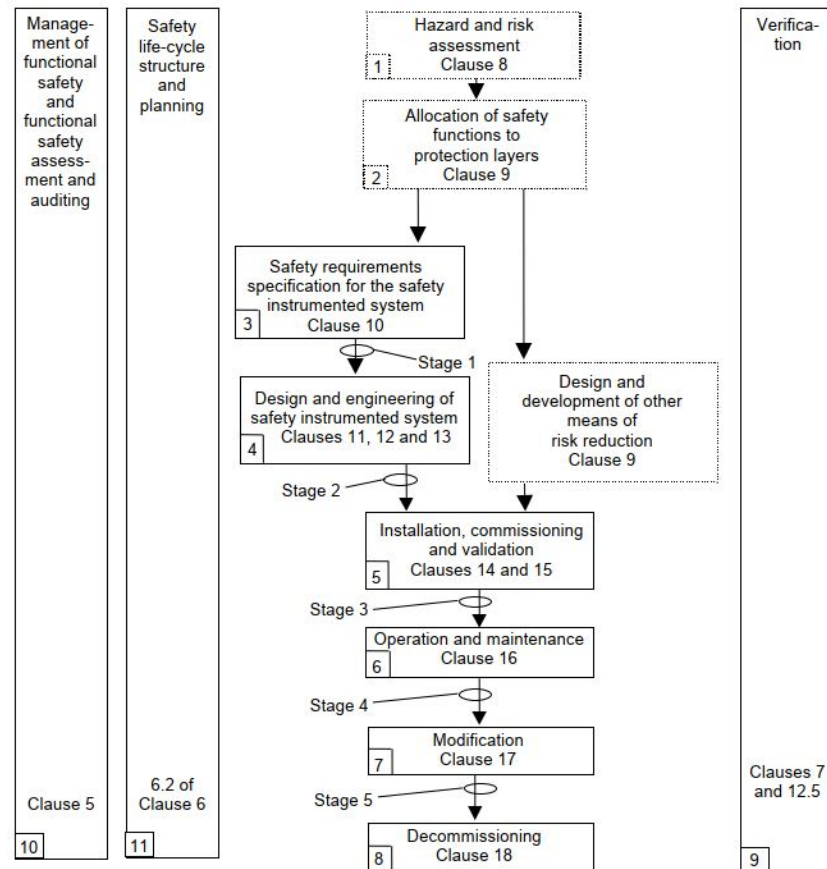
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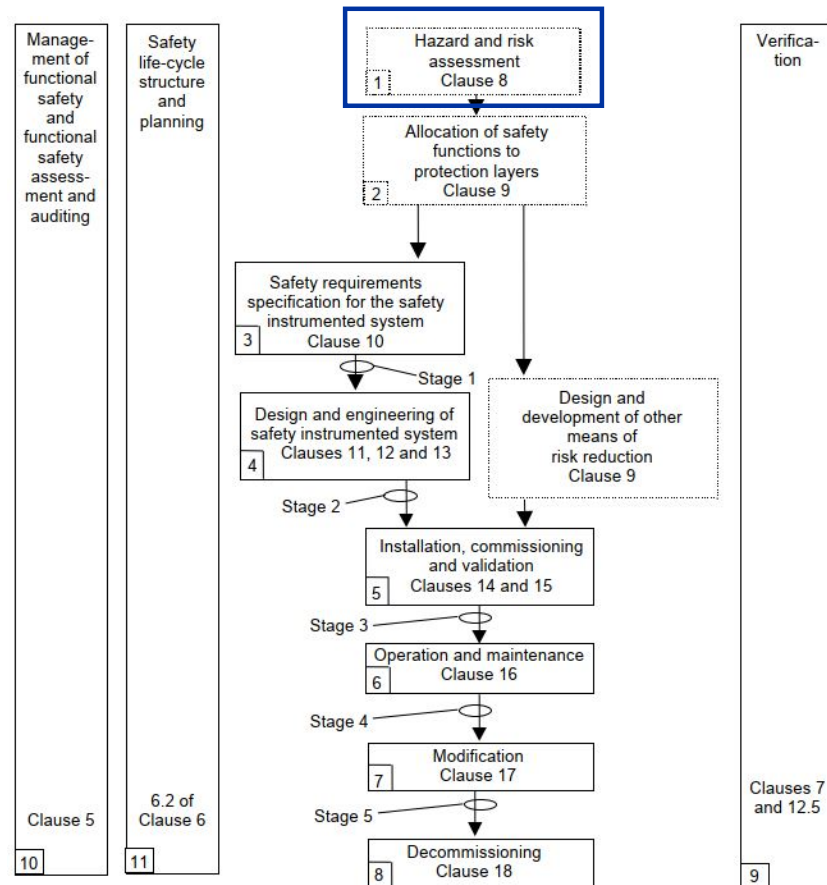
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 - 19 Clauses (**requirements**)



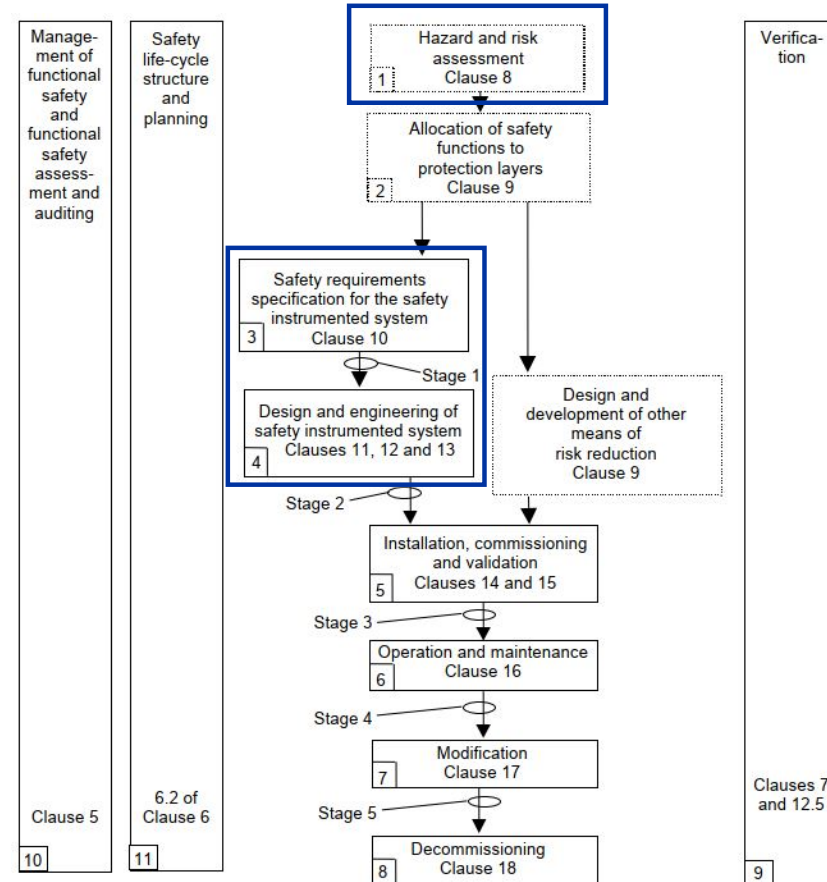
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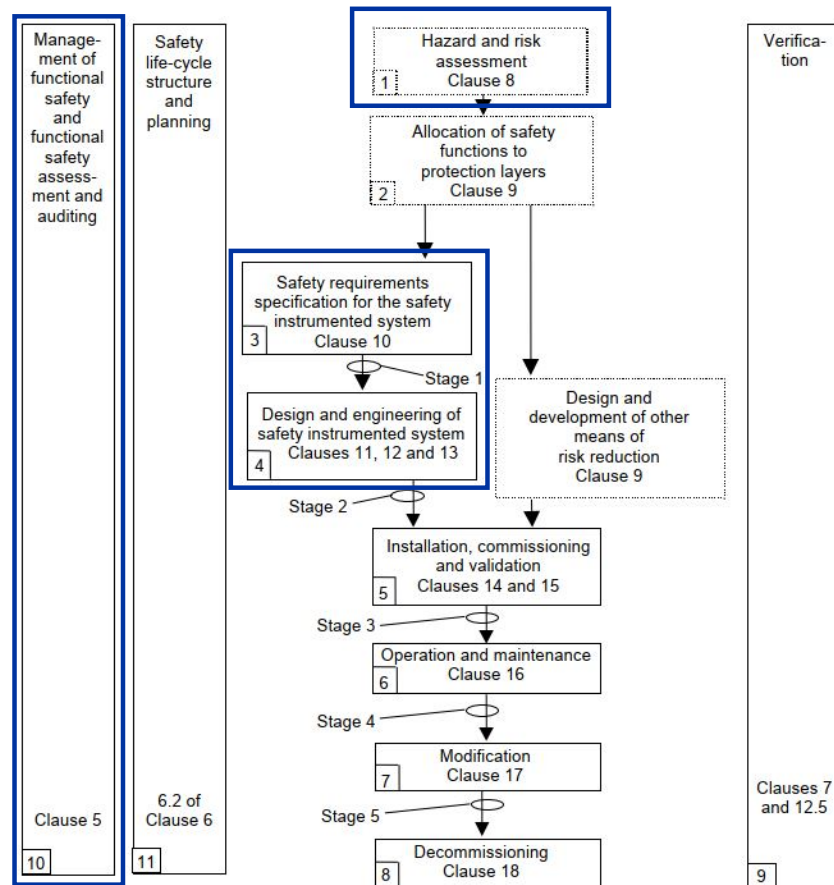
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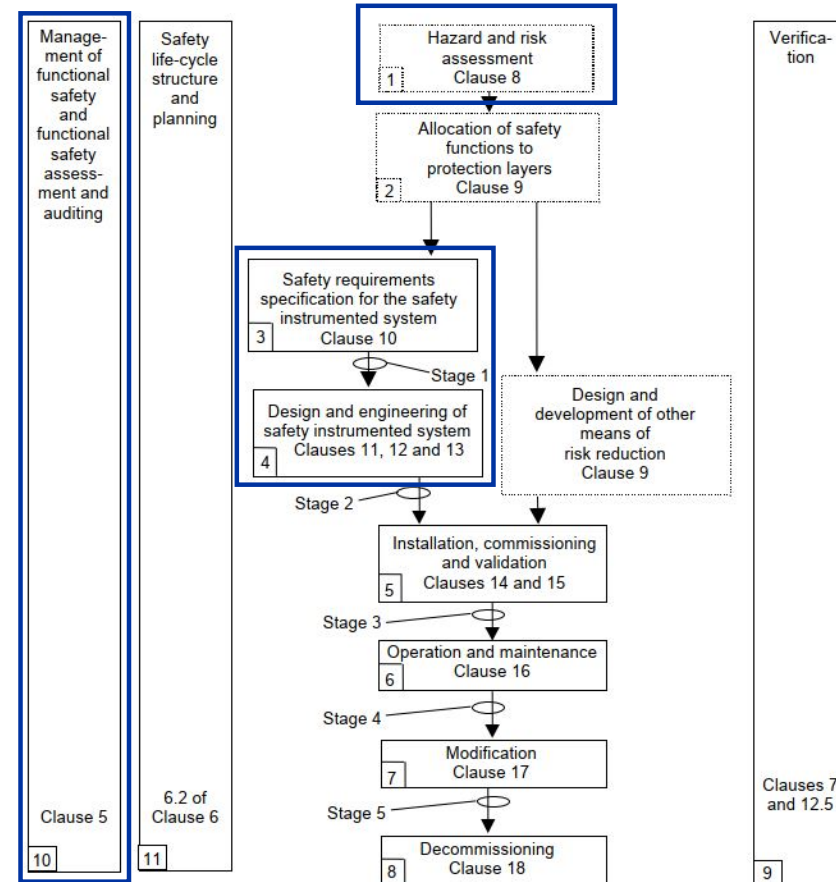
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- It provides the **safety life-cycle**:
 - 11 phases (to complete the project)
 - 19 Clauses (**requirements**)
- Very **challenging** task to **implement** all the requirements (lots of resources and time-consuming)



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Some major challenges:

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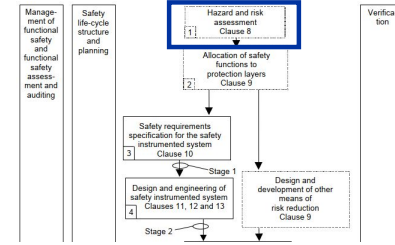
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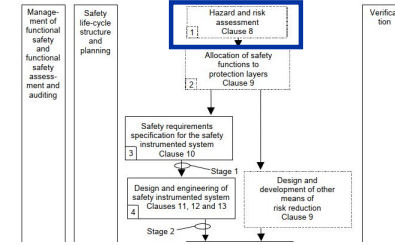
This paper analyses **some** of the most challenging **phases (1, 3, 4 and 10)** and presents the **adopted solutions**

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Target Safety Integrity Level (SIL)

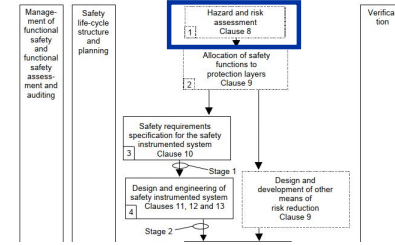


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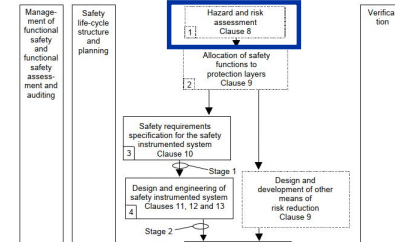


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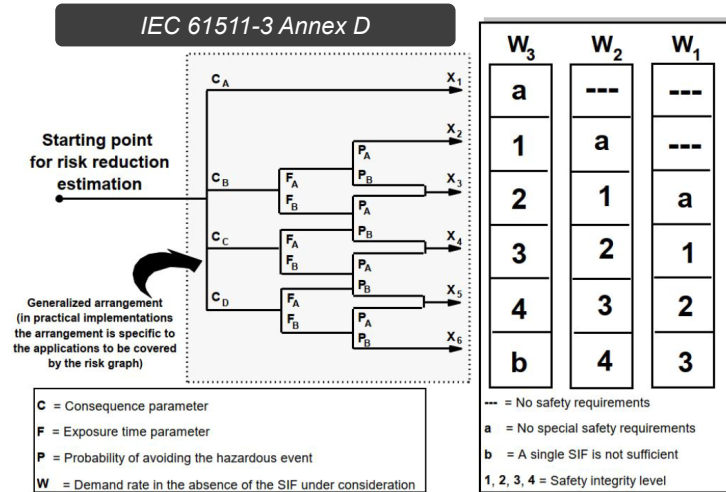
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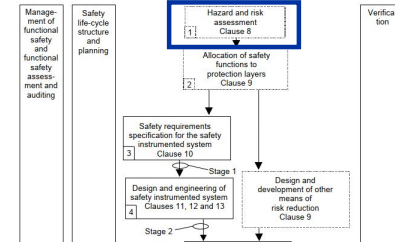
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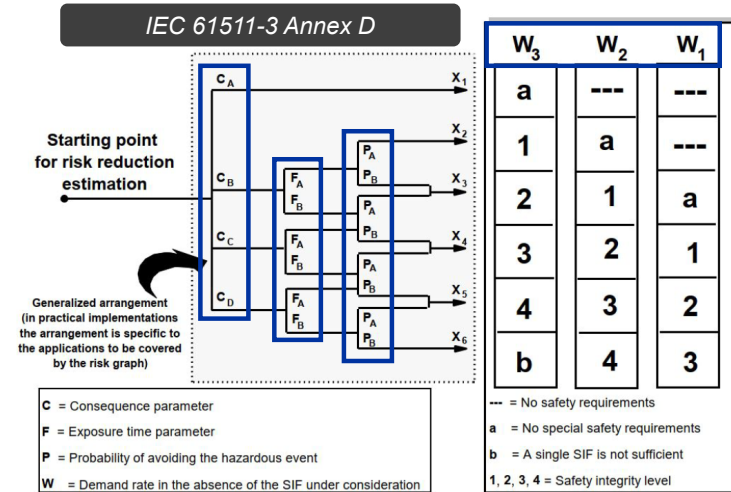
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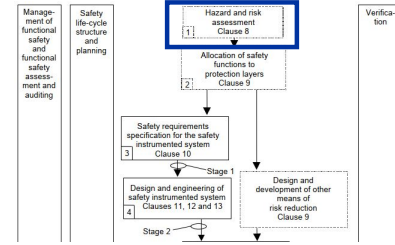
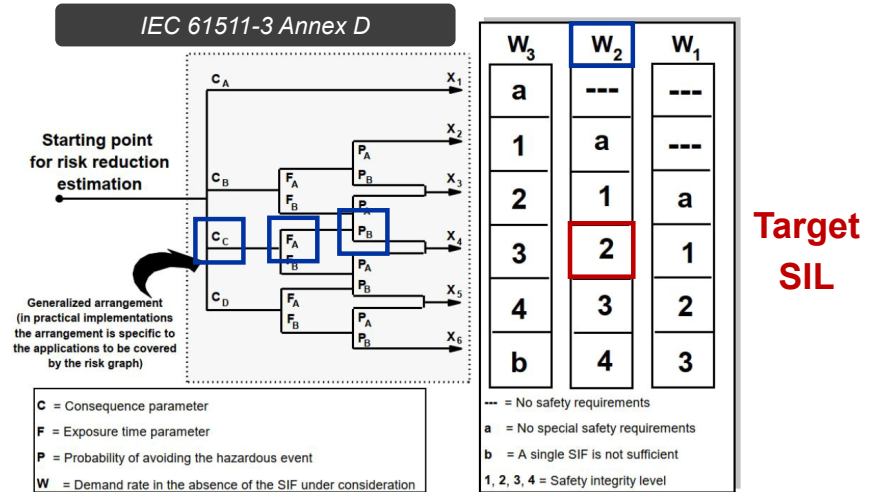
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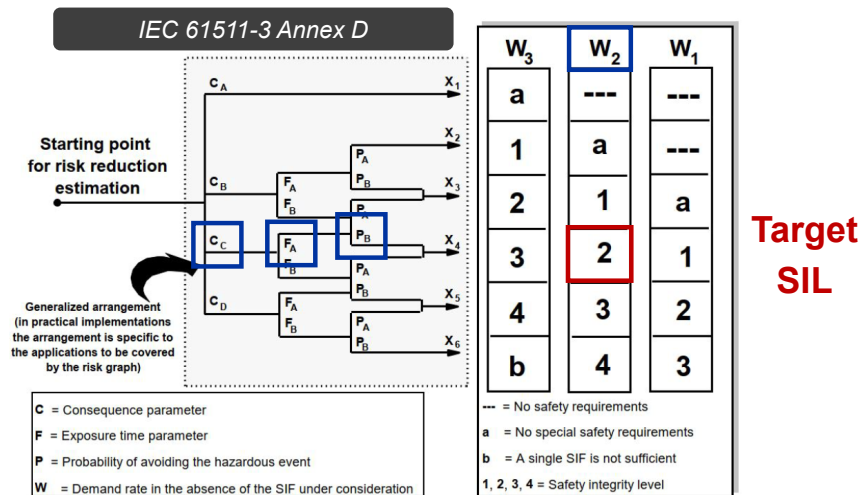
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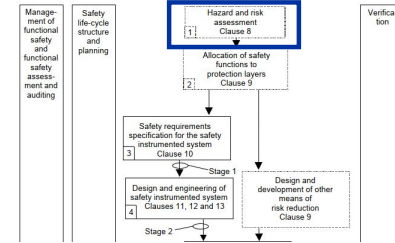
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For **personnel**, **machine** and **environmental** protection



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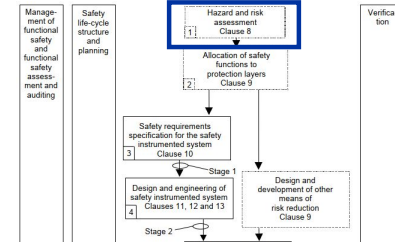
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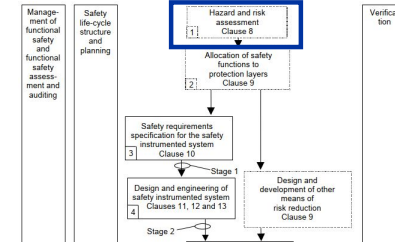
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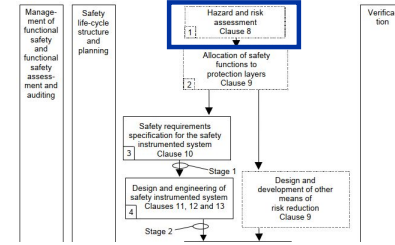
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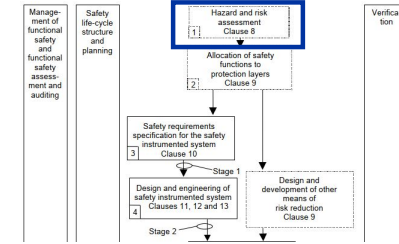
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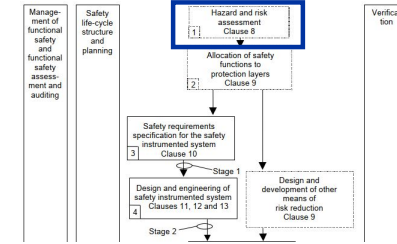


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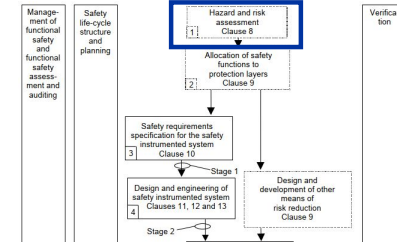
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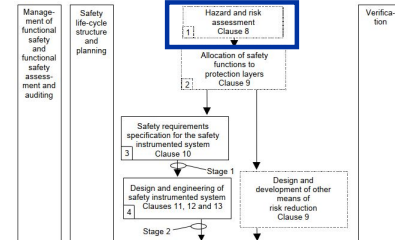
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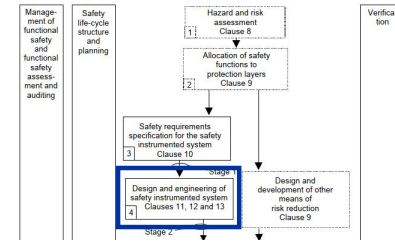
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Adopted solutions:

- FMEA + calibrated risk graph**
- Hazard and risk analysis and assessment **report templates**

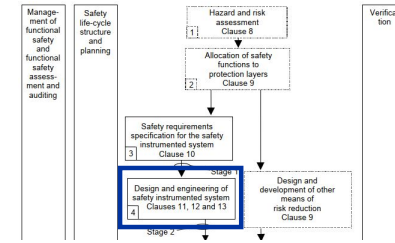


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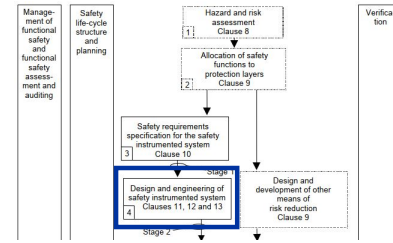
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SIS req.

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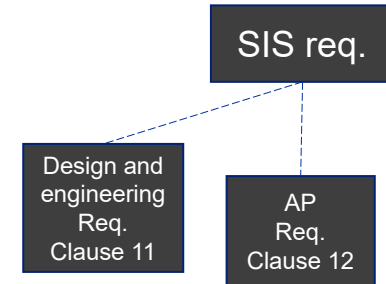
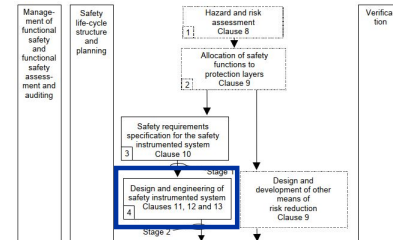
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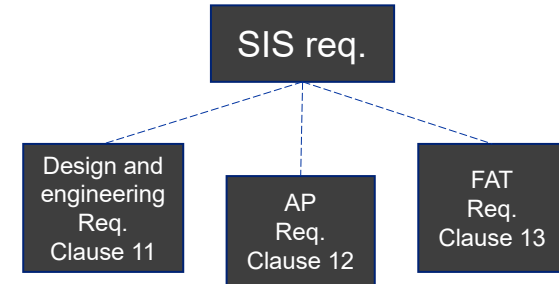
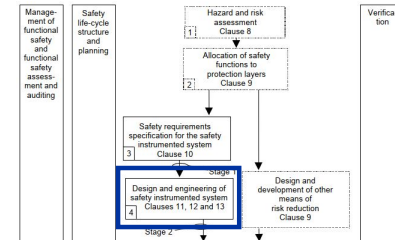
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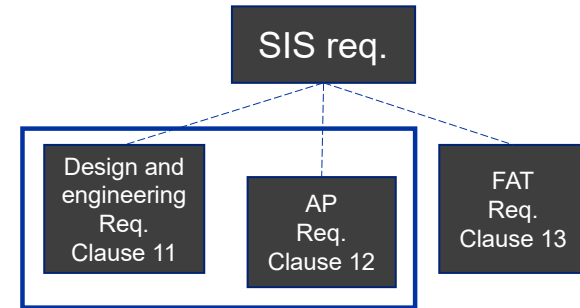
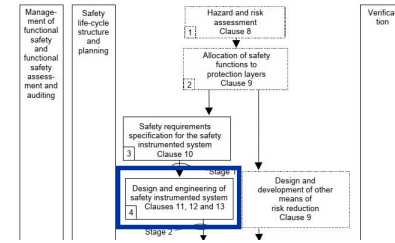
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Sensor Subsystem



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Average Probability of Failure
On Demand for the sensor group

IEC 61508-6:2010 Annex B

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Demand Mode of Operation		
Safety Integrity Level (SIL)	PFD_{avg}	Required risk reduction
4	$\geq 10^{-5}$ to $< 10^{-4}$	$> 10^4$ to $\leq 10^5$
3	$\geq 10^{-4}$ to $< 10^{-3}$	$> 10^3$ to $\leq 10^4$
2	$\geq 10^{-3}$ to $< 10^{-2}$	$> 10^2$ to $\leq 10^3$
1	$\geq 10^{-2}$ to $< 10^{-1}$	$> 10^1$ to $\leq 10^2$

SIS design and engineering – Hardware Fault Tolerance

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 - Even if the prob. of failure is compliant with target SIL, **we may need to apply redundancy**

SIS design and engineering – Hardware Fault Tolerance

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 - Even if the prob. of failure is compliant with target SIL, **we may need to apply redundancy**
 - **Use the reliability model** (sensors + controller + actuators) and **analyze the SIF architecture**



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Hardware Fault Tolerance
IEC 61511-1:2016 Clause 11.4

SIL	Minimum HFT
1 (any mode)	0
2 (low demand mode)	0
2 (continuous mode)	1
3 (high demand mode) or continuous mode)	1
4 (any mode)	2

HFT (Hardware Fault Tolerance)



SIS design and engineering – Hardware Fault Tolerance

▪ Challenges:

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*Hardware Fault Tolerance
IEC 61511-1:2016 Clause 11.4*

SIL	Minimum HFT
1 (any mode)	0
2 (low demand mode)	0
2 (continuous mode)	1
3 (high demand mode or continuous mode)	1
4 (any mode)	2

HFT (Hardware Fault Tolerance)



SIS design and engineering – Hardware Fault Tolerance

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Hardware Fault Tolerance
IEC 61511-1:2016 Clause 11.4

SIL	Minimum HFT
1 (any mode)	0
2 (low demand mode)	0
2 (continuous mode)	1
3 (high demand mode) or continuous mode)	1
4 (any mode)	2

HFT (Hardware Fault Tolerance)

Redundancy is needed, if
continuous mode



SIS design and engineering – Hardware Fault Tolerance

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- **Use the reliability model** (sensors + controller + actuators) and **analyze the SIF architecture**

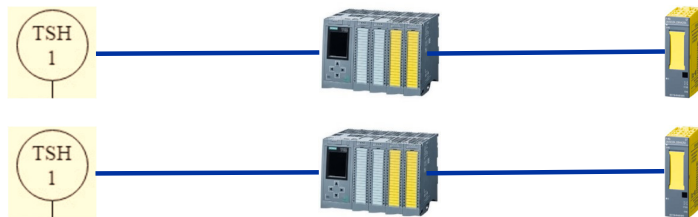
Hardware Fault Tolerance
IEC 61511-1:2016 Clause 11.4

SIL	Minimum HFT
1 (any mode)	0
2 (low demand mode)	0
2 (continuous mode)	1
3 (high demand mode) or continuous mode)	1
4 (any mode)	2

Architectural Constraints
IEC 61508:2010-2 Clause 7.4.4 Route 1H or 2H

HFT (Hardware Fault Tolerance)

Redundancy is needed, if
continuous mode



SIS design and engineering – Hardware Fault Tolerance

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Hardware Fault Tolerance
IEC 61511-1:2016 Clause 11.4

SIL	Minimum HFT
1 (any mode)	0
2 (low demand mode)	0
2 (continuous mode)	1
3 (high demand mode) or continuous mode)	1
4 (any mode)	2

HFT (Hardware Fault Tolerance)

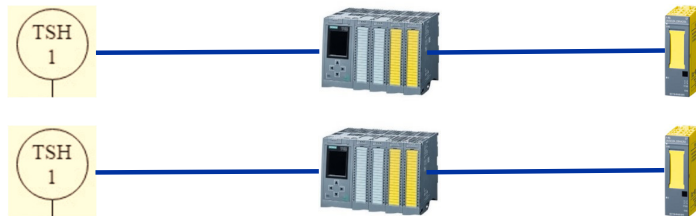
SFF (Safe Failure Fraction)

Architectural Constraints
IEC 61508-2:2010 Clause 7.4.4 Route 1H

SFF	HFT		
	0	1	2
$SFF < 60\%$	SIL1	SIL2	SIL3
$60\% \leq SFF < 90\%$	SIL2	SIL3	SIL4
$90\% \leq SFF < 99\%$	SIL3	SIL4	SIL4
$SFF \geq 99\%$	SIL3	SIL4	SIL4

Example for **type A** devices (without processor)

Redundancy is needed, if
continuous mode



SIS design and engineering – Hardware Fault Tolerance

Challenges:

- Even if the prob. of failure is compliant with target SIL, **we may need to apply redundancy**
- **Use the reliability model** (sensors + controller + actuators) and **analyze the SIF architecture**

Hardware Fault Tolerance
IEC 61511-1:2016 Clause 11.4

SIL	Minimum HFT
1 (any mode)	0
2 (low demand mode)	0
2 (continuous mode)	1
3 (high demand mode) or continuous mode)	1
4 (any mode)	2

HFT (Hardware Fault Tolerance)

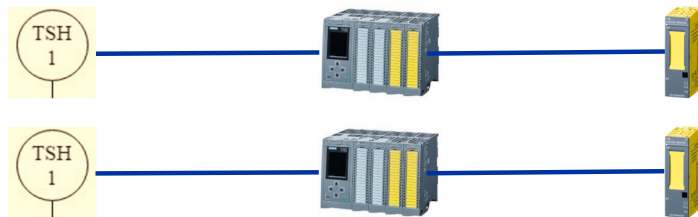
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Architectural Constraints
IEC 61508-2:2010 Clause 7.4.4 Route 1H

SFF	HFT		
	0	1	2
$SFF < 60\%$	SIL1	SIL2	SIL3
$60\% \leq SFF < 90\%$	SIL2	SIL3	SIL4
$90\% \leq SFF < 99\%$	SIL3	SIL4	SIL4
$SFF \geq 99\%$	SIL3	SIL4	SIL4

Example for **type A** devices (without processor)

Redundancy is needed, if
continuous mode



SIS design and engineering – Hardware Fault Tolerance

Challenges:

- Even if the prob. of failure is compliant with target SIL, **we may need to apply redundancy**
- Use the reliability model** (sensors + controller + actuators) and **analyze the SIF architecture**

Hardware Fault Tolerance
IEC 61511-1:2016 Clause 11.4

SIL	Minimum HFT
1 (any mode)	0
2 (low demand mode)	0
2 (continuous mode)	1
3 (high demand mode) or continuous mode)	1
4 (any mode)	2

HFT (Hardware Fault Tolerance)

SFF (Safe Failure Fraction)

Architectural Constraints
IEC 61508-2:2010 Clause 7.4.4 Route 1H

SFF	HFT		
	0	1	2
$SFF < 60\%$	SIL1	SIL2	SIL3
$60\% \leq SFF < 90\%$	SIL2	SIL3	SIL4
$90\% \leq SFF < 99\%$	SIL3	SIL4	SIL4
$SFF \geq 99\%$	SIL3	SIL4	SIL4

Example for **type A** devices (without processor)

Redundancy is needed, if
continuous mode



Redundancy is **not** needed, if
 $SFF \geq 60\%$ for type A devices

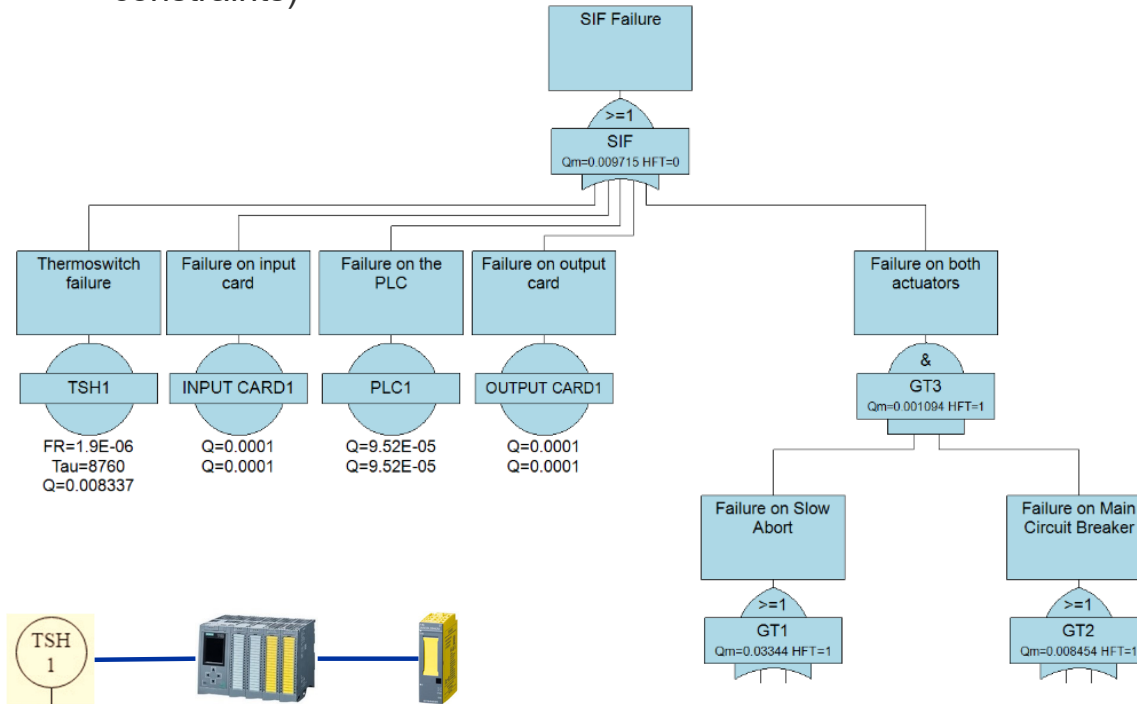
Phase 4 - SIS design and engineering (both)

Phase 4 - SIS design and engineering (both)

- **Adopted solution: Isograph's Reliability workbench** (both for hardware random failures and architectural constraints)

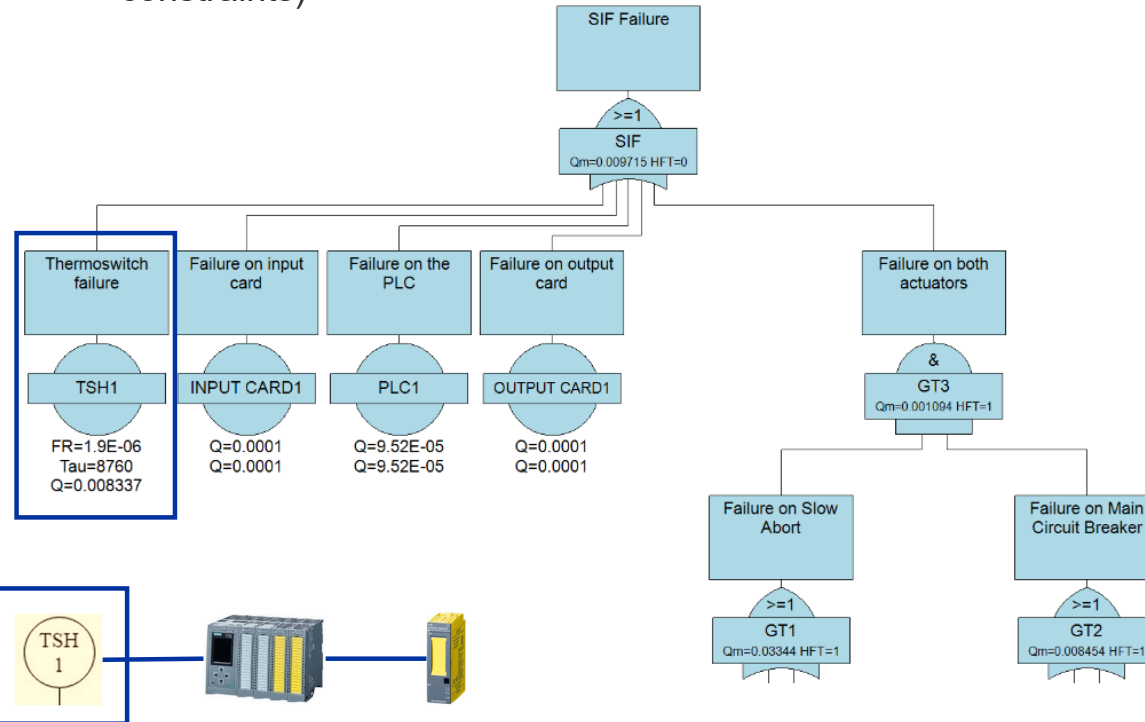
Phase 4 - SIS design and engineering (both)

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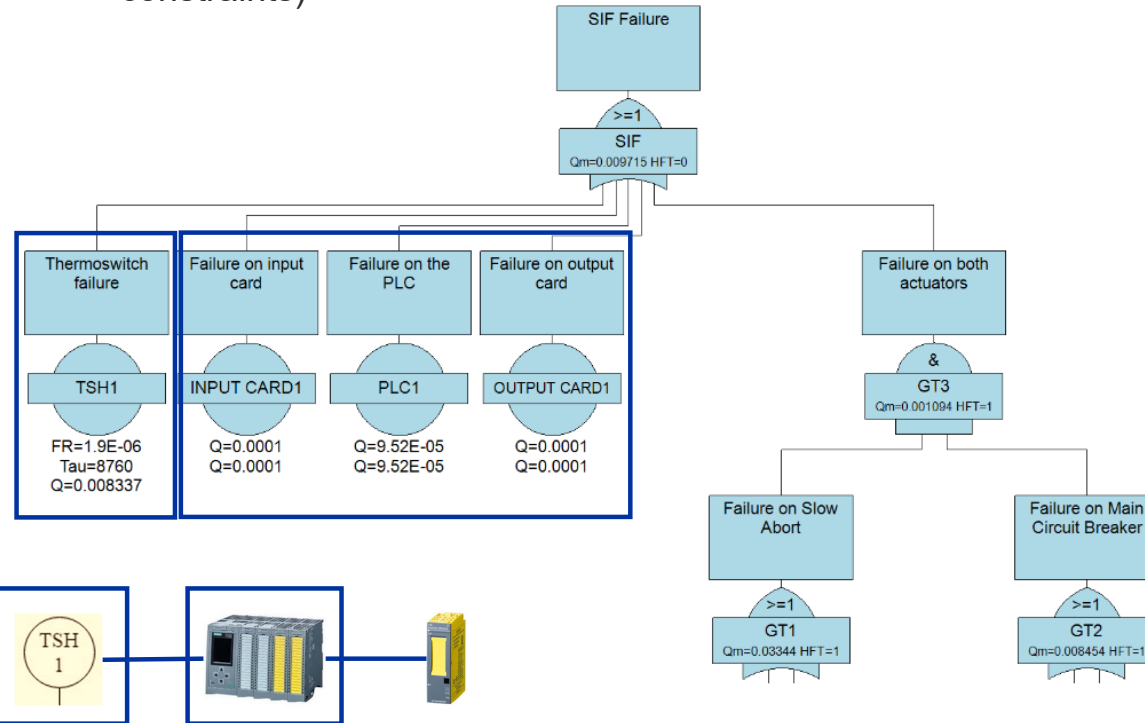
Phase 4 - SIS design and engineering (both)

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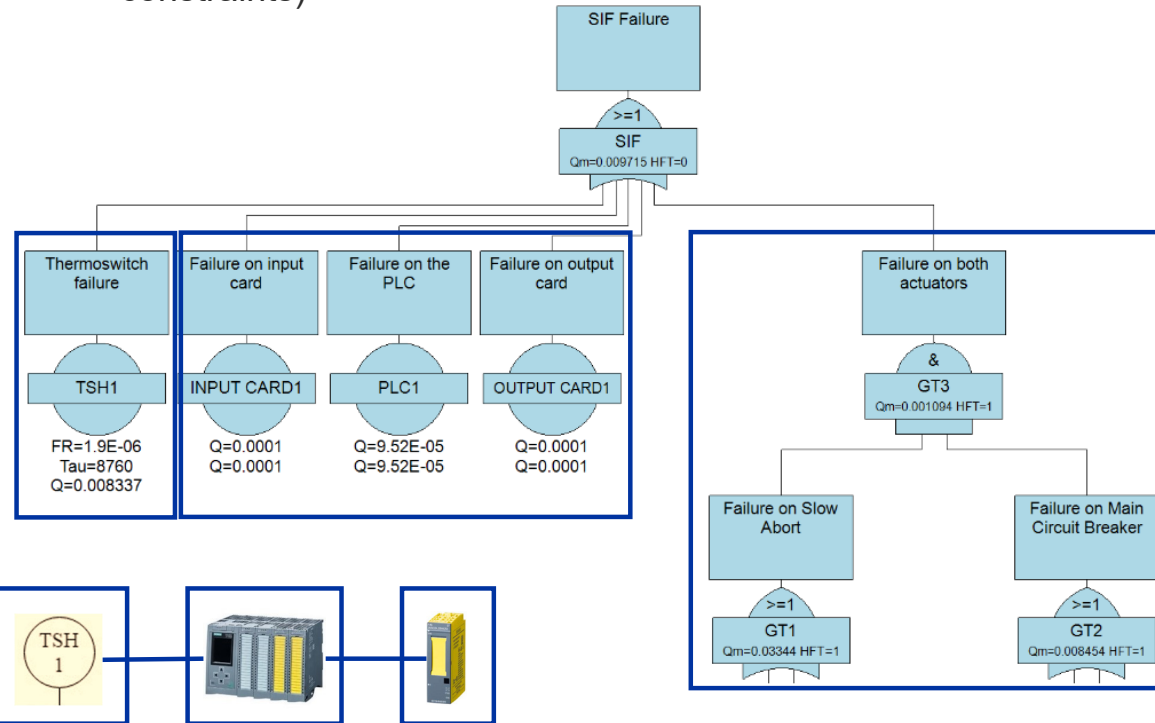
Phase 4 - SIS design and engineering (both)

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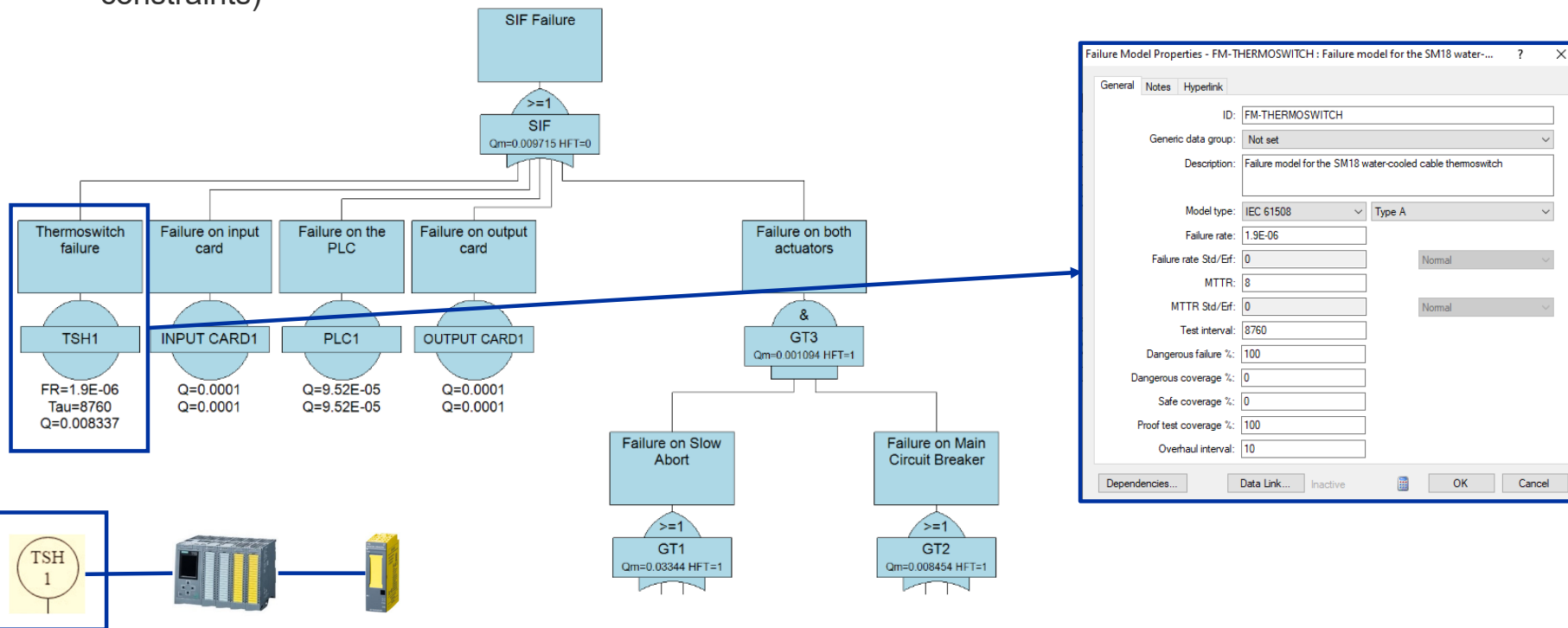
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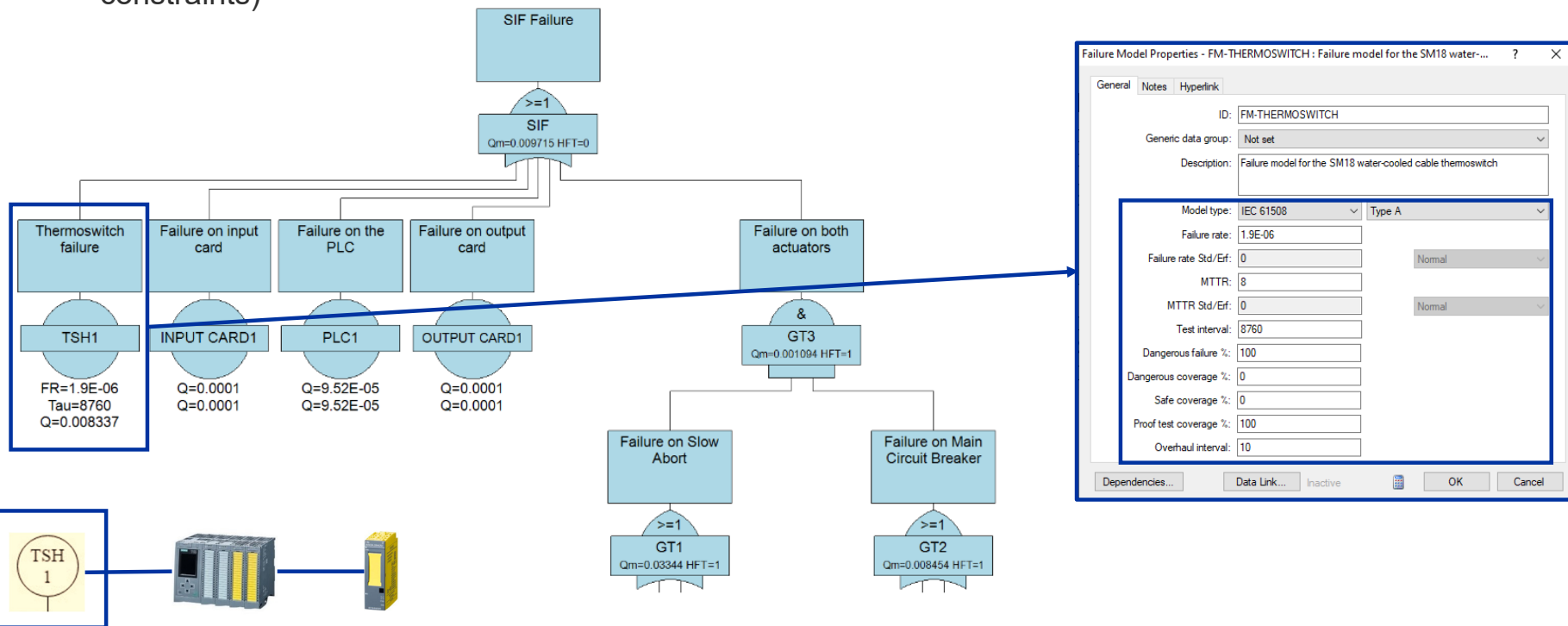
Phase 4 - SIS design and engineering (both)

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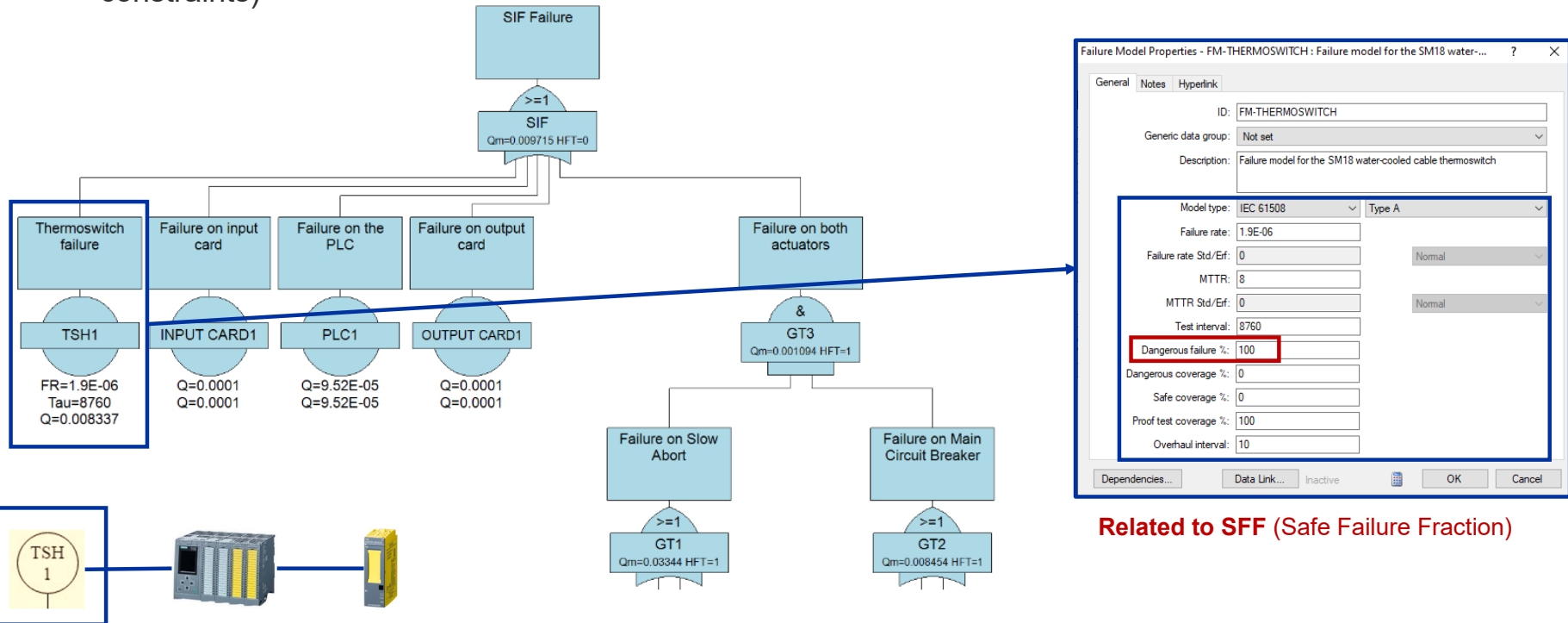
Phase 4 - SIS design and engineering (both)

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SIS design and engineering – Application Program (AP)

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- **Challenges:**

- Requirements to **design, implement** and **verify APs**

IEC 61511-1: 2016 Clause 12

SIS design and engineering – Application Program (AP)

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- Requirements to **design, implement** and **verify APs**

IEC 61511-1: 2016 Clause 12

- **Guidelines** (examples and recommendations)

IEC 61511-2:2016 Annex B

SIS design and engineering – Application Program (AP)

- **Challenges:**

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IEC 61511-1: 2016 Clause 12

- **Guidelines** (examples and recommendations)

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*“The traditional **text based approach of safety AP specification is not efficient** enough to handle the advanced, complex safety requirements commonly found in SIF specifications. The most efficient tool to address these challenges is the **Model-based design (MBD)**...”*

SIS design and engineering – Application Program (AP)

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*“... **specification** should be implemented in the **graphical language of the model checking workbench** environment...”*

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- **Adopted solutions:**

SIS design and engineering – Application Program (AP)

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IEC 61511-1: 2016 Clause 12

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*“... **specification** should be implemented in the **graphical language of the model checking workbench** environment...”*

- **Adopted solutions:**

- MBD for the **SRS** (Safety requirements Specification) - **phase 3** = logic to be implemented in the PLC:
 - **CEM** (Cause and Effect Matrix) – **SISpec** tool*
 - **LD** (Logic Diagrams) – **Grassedit** tool*
 - **Model Checking** for the PLC program verification – **PLCverif** tool*

*developed at CERN

SIS design and engineering – AP specification

SIS design and engineering – AP specification

CEM (Cause and Effect Matrix) - SISpec

More details: [MOPHA041](#)

Cause	Effect	SIF1
COM_1		A1,A2,A3,A4
CON_A		A1,A2,A3,A4
TSH1		NA1
TSH2		NA2
FSL1		NA3
FSL2		NA4

Cause	Effect	PC1_PP
SIF1		NA1
SIF2		NA1
SIF3		
SIF4		NA1
PC1_OPER		A1

SIS design and engineering – AP specification

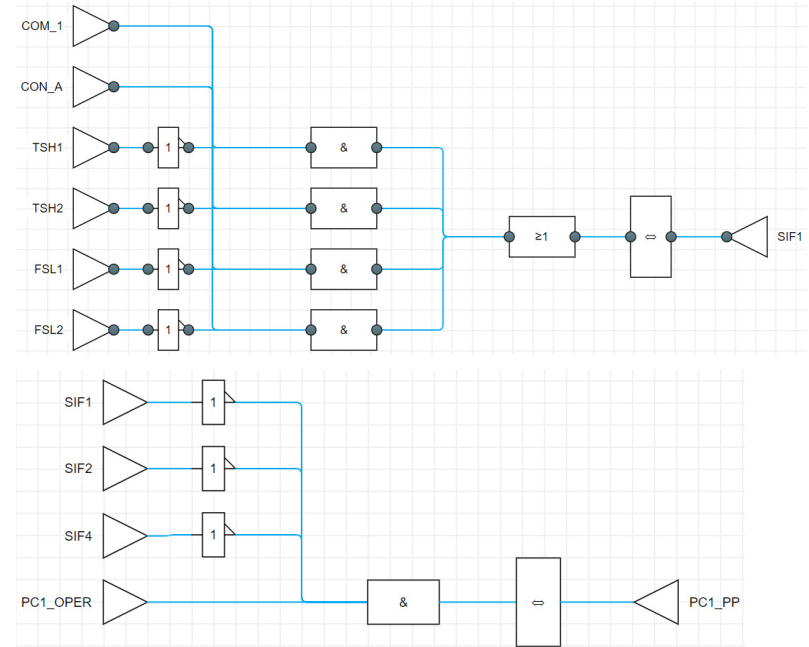
CEM (Cause and Effect Matrix) - SISpec

More details: [MOPHA041](#)

Cause	Effect	SIF1
COM_1		A1,A2,A3,A4
CON_A		A1,A2,A3,A4
TSH1		NA1
TSH2		NA2
FSL1		NA3
FSL2		NA4

Cause	Effect	PC1_PP
SIF1		NA1
SIF2		NA1
SIF3		
SIF4		NA1
PC1_OPER		A1

LD (Logic Diagrams) - Grassedit



Simulation, test and verification case generation and **code generation** is possible

SIS design and engineering – Application Program

SIS design and engineering – Application Program

AP specification

AP development

AP verification

SIS design and engineering – Application Program

AP specification

AP development

AP verification

SISpec

(a) Top Operational CEM			
Cause	Effect	PC1_OPER	PC2_OPER
SEL_PC1		A1A2A3A4A5	
SEL_PC2			A1
TEST_A		A1	
TEST_B		A2	A1
TEST_C		A3	
TEST_D		A4	
TEST_E		A5	
(c) Bottom Operational CEM			
Cause	Effect	TEST_A	TEST_B
SEL_TEST_A		A1	
SEL_TEST_B			A1
CRVO_A		A1	A1
CRVO_B			A1
DAQ_A		A1	
DAQ_B			A1

(b) Top Safety CEM			
Cause	Effect	PC1_PP	PC2_PP
SIF1		NA1	
SIF2		NA1	
SIF3			NA1
SIF4		NA1	NA1
PC1_OPER		A1	
PC2_OPER			A1
(d) Bottom Safety CEM			
Cause	Effect	SIF1	SIF2
COM1		A1A2A3A4	
CON_A		A1A2A3A4	
TSH1		NA1	
TSH2		NA2	
FSL1		NA3	
FSL2		NA4	

SIS design and engineering – Application Program

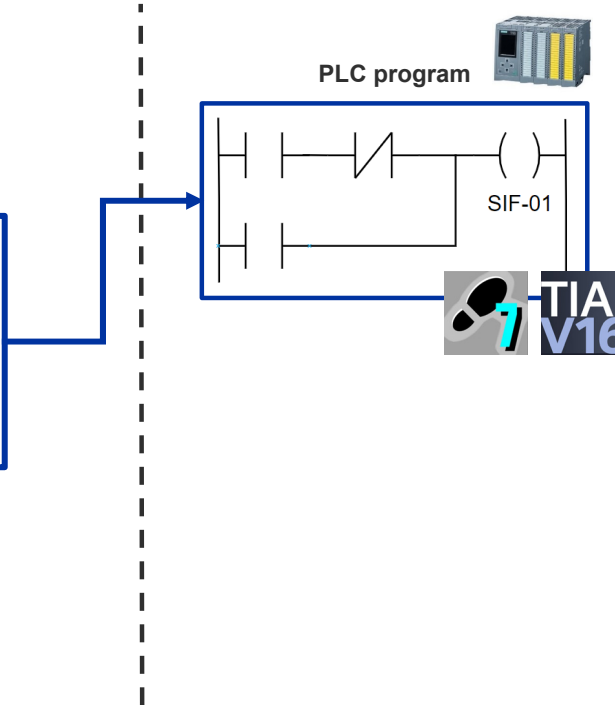
AP specification

AP development

AP verification

SISpec

(a) Top Operational CEM			
Cause	Effect	PC1_OPER	PC2_OPER
SEL_PC1		A1A2A3A4A5	
SEL_PC2			A1
TEST_A		A1	
TEST_B		A2	A1
TEST_C		A3	
TEST_D		A4	
TEST_E		A5	
(c) Bottom Operational CEM			
Cause	Effect	TEST_A	TEST_B
SEL_TEST_A		A1	
SEL_TEST_B			A1
CRVO_A		A1	
CRVO_B			A1
DAQ_A		A1	
DAQ_B			A1



SIS design and engineering – Application Program

AP specification

AP development

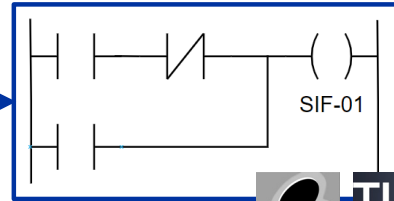
AP verification

SISpec

(a) Top Operational CEM			
Cause	Effect	PC1_OPER	PC2_OPER
SEL_PC1		A1A2A3A4A5	
SEL_PC2			A1
TEST_A		A1	
TEST_B		A2	A1
TEST_C		A3	
TEST_D		A4	
TEST_E		A5	
(c) Bottom Operational CEM			
Cause	Effect	TEST_A	TEST_B
SEL_TEST_A		A1	
SEL_TEST_B			A1
CRVO_A		A1	
CRVO_B			A1
DAQ_A		A1	
DAQ_B			A1

(b) Top Safety CEM			
Cause	Effect	PC1_PP	PC2_PP
SIF1		NA1	
SIF2		NA1	
SIF3			NA1
SIF4		NA1	NA1
PC1_OPER		A1	
PC2_OPER			A1
(d) Bottom Safety CEM			
Cause	Effect	SIF1	SIF2
COM1		A1A2A3A4	
CON_A		A1A2A3A4	
TSH1		NA1	
TSH2		NA2	
FSL1		NA3	
FSL2		NA4	

PLC program



Verification cases

```
//#ASSERT(  
(  
    NOT Inputs.In1 OR  
    NOT Inputs.In2  
)  
--> (Out1 = FALSE)  
): SIF01;
```

SIS design and engineering – Application Program

AP specification

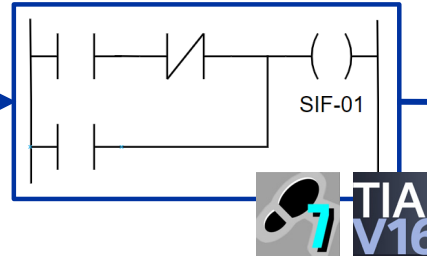
SISpec

(a) Top Operational CEM			
Cause	Effect	PC1_OPER	PC2_OPER
SEL_PC1		A1A2A3A4A5	
SEL_PC2			A1
TEST_A		A1	
TEST_B		A2	A1
TEST_C		A3	
TEST_D		A4	
TEST_E		A5	
(c) Bottom Operational CEM			
Cause	Effect	TEST_A	TEST_B
SEL_TEST_A		A1	
SEL_TEST_B			A1
CRVO_A		A1	
CRVO_B			A1
DAQ_A		A1	
DAQ_B			A1

(b) Top Safety CEM			
Cause	Effect	PC1_PP	PC2_PP
SIF1		NA1	
SIF2		NA1	
SIF3			NA1
SIF4		NA1	NA1
PC1_OPER		A1	
PC2_OPER			A1
(d) Bottom Safety CEM			
Cause	Effect	SIF1	SIF2
COM1		A1A2A3A4	
CON_A		A1A2A3A4	
TSH1		NA1	
TSH2		NA2	
PSL1		NA3	
PSL2		NA4	

AP development

PLC program



AP verification

Exported source code



Verification cases

```
//#ASSERT(  
(  
    NOT Inputs.In1 OR  
    NOT Inputs.In2  
)  
--> (Out1 = FALSE)  
): SIF01;
```

SIS design and engineering – Application Program

AP specification

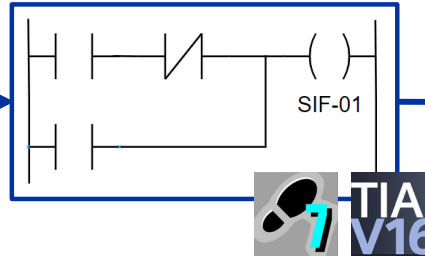
SISpec

(a) Top Operational CEM			
Cause	Effect	PC1_OPER	PC2_OPER
SEL_PC1		A1A2A3A4A5	
SEL_PC2			A1
TEST_A		A1	
TEST_B		A2	A1
TEST_C		A3	
TEST_D		A4	
TEST_E		A5	
(c) Bottom Operational CEM			
Cause	Effect	TEST_A	TEST_B
SEL_TEST_A		A1	
SEL_TEST_B			A1
CRVO_A		A1	
CRVO_B			A1
DAQ_A		A1	
DAQ_B			A1

(b) Top Safety CEM			
Cause	Effect	PC1_PP	PC2_PP
SIF1		NA1	
SIF2		NA1	
SIF3			NA1
SIF4		NA1	NA1
PC1_OPER		A1	
PC2_OPER			A1
(d) Bottom Safety CEM			
Cause	Effect	SIF1	SIF2
COM_1		A1A2A3A4	
CON_A		A1A2A3A4	
TSH1		NA1	
TSH2		NA2	
PSL1		NA3	
PSL2		NA4	

AP development

PLC program



Exported source code

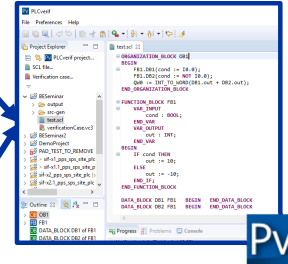


Verification cases

```
//ASSERT(
(
    NOT Inputs.In1 OR
    NOT Inputs.In2
)
--> (Out1 = FALSE)
): SIF01;
```

AP verification

PLCverif



SIS design and engineering – Application Program

AP specification

AP development

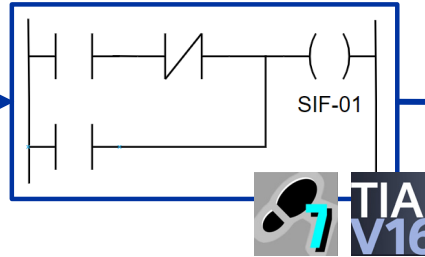
AP verification

SISpec

(a) Top Operational CEM			
Cause	Effect	PC1_OPER	PC2_OPER
SEL_PC1		A1A2A3A4A5	
SEL_PC2			A1
TEST_A		A1	
TEST_B		A2	A1
TEST_C		A3	
TEST_D		A4	
TEST_E		A5	
(c) Bottom Operational CEM			
Cause	Effect	TEST_A	TEST_B
SEL_TEST_A		A1	
SEL_TEST_B			A1
CRVO_A		A1	
CRVO_B			A1
DAQ_A		A1	
DAQ_B			A1

(b) Top Safety CEM			
Cause	Effect	PC1_PP	PC2_PP
SIF1		NA1	
SIF2		NA1	
SIF3			NA1
SIF4		NA1	NA1
PC1_OPER		A1	
PC2_OPER			A1
(d) Bottom Safety CEM			
Cause	Effect	SIF1	SIF2
COM1		A1A2A3A4	
CON_A		A1A2A3A4	
TSH1		NA1	
TSH2		NA2	
PSL1		NA3	
PSL2		NA4	

PLC program



Exported source code



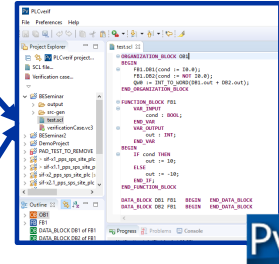
LADDER XML



Verification cases

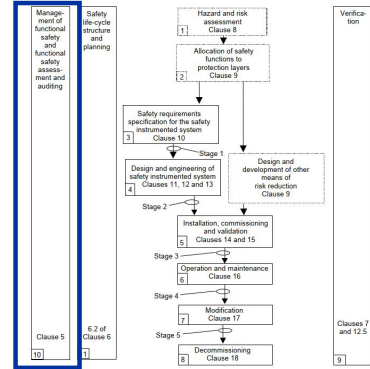
```
//ASSERT(
(
    NOT Inputs.In1 OR
    NOT Inputs.In2
)
--> (Out1 = FALSE)
): SIF01;
```

PLCverif



PLCverif more details:
<https://cern.ch/plcverif>
 MOPV042, WEPV042, etc.

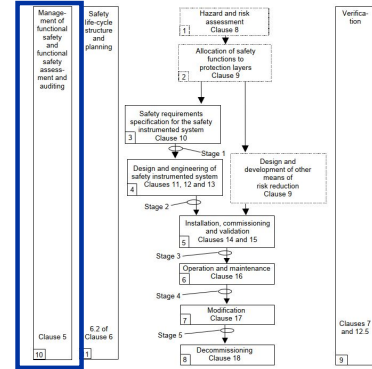
Phase 10 - Management of an FS project



Phase 10 - Management of an FS project

- **Challenges:**

- Define the **roles** and **responsibilities** of the project members
- Define the **workflow** and **documentation to coordinate all project members**



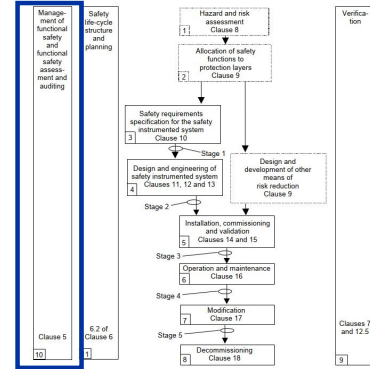
Phase 10 - Management of an FS project

- **Challenges:**

- Define the **roles** and **responsibilities** of the project members
- Define the **workflow** and **documentation to coordinate all project members**

- **Adopted solutions:**

- Definition of roles and responsibilities – ongoing work (**example** below)
- Report templates
- Functional Safety projects workflow – ongoing work



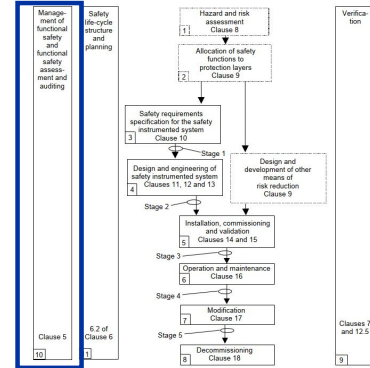
Phase 10 - Management of an FS project

Challenges:

- Define the **roles** and **responsibilities** of the project members
- Define the **workflow** and **documentation to coordinate all project members**

Adopted solutions:

- Definition of roles and responsibilities – ongoing work (**example** below)
- Report templates
- Functional Safety projects workflow – ongoing work



Role	Responsibilities
Functional Safety (FS) expert	Apply the FS standards
Process expert	Process knowledge and risk analysis
Instrumentation and controls expert	Design and implementation of the safety system
Departmental Safety Officer (DSO)	Risk graph calibration and safety support
Health & Safety and Environmental Protection (HSE) unit representative	Safety support and safety audits

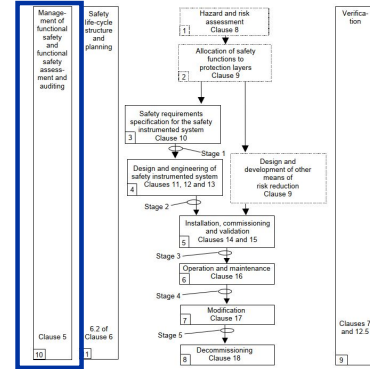
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Conclusions and future work

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Safety life-cycle phase	Tools	Methods	Report templates
H&R assessment	-	FMEA and calibrated risk graph	Risk assessment report
SRS	SISpec and Grassedit	CEM and Logic Diagrams	SRS report
Design and engineering	Isograph, PLCverif and UNICOS (future work)	FTA, RBD, model checking and FAT	Design and verification report
Validation	-	-	Proof test
Management	-	-	FSA and safety manual

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Future work:

- **Traceability** (explore commercial tools)
- **Workflow** procedures
- **Code generation** of application programs
- **Integration** in our frameworks (e.g. UNICOS)

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