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White Rabbit and MTCA.4 use in the LLRF upgrade for CERN's SPS

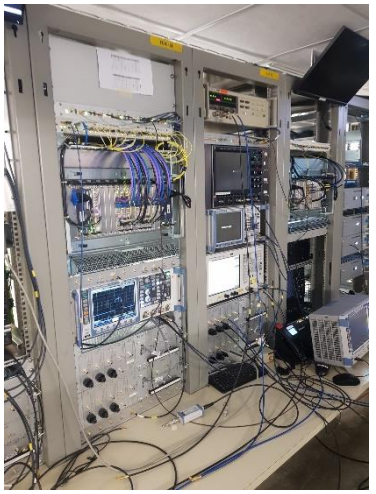
Zoom, 21 October 2021

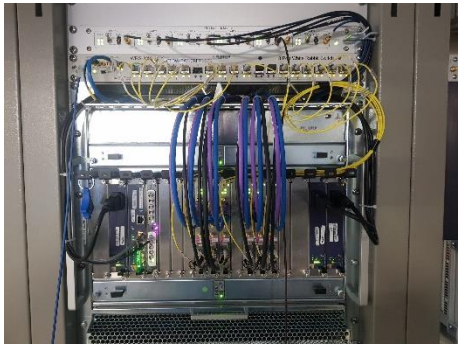
Background

- In 2016 a decision was taken to renovate the Low Level Radio Frequency controls in the Super Proton Synchrotron[1] at CERN
- The new system relies on distribution of the reference clock and RF signals over White Rabbit. In order to be able deliver beams of requested quality, the RF required:
- **< 13 ps end-to-end precision (reproducible every power cycle)**
- **-130 dBc/Hz PN at 1 kHz (223 MHz)**

The "old" analog LLRF system

WR-based LLRF

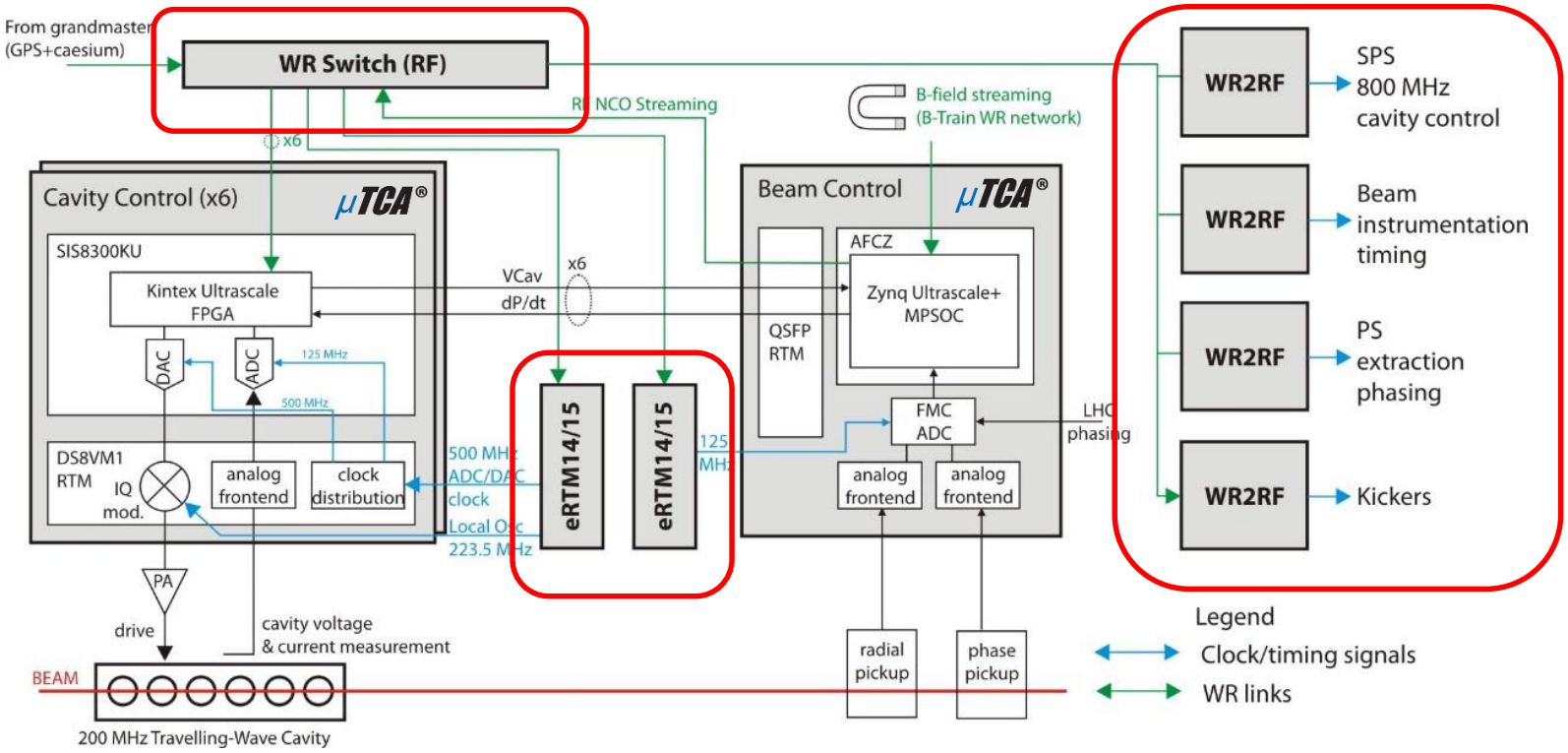




We had to deliver WR gear that can do that: **WRS-LJD, LPDC, eRTM, WR2RF**

[1] The second-largest accelerator at CERN (8 km circumference) and a direct injector to the LHC.

The LLRF System Overview



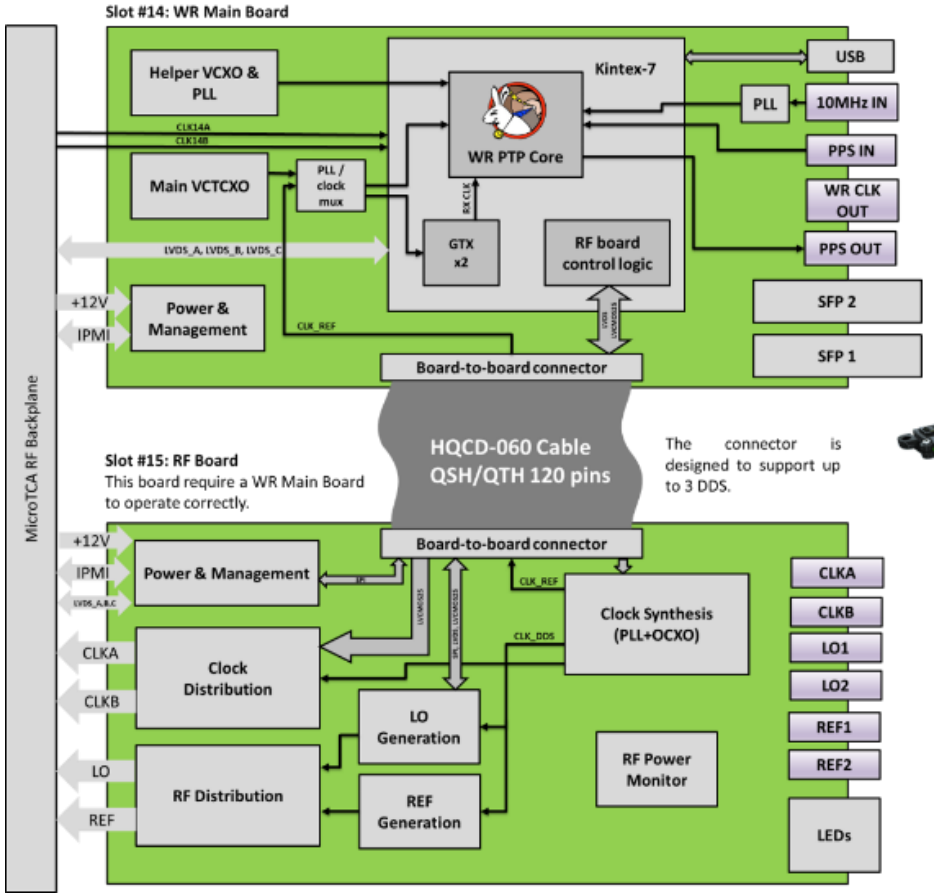
- **Cavity Controller** handles a single RF cavity (we have 6 in the SPS)
- **Beam Controller** calculates the RF frequency (called "RF-Train") and distributes it using WR Streamers
- The **CC** and **BC** reside in two **MTCA.4** crates, with the **LLRF backplane**

- The **eRTM** provides the Local Oscillator and ADC/DAC clocks for the CC/BC
- The **WR2RF** receives the RF-Train and can generate the actual cavity RF signals and RF-synchronous trigger pulses.
- **WRS-LJD** and **LPDC** allow for improved precision and PN

The eRTM14/15

MTCA.4 Rear Transition Module that fits in the MTCA LLRF backplane for low noise clock and RF reference distribution:

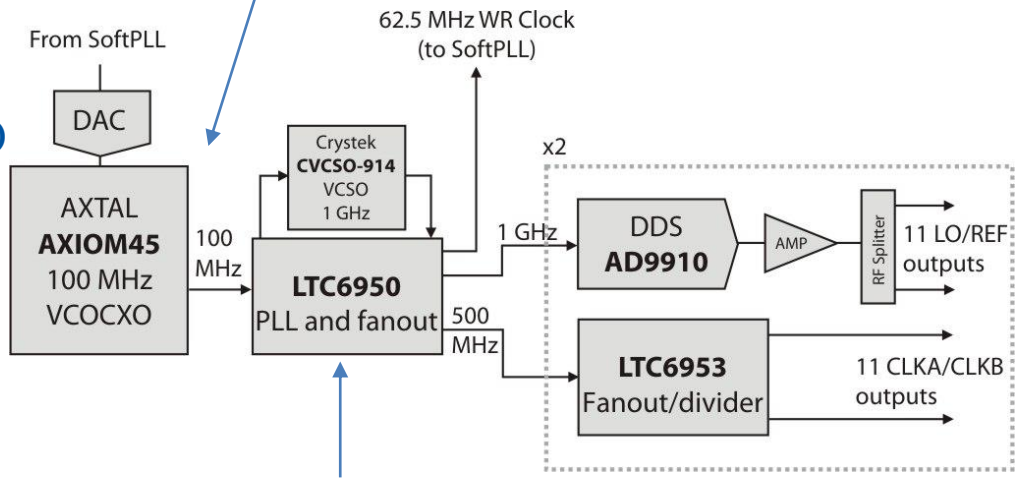
- "Sandwich" of two boards: digital with the FPGA and analog with the oscillators and clock distribution
- Kintex-7 7K70T FPGA
- Two DDS analog clocks LO and REF:
  - From 10 to 300 MHz, sine wave
  - 11 outputs for each (backplane + FP)
- Two digital clocks CLKA and CLKB:
  - 62.5, 125, 250 or 500 MHz
  - 10 outputs for each (backplane + FP)
- PPS and 10 MHz in/out
- Two WR uplink ports
- Software control over USB
- Stand-alone (no MTCA crate) operation possible



The eRTM14/15 Clock Recovery and Distribution

- LO output must have PN better than -130 dBc/Hz at 1 kHz offset @ 223 MHz
- This is above WR PLL bandwidth and PN figure offered by FPGA PHYs
- Must provide enough PN headroom for the DDS
- **Solution:** AXIOM45ULN 100 MHz OCXO
- DDS and digital clocks require ~100 fs rms jitter and a master clock of 1 GHz
- **Solution:** multiply using PLL + discrete oscillator combo (CVCSO-914-1000)
- 2nd PLL bandwidth = ~10 kHz
- PN at offsets below 10 Hz not critical (not "seen" by the beam)
- LO/REF outputs used for driving RF mixers (low-distortion sinewave), using an analog network of RF amplifiers and passive splitters

-100	dBc/Hz	@ 10 Hz
-135	dBc/Hz	@ 100 Hz
-162	dBc/Hz	@ 1 kHz
-172	dBc/Hz	@ 10 kHz
-175	dBc/Hz	@ 100 kHz

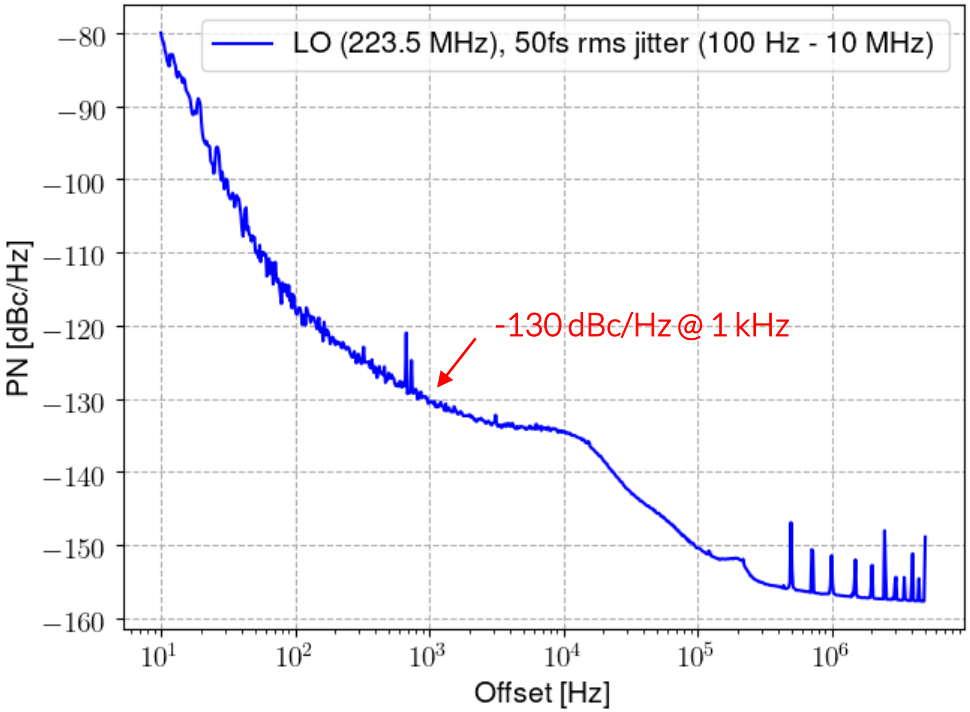


Phase Noise Typical:

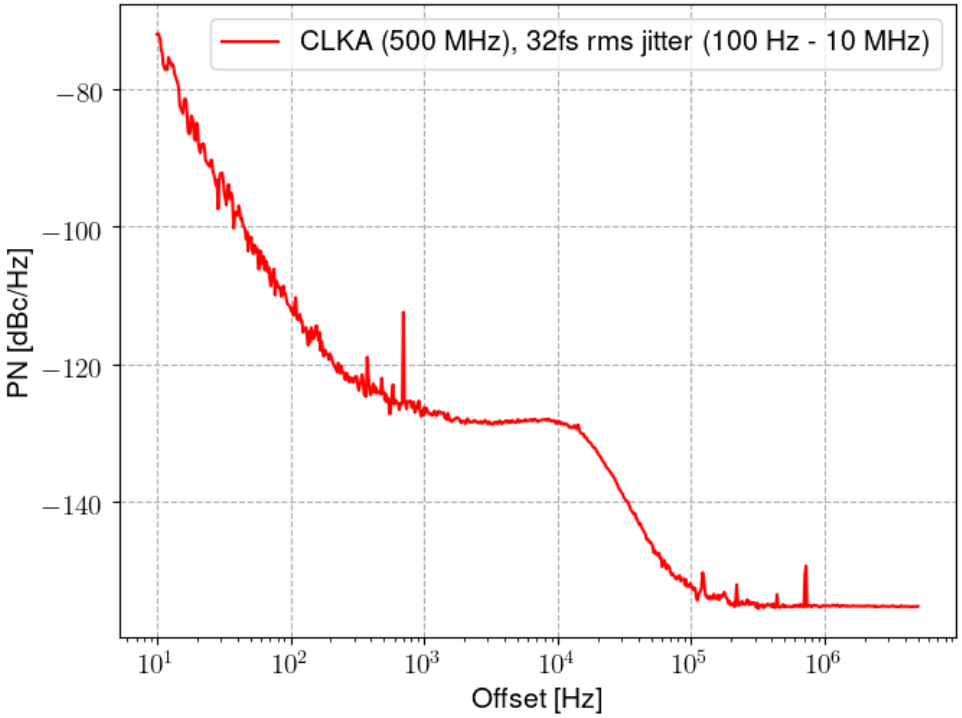
1kHz	**-110 dBc/Hz**
10kHz	**-139 dBc/Hz**
100kHz	**-160 dBc/Hz**
1MHz	**-170 dBc/Hz**
10MHz	**-174 dBc/Hz**

The eRTM14/15 PN measurements

LO (front panel) @ 223.5 MHz



CLKA (front panel) @ 500MHz



- DDS LO/REF PN of **-130.5 dBc/Hz** at 1 KHz (223.5 MHz), jitter **51 fs** (100 Hz – 10 MHz)
- CLKA PN of **-126 dBc/Hz** at 1 KHz (500 MHz), jitter **32 fs** (100 Hz – 10 MHz)
- Measured for front panel outputs of the eRTM14/15
- At these PN levels, even mechanical vibrations caused by cooling fans matter!

The WR2RF

VME64x card for interfacing the WR LLRF with the "analog" world

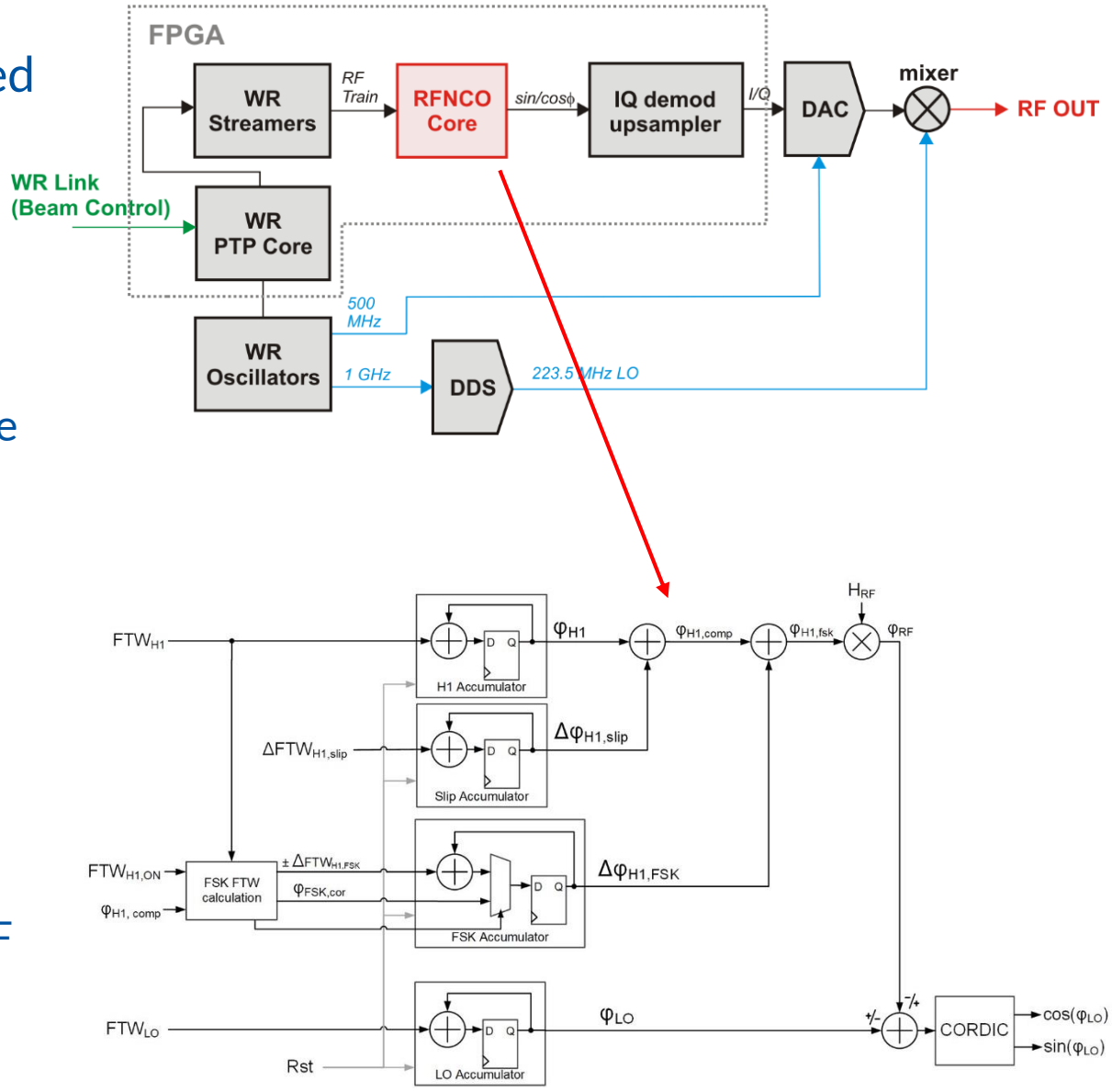
- Replaces expensive coaxial cabling with a single WR fiber
- WR Clock and DDS identical as in the eRTM board
- 2 independent RF outputs
- 250 MSPS 16-bit I/Q DAC followed by an upconverter
- Numerically Controlled Oscillator capable of reproducing the SPS cavities RF signal
- 2 low jitter Trigger Units per each RF output, generating pulse patterns synchronous with the RF (bunch clock, orbit clock or arbitrary pulses)
- A number of standard timing I/Os (PPS, 10 MHz, slow triggers)
- User API in C

Applications: driving systems that require beam-synchronous analog timing (instrumentation, kickers, synchronization with the Proton Synchrotron)

The WR2RF RF Synthesis

Based on the RFNCO core provided by the LLRF team

- A bit more complex than the „DDS over WR" idea presented in the past...
- Inputs momentary RF parameters (machine-specific) broadcast by the Beam Controller using the WR Streamers
- The NCO core computes the momentary RF phase and outputs *sin/cos* for the DAC
- External DAC and mixer produce the ultimate RF output
- Performance very similar to eRTM (-132 dBc/Hz @ 1kHz/200 MHz RF out)

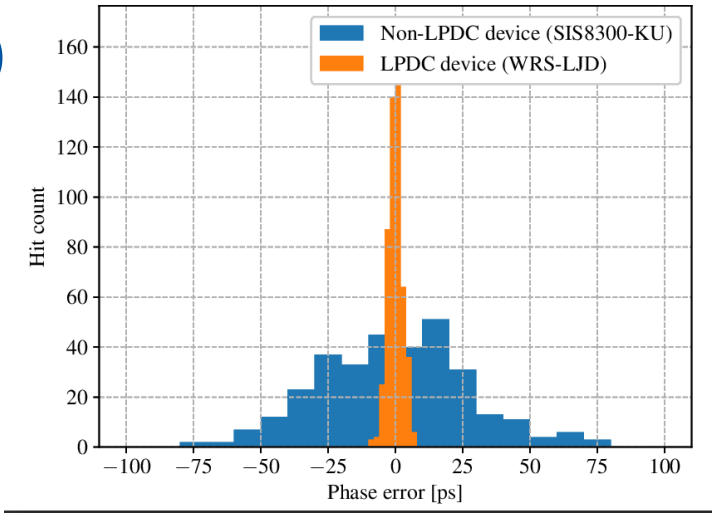


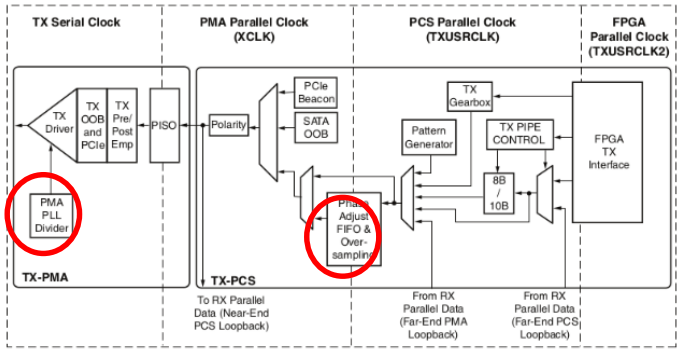
Drawings courtesy J. Gill, A. Spierer and G. Hagmann

Improving WR Precision

Goal: The RF system needs the phase reproducibility (power-cycle) better than 13 ps (1 degree at 200 MHz)

- "Standard" WR offers ~100 ps
- Most of this comes from the FPGA transceiver
- Two main sources of uncertainty:
  - Xilinx's TX/RX Phase Align logic
  - PMA bit clock -> PCS word clock dividers, where each 'tap' introduces slightly different phase offset
- Solution: **LPDC** (**L**ow **P**hase **D**rift **C**apable) ports:
  - Disable Phase Alignment
  - *Tom's Casino*[1] approach – keep resetting the TX/RX path measuring the phase of the clocks until it hits a predefined value (bypasses divider uncertainty)
- Currently available for GTXE1 (Virtex-6) and GTXE2 (Kintex 7 and Zynq-7000)
- Supported devices: WRS v6.0, eRTM, WR2RF-VME, SPEC7





[1] For more details/bibliography, see THBR02 paper. Name by Peter Jansweijer/NIKHEF ☺

Our experience with MTCA.4

The SPS LLRF was also the first application of MTCA.4[1] in the CERN Accelerator Sector – and as such came with some issues:

- NDA required to obtain the snippets of schematics from one of RTM vendors…
- Thermal design of the crate and fan units: eRTM14/15 slots and RPM slots overheating because of insufficient airflow
- Power Module firmware issues with powering and communicating with the LLRF RTMs
- Bugs in MCH firmware, such as non-functional configuration parameters
- CPU BIOS configuration (PCI Express) is very complex. Wrong settings can 'brick' the CPU module

After 4 months of intense collaboration with the vendors – all issues fixed

[1] Platform: Schroff/Nvent 11850-026 crate + LLRF backplane + NAT MCH/CPU/PMs

Conclusions

- Numerous new features for the White Rabbit ecosystem, enabling new areas of applications
- Vastly improved PN and phase reproducibility
- MTCA.4: proven platform (after some bugfixing)
- Fully digital LLRF system entirely relying on WR for synchronization and RF distribution, including driving the RF cavities in a large operational machine
- All components available as Open Source Software/Hardware on the OHR

Acknowledgements:

- Grzegorz Daniluk, Maciej Lipiński, Javier Serrano, Adam Wujek | Core WR Team
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