IMPLEMENTATION OF A VHDL APPLICATION FOR INTERFACING ANYBUS COMPACTCOM

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ICALEPCS 2021

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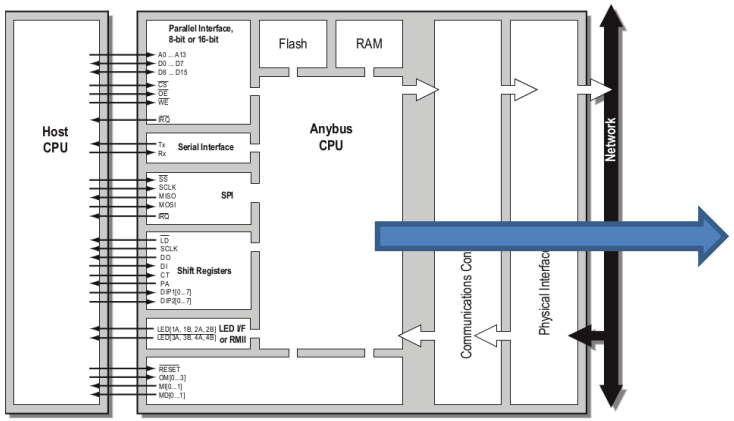
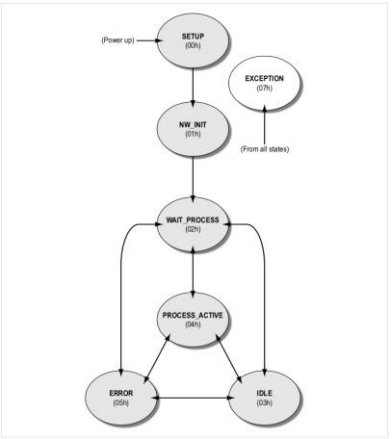
The Machine Protection System (MPS) at ESS must be fast and reliable and for this reason a Fast Beam Interlock System (FBIS) based on FPGAs is required.

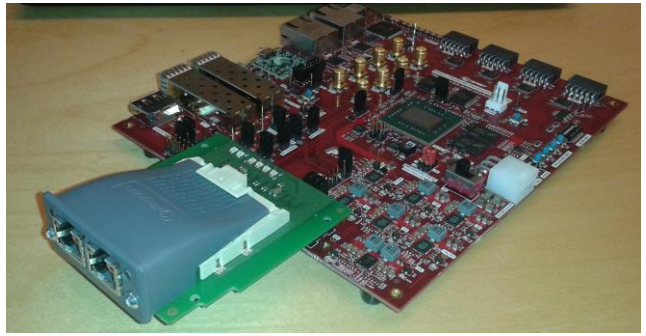
Some protection functions monitoring slow values are managed by PLCs

The communications protocol established between PLCs and FBIS is PROFINET fieldbus based. The Anybus CompactCom allows an host to have connectivity to industrial networks as PROFINET.





The code is written in VHDL. So far has been tested with two different hosts:



1) Xilinx Kintex UltraScale Development Kit 3, mounting a Xilinx XCKU040 FPGA.
2) Custom board SCS_1600 designed by IOxOS ounting an Zynq® UltraScale+™ MPSoC XCZU7EG-FFVF15174.

The maximum clock frequency tested was 250MHz.

The Xilinx XCKU040 utilization metrics is

LUT	LUTRAM	BRAM	DSP48	Max. Freq.
2170	21	0	0	250 MHz

The data decoded from one Anybus CompactCom is read by two different masters.

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- The complexity of the ESS machine (multiple beam destinations, beam modes, etc) requires not only transferring binary data from the PLC based interlock systems to the FPGA based Fast Beam Interlock System (Beam Permit OK/NOK), but also to transfer information on e.g. machine configuration, device location, etc..

- For that purpose, a so-called datalink has been implemented. It transmits data from the PLCs via PROFINET towards the FPGAs, using an intermediate commercial module, a CompactCom, which communicates via SPI with an ESS in-house developed firmware driver

- The implementation of this link was particularly challenging, as the CompactCom is designed to communicate with software entities like microprocessors, but not with FPGA firmware written in VHDL.

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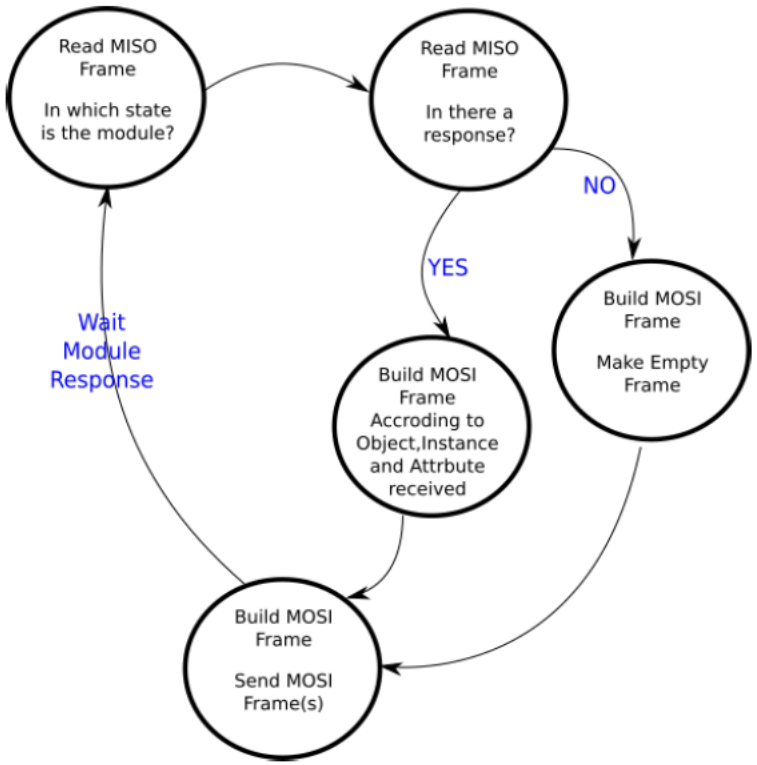

In each of its state a subset of the SPI FSM handles communication until the Anybus reaches the Process Active state in which the system becomes fully operational. This cyclic communication was needed to:

- keep the Write Process Data updated since this data is buffered by the Anybus CompactCom, and may be sent to the network after a state shift.

- catch the responses received by the Anybus CompactCom and according to the object, instance and attribute read, build the proper following command. In the case the firmware cannot catch the response an object error is sent back.

- send the commands. Depending on the type of commands one or more SPI frames have to be delivered to the Anybus CompactCom.

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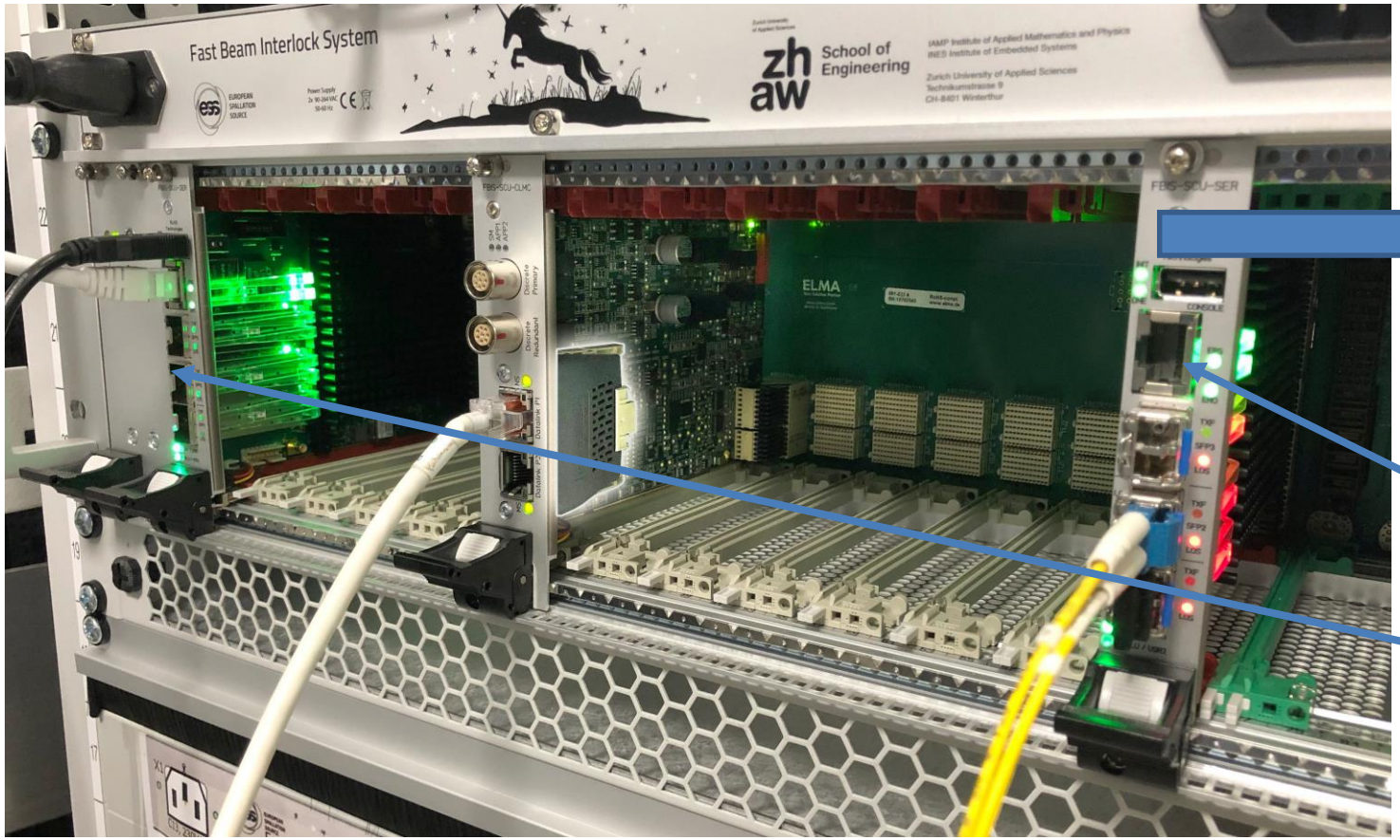

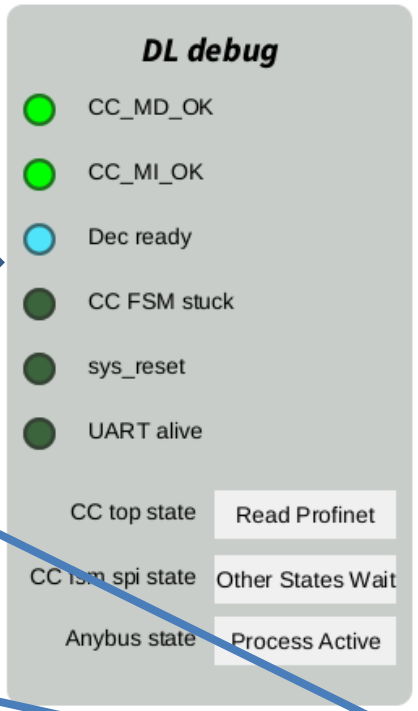

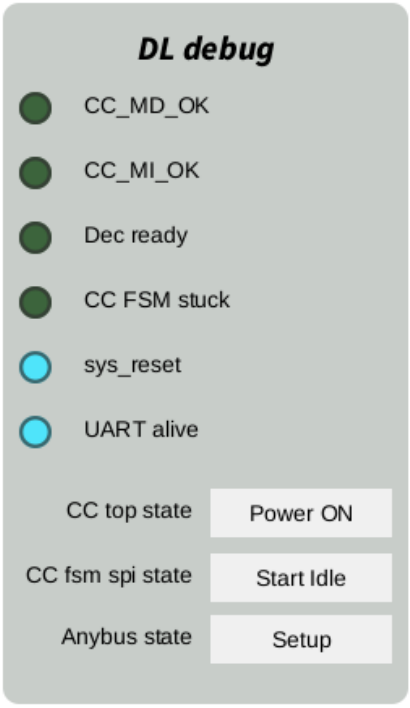

OPIs belonging to the two masters where the status of the Anybus CompactCom module is monitored.

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… and further improvements:

- So far only a limited number of objects are caught in the code. In case the module sends a command requesting an answer that is not foreseen in the host, this can lead to the Anybus state machine getting trapped in the Network Init or Wait Process state.

- Both masters communicate through UART to arbitrate which one interfaces the module. Now it's under investigation the opportunity to exploit the backplane Ethernet communication in order to replace the UART link.

- The communication with the Anybus CompactCom could be managed by both masters in parallel. As there is only slave, the CS is whatever always in use (tied to 0) and the arbitration just has to be managed between the masters, out of the SPI protocol.