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# THE FPGA-BASED CONTROL ARCHITECTURE, EPICS INTERFACE AND **ADVANCED OPERATIONAL MODES OF THE HIGH-DYNAMIC** DOUBLE-CRYSTAL MONOCHROMATOR FOR SIRIUS/LNLS

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## Abstract

DOI

The High-Dynamic Double-Crystal Monochromator (HD-DCM) has been developed since 2015 at Sirius/LNLS with an innovative high-bandwidth mechatronic architecture to reach the unprecedented target of 10 nrad RMS (1 Hz -2.5 kHz) in crystals parallelism also during energy fly-scans. After the initial work in Speedgoat's xPC rapid prototyping platform, for beamline operation the instrument controller was deployed to NI's CompactRIO (cRIO), as a rugged platform combining FPGA and real-time capabilities. Customized libraries needed to be developed in LabVIEW and a heavily FPGA-based control architecture was required to finally reach a 20 kHz control loop rate. This work summarizes the final control architecture of the HD-DCM, highlighting the main hardware and software challenges; describes its integration with the EPICS control system and user interfaces; and discusses its integration with an undulator source.

## **INTRODUCTION**

With performance numbers in the range of single nm and tens of nrad, the High-Dynamic Double-Crystal Monochromator (HD-DCM) is a high-end control-based beamline instrument for energy selection with fixed-exit monochromatic beam [1]. It has been developed at the Brazilian Synchrotron Light Laboratory (LNLS/CNPEM) for the 4th-generation Sirius light source [2] to be the first vertical-bounce DCM to reach, even in motion, 10 nrad RMS inter-crystal parallelism over the broad frequency range from 1 Hz to 2.5 kHz, representing improvements by factors between 3 and 100.

Due to its singular architecture, different aspects of the HD-DCM have already been detailed to the community: conceptual design, mechatronic principles and thermal management [3-5]; results of in-air validation of the core, together with system identification and control techniques in the prototyping hardware [6, 7]; offline performance of the full in-vacuum cryocooled system, including scans solutions [8]; dynamic modelling work, updated control design and FPGA implementation in the final NI's CompactRIO (cRIO) [9-11]; and calibration and commissioning procedures, together with the first experimental results with beam [12]. Here, updated schemes of the control system, as a result of operational maturity with two units at the MANACÁ and EMA undulator beamlines, and the emerging control-related strategies and bottlenecks concerning a holistic beamline operation are discussed.

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 $f_{ENG}(UND, HAR)$  $f_{VSV}(PTC)$  $f_{ENG}(BRG)$ fysy (BRG.GAP) XEN Figure 1: Simplified control diagram for the current HD-DCM integration at Sirius undulator beamlines.

# APPLICATION OUTLINE

The application, as currently implemented at the EMA and MANACÁ beamlines, can be briefly introduced via the simplified control diagram in Fig. 1. Planar undulators by Kyma have been provided for the early operation phase, before the definitive Delta undulators that have been developed in-house for Sirius become available. Then, due to the perspective of short-time replacement, only basic features have been specified. Indeed, running on Beckhoff controllers, the systems can be operated by the users only via a limited set (PV<sub>UND</sub>) of high level process variables (PVs) in the EPICS control system [13]. Complementary, the quadrature signal of the phase encoders have been derived to be used as the leading digital signals to the HD-DCMs, if desired.

The HD-DCMs can be defined by four main closed control loops running in NI's CompactRIO (cRIO) hardware. Firstly, BRG, with a bandwidth of 20 Hz, is responsible for controlling the angle of incidence of the beam on the socalled *first crystal*, for energy selection according to Bragg's law of diffraction. Then, GAP, PTC and RLL, with bandwidths between 150 and 250 Hz, are part of the so-called crystal cage (CCG), responsible for positioning the so-called second crystal with respect to the first one, so that fixedexit monochromatic outgoing beam can be maintained at



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different Bragg angles. The GAP controls the distance between the crystals, while PTC and RLL (for pitch and roll angles) control the inter-crystal parallelism. Due to a careful mechatronic architecture, in practice the originally *multipleinput-multiple-output* (MIMO) system can be statically decoupled, so that the loops may be addressed independently and simpler *single-input-single-output* (SISO) controller design techniques, such as loop-shaping, can be used (see [6, 10]).

The plants and controllers are represented as  $P_i$  and  $C_i$ , respectively, where *i* refers to UND, BRG, GAP, PTC and RLL. Each loop follows a reference  $r_i$  and provides a measurement  $y_i$ , being subject to actuator and plant disturbances, as well as measurement noise from sensors (encoders and laser interferometers). The most strict requirements for the HD-DCM are related to the errors ( $e_i = r_i - y_i$ ) for: BRG, which ideally should be limited to the sub-µrad range to preserve the energy selection; and, more critically, PTC, specified as 10 nrad RMS (1 Hz-2.5 kHz) to preserve the beam position over long lever-arms at the beamlines (see [3]).

The reference signals for the CCG loops are defined as nominal or calibrated (linear or non-linear) functions  $f_i$  of the Bragg angle, being more suitably derived from  $r_{BRG}$ , rather than from  $y_{BRG}$ , to prevent disturbances and noise contamination which would deteriorate the CCG performances. The reference  $r_{BRG}$  itself, in turn, may result from three possibilities, namely: a trajectory calculated internally in the cRIO just before motion, a real-time conversion from a leading signal, or a trajectory previously stored in a file in the cRIO, thus defining three operational modes (PV<sub>OPM</sub>).

The first is the stand-alone mode, in which the HD-DCM can be operated at a high level via EPICS PVs. With userdefined parameters, an internal block in cRIO generates a 3rd-order trajectory and  $r_{BRG}$  is updated accordingly to a target value. This is a basic mode for *stand-still* or *step-by-step* scanning experiments, either at bending magnet or undulator beamlines. In the latter case, as at EMA and MANACÁ, the undulator phase must be independently adjusted by the user, so that the appropriate tuning between its emission spectrum and the HD-DCM energy is assured for ideal flux and beam shape/size. Although not optimum in terms of timing, this can often be handled via standard step-scanning beamline pieces of software. Moreover, this would also be a straightforward option for the so-called *fly-scanning* continuous motion operation in bending magnet beamlines. Indeed, by reducing the previous state-of-the-art pitch parallelism levels at stand-still from about 50 to 10 nrad RMS, the HD-DCM can already provides more accurate beam delivery for a number of experiments, such as crystallography and imaging. Yet, it is by keeping these unprecedented high-performance numbers in fly-scans that scientific opportunities are created in spectroscopy, with typical experiment times reduced by up to one or two orders of magnitude for much higher throughput, and new strategies.

Next, in the *follower* mode,  $r_{BRG}$  is updated in real time as a nominal or calibrated function of a leading input signal, which can be either an external real-time trajectory generator or a direct instrument signal, such as the phase from an undulator source at an undulator beamline, which is the case for EMA and MANACÁ. Indeed,  $r_{BRG}$  can be completely determined by the undulator phase value, a desired harmonic number (PV<sub>HAR</sub>) from the emission spectrum, and energy-conversion functions  $f_{BRG}$ . Then, by controlling the undulator alone, the user would ideally obtain a well-tuned fixed-exit monochromatic beam over the whole energy range, allowing the fly-scan potential to be explored as well. Lastly, expanding flexibility in fly-scans and integration options, the HD-DCM can be potentially used in a *triggered* mode, in which arbitrary trajectories can be directly consumed from a file after a software or hardware trigger. At bending magnet beamlines, this would release boundaries

Lastly, expanding flexibility in fly-scans and integration options, the HD-DCM can be potentially used in a triggered mode, in which arbitrary trajectories can be directly consumed from a file after a software or hardware trigger. At bending magnet beamlines, this would release boundaries related to the embedded 3rd-order trajectory generator in the HD-DCM, while preventing complementary real-time external trajectory generators for customized profiles. At undulator beamlines, in turn, not only may it also open opportunities with respect to possibly limited profiles in undulator controllers — which is the case with the Kyma commissioning undulators —, but, more importantly, it creates additional integration options, other than the control-loop-based ones that define the follower mode. The price to be paid is that more advanced following and synchronization functionalities must be provided by the undulator system as well, which has been considered for the Delta undulators.

Finally, complementary performance indicators can be computed in real time to indicate compliance. Firstly, the virtual source vertical shift  $\chi_{VSV}$ , as a function  $f_{VSV}$  of the Bragg angle, the gap value and the pitch angle, is a useful figure, either in bending magnet or undulator beamlines<sup>1</sup>. Then, in undulator beamlines, such as EMA and MANACÁ, the mismatch  $\chi_{ENG}$  in energy tuning between the source and the HD-DCM, as a function  $f_{ENG}$  of the Bragg angle, O and the harmonic number and the phase, can be seen as a crucial parameter, particularly during fly-scans.

To conclude, as demonstrated in the *Results and Discussions*, it turns out that getting the measurement signal  $y_{UND}$  from the undulator currently brings significant practical limitations to the experiments, which, so far, have been nonideally mitigated with an undesired aggressive low-pass filter for the encoder signal. All of this shines light on the increasing complexity and interdependence among the several instruments in new-generation beamlines. In particular, the results presented here will serve as guidelines for a more adequate architecture with the forthcoming Delta undulators and/or for upgrades in Kyma's. The main issues and alternatives are discussed in the following sections, after a brief review of the HD-DCM control hardware and software.

# **CONTROL ARCHITECTURE**

During the prototyping phase, the HD-DCM mechatronic concept was validated in a rapid control prototyping tool in

<sup>&</sup>lt;sup>1</sup> An indicator for the lateral shift of the virtual source  $\chi_{VSH}$  could be computed as well, but, it has a more complex dependence on the Bragg and roll angles and, fortunately, is not a critically sensitive parameter.



Figure 2: HD-DCM control architecture.

a real-time target machine from Speedgoat [7] – in which, besides preliminary operation, essential functionalities, such as plant identification and controller design via loop-shaping, were also developed [6]. To summarize the architecture, the FPGA layer was responsible for input and output drivers, while complex calculations were handled by its powerful processor at the real-time operating system (RTOS). However, in spite of being very flexible for rapid prototyping, this platform is not intended for reliable continuous operation, as demanded in a beamline environment. Therefore, NI cRIO was chosen as the standard controller for Sirius beamlines due to its industrial applications certifications and wide range of hardware modules, among other reasons.

The first architecture proposed for the control platform migration to cRIO was, naturally, the same one used in the Speedgoat xPC, but benchmark tests [11] revealed that the cRIO processor could not calculate the control loops sufficiently fast to meet the mechatronic requirements – namely, the high order controllers should run in a 20 kHz deterministic loop. Hence, an alternative approach with the whole control loop placed in the FPGA defined the final control architecture, which, as illustrated in Fig. 2, can be divided in three layers: FPGA, RTOS and Host Computer

Due to the results of the benchmark tests (see [11]), all the critical deterministic tasks are implemented in the FPGA layer. The *sensor drivers* are composed of decoders for BiSS-C absolute encoders, and incremental encoders and interferometers. Then, since the quadrature incremental signals demand high acquisition rates – specially when nanometric resolution is combined with relatively high velocity specifications –, the high frequency sensing noise is attenuated by decimation (or downsampling) from 10 MHz to 20 kHz in the *average filter*. Next, the *forward kinematics* converts individual sensor measurements into control coordinates, completing the feedback signal processing.

The reference signal depends on the selected operating mode. In the *stand-alone* mode, trajectories are first generated in the RTOS and internally executed by the *synchronization triggers* in the FPGA. Then, in the *follower* mode, the current integration architecture (see Fig. 1) is such that

the *follower setpoint* calculates the BRG reference as polynomial functions of the averaged undulator encoder. Finally, in the *triggered* mode, trajectory files, previously generated via *Python scripts* and loaded in the cRIO memory (RTOS), are executed according to internal or external triggers that are managed by the *synchronization triggers* in the FPGA.

Once the reference and feedback signals are processed, the FPGA *controller* block can be executed. This implementation is particularly challenging because of the high-order controllers, broad numerical ranges, and high-resolution demands, especially in calculations. Hence, a new controller deployment workflow was created for standardization and reliability purposes, as described in next section. To complete the feedback control loop, the *inverse kinematics* distributes the forces and torques from control coordinates to actuator actions, which are passed by the *actuator drivers* to 3-phase brushless, stepper and voice-coil motors<sup>2</sup>. Complementary, two additional features implemented via FPGA FIFOs (first in, first out) are: a bidirectional *user interface* and a triggered *data acquisition* lossless logger for files.

Next, since all time-critical features are already addressed at the FPGA, no deterministic task relies on the RTOS layer, which is, then, used to manage four main tasks, namely: 1) the RTOS side of the *user interface*; 2) the *EPICS IOC* server implemented via *Nheengatu* [14] (further discussed in the following sections); 3) the generation or loading of *trajectories*; and 4) the RTOS side of the *data acquisition* file logger. Finally, working as an EPICS client, the Host Computer layer is responsible for providing user-friendly graphical interfaces (GUIs) and more sophisticated operational routines via Python scripts or Jupyter Notebooks, as discussed in more detail in the following sections.

# Matlab-LabVIEW Integration Toolbox

The most challenging step for executing complex calculations in an FPGA is the trade-off between multiple hardware resources and timing constraints, like FPGA slices, memory blocks, lookup tables, Digital Signal Processors and timing violations, while taking care of the integrity of the results and proper numeric representations. That is the case in the HD-DCM controller, in which five SISO controllers<sup>3</sup>, with up to 16 states each, process data at high loop rates and deliver forces and torques for a nanometric-precision motion control system.

Therefore, aiming at achieving a standardized procedure, a new workflow was defined, as depicted in Fig. 3. The first six steps are performed in Matlab and Speedgoat environments, whereas the last two using LabVIEW and cRIO: 1) *Plant identification*: stimulus and response analyses for system identification using *multisine* techniques. 2) *Loopshaping controller design*: phase-margin and gain-margin analyses, with high low-frequency gain for disturbance attenuation and low high-frequency gain for noise rejection.

<sup>&</sup>lt;sup>2</sup> The stepper motor is used in the long-stroke stage for the GAP, not discussed here for conciseness. For more details, see [3, 8].

<sup>&</sup>lt;sup>3</sup> Again, the complementary long-stroke control loop was left out of Fig. 1 for the sake of clarity, but it, indeed, consumes resources in the hardware.

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Figure 3: HD-DCM FPGA controller design and deployment workflow.

3) Robustness analysis: analyses of plots of open-loop Bode, Nyquist, sensitivity and characteristic loci for robustness and SISO validations. 4) Conversion to FPGA data types: reduction of high order controllers into lower order ( $\leq 4$ ) transfer functions to preserve the transfer function integrity, with the required numeric representation reduction from double-precision floating point to single-precision floating point. 5) FPGA controller validation: testing of all transfer functions after data type conversion, to check if the increased quantization errors cause undesired changes in the dynamic system behaviour (Bode plot) (see [11]). 6) Export from Matlab to LabVIEW: file generation for exporting the transfer functions coefficients with no data loss. 7) Deployment to FPGA: updating of the multiple transfer function coefficients as constants into FPGA bitstream, as part of the strategy for saving hardware resources. 8) Machine tests: closed-loop controller validation using the real hardware, and performance analyses for compliance with specifications.

# EPICS and Python

With the appropriate hardware, and low- and mid-level architectures validated in cRIO, an essential feature for the high-level user operation was having the HD-DCM control system compatible with EPICS, such that the day-to-day beamline work can be based on user-friendly graphical interfaces, or robust and efficient scripts.

With the standardization of the cRIO at Sirius beamlines, the Nheengatu solution has been internally developed by the Beamline Software Group (SOL) to integrate EPICS with cRIO (see [14]). In the HD-DCM, it is used for publishing cRIO variables as PVs in an EPICS IOC server running in the RTOS, as shown in Fig. 2. This occurs via two different communication interfaces, namely: inter-process communication for RTOS PVs; and NI's FPGA Interface C API for direct access to FPGA PVs. Most PVs are accessed through RTOS, except for the time-critical ones, like software triggers used for motion or data acquisition.

As a side note, it is worth mentioning that, although the architecture for time-critical PVs avoid delays related to realtime software processing, memory sharing between RTOS and FPGA, and also FPGA processing, it is important to keep in mind that the standard update rate in the EPICS server is only 10 Hz. So, hardware triggers are also essential for fast integration and synchronization at the beamline, having been implemented for low latency synchronization (update rates up to 9 MHz) for compatibility with the TATU FPGAbased solution that was also recently developed by the SOL group for Sirius beamlines [15] (see also [12]).

Next, the framework used to build the EPICS GUI is called PyDM (Python Display Manager) [16], which is based on PyQt and includes a variety of widgets (plugins) for QtDesigner for building GUIs that communicate with EPICS PVs. Besides these widgets, customized Python routines were also added to the GUI project for more specific behaviors. The main advantage of using PyDM is the possibility of rapidly assembling control system GUIs connected to EPICS PVs, and adding code when necessary in a natural, pythonic way. Also, PyDM has been widely used at Sirius for beamline operation GUIs, thus, knowledge, objects and routines could be reused for the HD-DCM GUI.

Then, to automate, standardize and speed up procedures and operations with the HD-DCM, several sets of Python scripts and Jupyter Notebooks have been developed. The structure is flexible, such that many tasks can be scripted independently, simply addressing EPICS PVs for different purposes. Yet, a more controlled Python library has also been created to handle generic tasks and sub-tasks, as well as essential routines and procedures. Among the most important library procedures are: homing, for machine start-up, which previously required trained human operation via GUI, but now can be executed robustly by any user via a script in only 3 minutes; and calibration routines with the X-ray beam, such as tuning with respect to the undulator and fixed-exit refinement (see [12]).

### **RESULTS AND DISCUSSIONS**

For higher positioning accuracy and scanning throughput, the HD-DCM mechatronic architecture is based on what has been developed over the last decades for lithography machines in the semiconductors industry [17]. Now, to investigate the integration of the HD-DCM at the beamlines, examples in that field can also be explored as general references. Indeed, in [18], the leader-follower configuration for the reticle with respect to the wafer stage is conceptually equivalent for the HD-DCM with respect to the undulator in Fig. 1. However, fundamental differences can also be listed, including: type of motion; setpoint levels; and repeatability of tasks, motivating continued research.

One basic issue in adapting the strategy in [18] – i.e. with the measurement signal as input to the follower stage - to the HD-DCM is that there the wafer stage is also an ultralow-noise nanometer-level system, whereas the undulator is an instrument that performs at the micrometer-level. Indeed, Kyma's encoder has a resolution of 0.5 µm, such that  $y_{UND}$  in Fig. 1 contains already a variation of a few microns peak-to-peak from quantization noise alone. When this is coupled to the HD-DCM,  $r_{BRG}$  becomes a signal with broad-

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Figure 4: HD-DCM inter-crystal pitch (PTC) control error in stand-still condition at the EMA beamline at Sirius.

band noise reaching several µrad even at stand-still, critically deteriorating the HD-DCM closed-loop performance.

An example is given in Fig. 4, with measurements made at 6 keV at the EMA beamline, comparing the PTC control error in stand-alone and (low-pass filtered) follower modes. It can be seen that even with a Butterworth corner frequency as low as 2 Hz the RMS value is increased by about 20%, marginally respecting the desired spec of 10 nrad RMS. In this sense, some improvement can be expected by increasing the resolution of the encoder, thus reducing the noise background. Yet, this action alone would hardly completely solve the problem, because  $y_{UND}$  also captures the dynamics of the closed-loop undulator system, which may not have a sufficiently high performance due to its limited bandwidth and mechanical architecture.

Consequently, following y<sub>UND</sub> during motion for fly-scans makes the problem even worse, as the disturbances in the undulator are increased. Another practical issue is that the low-pass filter adds delay to the reaction of the HD-DCM, detuning the emission spectrum and the Bragg angle, which may reduce the beam flux and/or distort its shape. A sensitivity analysis for tolerable margins for  $\chi_{ENG}$  (not shown here due to space limitation) has been carried out via X-ray simulation tools by the Optics group, resulting in margins as low as  $\pm 4 \,\mu m$  for 10% increase in the beam full width at half maximum (FWHM). Within this budget, metrology accuracy, motion control errors, and delay effects must be considered. Hence, with typical motion errors measured within  $\pm 2 \mu m$  peak-to-peak (at least for velocities up to a few hundred µm/s) and the operation filter currently set 2 Hz, undulator velocities would be limited between 25 and 500 µm/s (depending on the undulator phase and harmonic) (if other errors are neglected). This translates to maximum scan speeds between 40 and 100 eV/s, which are at least 10 to 50 times slower than what can be expected under improved conditions, or in bending magnet beamlines.

This delay offset can be partly compensated via calibration, but practical limits are quickly found for more aggressive setpoints. Therefore, the ideal scenario probably involves directly extracting  $r_{UND}$  as the leading signal from the undulator controller, or making the undulator control system

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Figure 5: Virtual source vertical shift indicator  $\chi_{VSV}$  in flyscans of 1 keV at the EMA beamline at Sirius.

also capable of operating as a follower. Another alternative consists in linking the two systems solely via synchronized triggers, requiring that compatible trajectories be loaded in the different systems and executed accordingly. All these options are under investigation, but none of them are directly available with the current undulator solution. Still, in all cases, suitable velocity, acceleration and jerk parameters should be carefully identified to preserve performance.

An example of the fly-scanning capabilities is given in Fig. 5. The virtual source indicator  $\chi_{\rm VSV}$  is shown in follower mode for scans of 1 keV around 9 keV at the third harmonic of the Kyma undulator at the EMA beamline. Results for simulated smooth reference-based signals at different velocities and real encoder-based signals filtered at 2 and 5 Hz at the lower velocity are compared with 10% of the vertical beam size FWHM. The time axis has been normalized for readability, with the actual scans taking between 4 and 12 seconds. In the reference set, the peak-to-peak error increases by a factor 3 as larger speeds are associated with larger disturbances, yet, the standard deviation remains within to 10% of the beam size. In the encoder set, however, rougher setpoints and noise make the standard deviation exceed the margin even for the 2 Hz filter, which becomes worse with 5 Hz.

## **CONCLUSION**

The efforts in designing and implementing the High-Dynamic DCM, as a high-end mechatronic machine at Sirius beamlines, have been rewarded with unmatching stand-still performance and scanning capabilities. The control framework relies on a complex multi-system architecture, which has been gradually optimized, from the FPGA drivers to the user experience and automatic calibration routines in Python/EPICS. Now, global integration bottlenecks start to be revealed, stimulating a more holistic approach towards beamline operation.

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