UPGRADED BEAM INSTRUMENTATION DAQ FOR GSI AND FAIR: OVERVIEW AND FIRST EXPERIENCES

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Abstract

As construction of the **FAIR** accelerator complex progresses, the existing heavy ion synchrotron SIS18, the storage ring ESR and the high energy beam transfer lines HEBT have been upgraded to the future **FESA** based **control system**. Within this upgrade the **Beam Instrumentation** (BI) data acquisition systems (**DAQ**) have been heavily modernized too. These are now integrated into the control system with its **White Rabbit** based timing system, data supply (i.e. ion species, energy, etc) and services like archiving. Dedicated clients running in the main control room allow visualization and correlation of the data and status of the BI devices. The DAQ hardware has been upgraded using new state-of-the-art components. With a trend to slowly phase out **VME** based systems, solutions based on standard **Industrial PC** for few channels as well as on the new **microTCA** standard for many channels have been successfully implemented. This contribution will give an overview over the upgraded BI-DAQ systems like current transformers and counter applications for ionization chambers, scintillators and more. It will also present first experiences during beam operation with the new control system, which started summer last year.

Fig. 1: FAIR construction is progressing well. Here an aerial view on the SIS100 excavation. Mai 2019, Photo: D.Fehrenz/GSI/FAIR

FAIR will provide:
primary beams:
up to 35 GeV/u Uranium
up to 90 GeV/u Protons

secondary beams:
- broad range of radioactive beams
- antiprotons 0 - 30 GeV

storage and cooler rings:
- radioactive beams
- 10^{11} stored and cooled 0.8 - 14.5 GeV antiprotons

- very high diversity
- all elements from p to U
- parallel beam operation

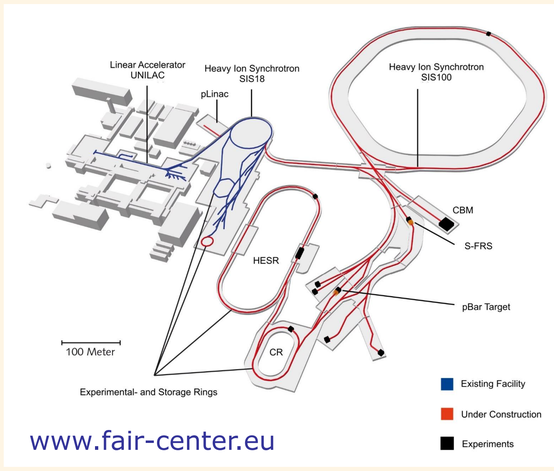

Fig. 2: Scheme of existing GSI (blue) and the new FAIR accelerators (red) plus attached experiments (black)

Control- and Data Acquisition System:

Three tier architecture (derived from CERN)

- Front-End: **FESA** / CentOS 7
- Middleware: CMW based on ZeroMQ
- Applications:
  - Java/JAPC (Java API for parameter control)
  - JavaFX
  - LHC Software Architecture (LSA) for settings management
- **White Rabbit** based timing system
  - Timing Receivers in PMC, AMC, PCIe, and VME
  - Sub-nanosecond synchronization
  - Connecting many nodes (~2000)
  - Long distances (up to 10km) between nodes
  - Fully open hardware, firmware and software

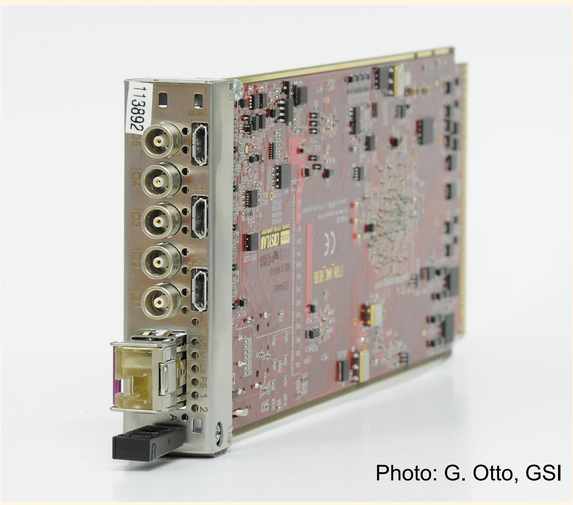

Fig. 3: Fair Timing Receiver (FTRN-AMC) in microTCA form-factor.

Beam Instrumentation Intensity Measurement

AC Current Transformer (ACCT)

Fig. 4: Transmission monitoring of UNILAC beam, here 40µs macro-pulses (top) to SIS18 synchrotron. Red curve shows the ideal efficiency, blue bottom graph shows the measured increase of intensity in the ring.

ACCT DAQ:
- IndustrialPC, 16-Bit Spectrum M2i.4963-Exp ADC, 64-Ch APCIe-1564-5V I/O, Pexaria (FTRN-PCIe)
- Standard arm-trigger-readout cycle
- HW trigger from FTRN on beam injection event
- baseline detection and subtraction
- Gate preparation (FTRN) for pre-amp

DC Current Transformer (DCCT)

Fig. 5: Intensity plot in number of particles (top) and beam current (bottom) in SIS18 using a DCCT.

DCCT DAQ:
- Same as for ACCT
- Continous readout (free running) with special DMA and I/O option of ADC module to sample timing signals into the data stream. Requires 2 Bits from ADC samples.
- FTRN software event for time stamping

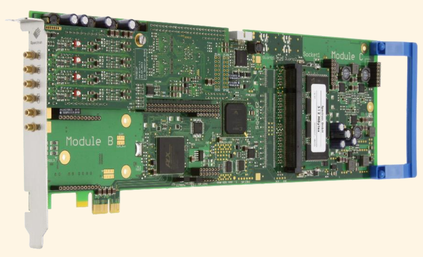

Fig. 6: High flexible Spectrum ADC, Model M2i.4963-Exp in PCIe form factor for IndustrialPC.

Photo: spec.de

Counters

Sampling of countable pulses from:
- Ionisation Chambers using IFC*
- Secondary Electron Monitors using IFC*
- Plastic Scintillators
- Virtual signals like rf, magnet ramps etc. using IFC* or UFC*

* IFC=Current to frequency converter
* UFC=Voltage to frequency converter

- Mixed form factors: VME and microTCA
  1. VME SIS3820 Scaler, GE VR12 CPU
  2. microTCA SIS8800 Scaler with SIS8980 Leading Edge discriminator RTM, CCT AM902 CPU

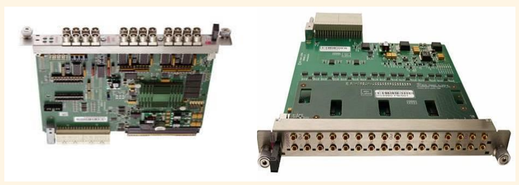

Fig. 7: MTCA.4 SIS8800 Multi Purpose Scaler und SIS8980 RTM Discriminator

Photo: struck.de

LASSIE (Large Analog Signal and Scaling Information Environment)

- JavaFX framework
- Collection of applications to show and correlate data from different free-running systems (Counters, ADCs etc.)
- Data as function of time, continous update data, trending, display of integral values, data analysis (FFT, cross-correlation etc.)

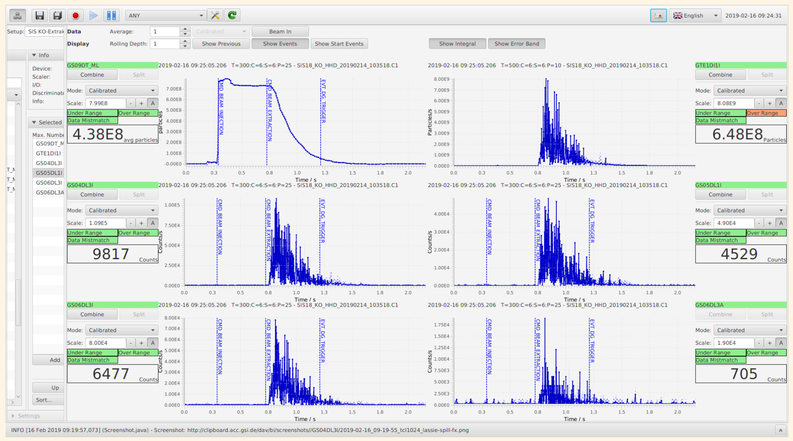

Fig. 8: Synchronous visualization of different acquisition types (ADC, scaler) in LASSIE of a complete SIS18 cycle. Upper left: Intensity in SIS18 (ADC). Upper right: slowly extracted beam in HEBT on plastic scintillator. All others graphs are in-ring beam boss monitors.

Profile Measurement (CUPID)

- GbE based Video Imaging
- IDS uEye CMOS GbE Cameras
- Pentax C1614ER and Linos MeVis Cm16 lenses with fixed focal length and remote controlled iris
- RadHard Cameras: CID based CCIR MegaRad3 (Thermo-Fischer) with Pleora frame-grabber

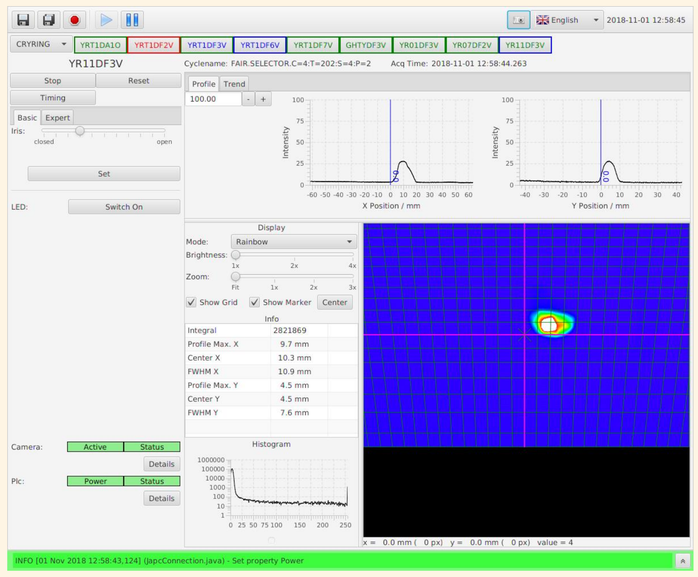

Fig. 9: Video imaging with CUPID for beam profile measurement on scintillating screens

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