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A/D and D/A Processing Unit for Real Time Control of Suspended Masses in Advanced Virgo Interferometer

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Abstract:

Advanced Virgo is the project to upgrade the Virgo interferometric detector of gravitational waves and has been completed in 2017, allowing Virgo to join with LIGO in an observation state and the creation of the first network of three gravitational wave detectors. The goal of Advanced Virgo is the detection of gravitational waves. A major upgrade consisted of the design of a new control electronics of the seismic isolation systems called Super-Attenuators. We present a new compact A/D-D/A conversion and processing unit used in the Advanced Virgo control electronics upgrade. The unit consists of an analog to digital conversion stage that samples the input signals. One Altera Cyclone IV GX FPGA that collects, pre-processes and sends data to a Texas Instruments TMS320C6678 DSP using a PCI Express GEN2 link with 2 lanes at 2.5 Gbps. The DSP processes data and sends outputs to the FPGA for feeding the digital to analog conversion stage. The unit is equipped with six low noise and distortion 4 MSPS - 24-Bit A/D converters and six low noise and distortion 24-Bit D/A converters with sampling rates up to 640 kHz in Direct Stream Digital (DSD) mode and 384 kHz in PCM mode. Two FPGA transceivers are used for PCI Express link while a third one is used for a custom data transmission optical link. The TMS320C6678 is a multi-core fixed and floating point architecture DSP, with eight cores running at 1.25 GHz. The unit has a dedicated input to interface directly to GPS timing signals. It is pluggable into a standard MicroTCA backplane. Using multiple units, sharing the same MicroTCA backplane and communicating via up to 4 Serial RapidIO lanes at 5 Gbps, it allows composing a flexible and modular system with a large number of channels suitable for the Advanced Virgo control electronics.

Introduction

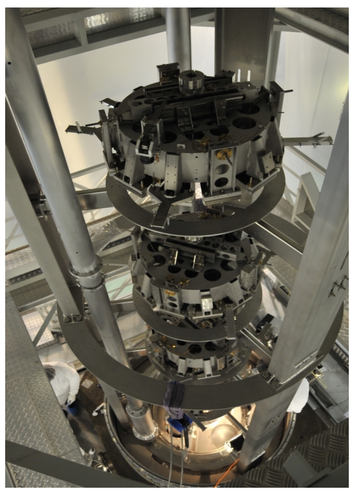
Modern astrophysics detectors, such as LIGO and Virgo, have been upgraded to increase the detection rate by three orders of magnitude. The goal of Advanced Virgo is the detection of gravitational waves, discovered with the first LIGO-Virgo detection of a binary black holes merger, opening a new observation window on the universe. One of the major upgrades concerned the control electronics of the Super Attenuators (SA). SAs are complex mechanical structures used to insulate optical elements from seismic noise. The control electronics is used to manage sensors and actuators, namely accelerometers, displacement sensors, the stepping motors and magnet-coil actuators placed in the Super Attenuators. We present a flexible and easily expandable A/D-D/A conversion and processing unit based on a powerful DSP and one FPGA that controls up to six high-performance 24-bit A/D and six 24-bit D/A converters and process data, used in the Advanced Virgo control electronics upgrade. Up to 18 units are used to control a single SA, hosted into two custom MicroTCA crates, for 10 SAs for the entire Advanced Virgo upgrade.

The A/D and D/A Processing Unit Architecture

A photo of the unit is shown in fig. 1. The FPGA (Altera EP4C30GXCF23C7N) is responsible for interfacing A/D-D/A converters with the DSP (Texas Instruments TMS320C6678) through a PCI Express link x2 at 2.5Gbps. The FPGA takes care to set up D/A and A/D converters, distributing a start conversion signal so that all devices begin the conversion process at the same time; in addition, it takes care of receiving the IRIG-B signal. Concerning the D/A converters, the digital data are sent using DSD and PCM data format. A sampling frequency up to 640 kHz and 384 kHz can be achieved using DSD and PCM data format respectively. Six parallel D/A channels are simultaneous managed. The FPGA also reads the digitized data coming from the A/D converters. All the A/D channels are read in parallel and then digitized signals are transmitted to FPGA using LVDS differential channels, with a maximum throughput of 4 MSPS per channel. Three PLL distributors take care of distributing all necessary clocks to the devices: PCI Express reference clock, A/D and D/A clock and general clock for DSP and FPGA. The DSP takes care of processing data, manages local controls and it interfaces through the MicroTCA backplane using Serial RapidIO protocols for communicating with other units for properly controlling a SA. Twenty units are necessary to equip and control an entire SA, for a total of two hundred units for 10 SAs foreseen for the Advanced Virgo upgrade.

Fig. 1

SUPERATTENUATOR



SUPERATTENUATORS (SA)

Used for isolating the VIRGO interferometer from the seismic noise

SA is a chain of cascaded mechanical filters used for suspending the mirrors to detect gravitational waves

SA is a passive device acting as low pass filter in all six degrees of freedom, capable of attenuating the ground motion by an order of 10exp(15)@ 10Hz

The control electronics is used to manage sensors and actuators, namely accelerometers, displacement sensors, the stepping motors and magnet coil actuators placed in the SA

A/D and D/A Processing Unit is the core of the control electronics and it has been used for its upgrade

PCIe INTERFACE

PCIe INTERFACE

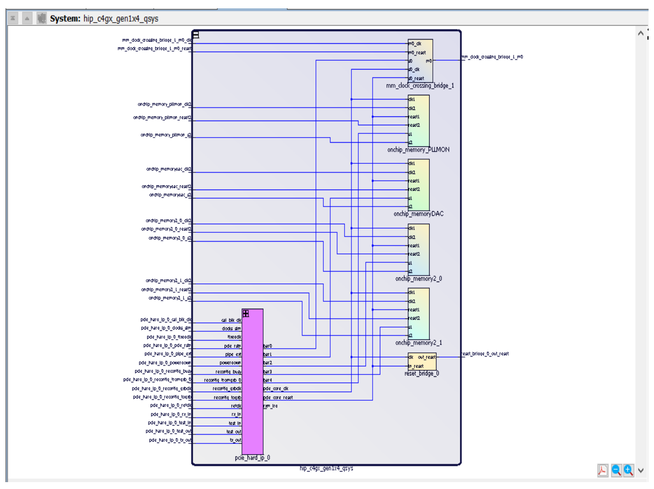
PCIe is a GEN1 x2 lines @2.5 GSPS

Loaded into the Altera FPGA as Endpoint and as Root Complex in the DSP

The Endpoint is driven by the DSP for

interface the A/D and D/A devices in parallel

interface the TOLM network, that is responsible to collect and distribute the digital data



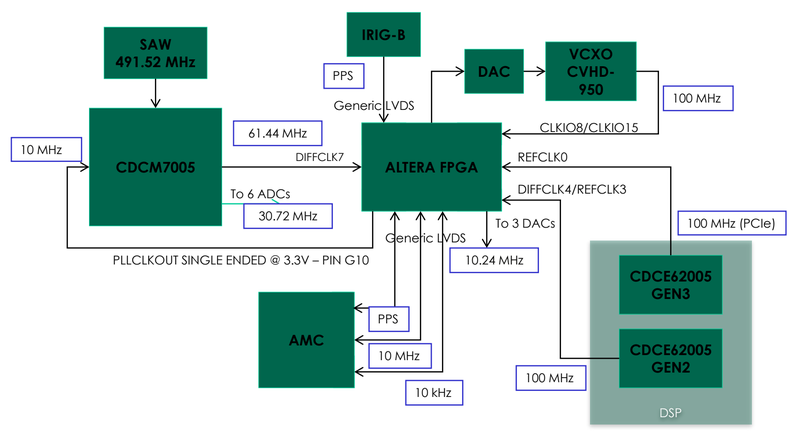
PCIe Architecture scheme

The A/D and D/A part

The D/A section is based on the Analog Devices AD1955, a high-performance 24-bit stereo audio playback system. It includes a multi-bit Sigma-Delta modulator, a digital interpolation filter, and a continuous differential output DAC. The choice of an audio converter was taken only after accurate testing in the sub-audio frequency range where chip behavior is not always fully specified by suppliers. The AD1955 is an optimum compromise between noise (i.e. effective number of bits), linearity, glitch energy and short conversion time. The device uses two data formats: PCM and DSD. In the DSD case, a DSD clock frequency of 5.12 MHz can be achieved with the limit of 640 kHz sampling frequency given by the internal DSD filter that cannot be bypassed. The advantage of DSD mode is that the group delay is about 8 µs and so is suitable for fast feedback control loops. The disadvantage is that quite large resources of the FPGA or DSP have to be used for implementing the modulator (the order depending on the noise budget of the specific application). Instead, in PCM mode a group delay of 9 us can be reached if an external digital filter is used limiting the frequency up to 384 kHz, finding an optimum compromise between DSP/FPGA resource utilization and speed requirements for fast control loops. Accurate measurements were performed on the AD1955 regarding noise below 100 Hz and harmonic distortion. In fig. 2 and in fig. 3 the THD and the noise spectra below 100 Hz are shown, while the AD1955 is converting in PCM mode at 320 kSPS

The A/D section is based on Texas Instruments ADS1675, a high performance, 24-bit Sigma-Delta ADC. It provides wide input bandwidth and high speed with the benefits of conversion to achieve a 103 dB dynamic range and -107 dB THD at 4 MSPS, making it suitable for high speed and accuracy data acquisition. Two digital filters are integrated, offering the possibility to set the frequency response, data rate, bandwidth and settling time. Furthermore, a very compact and flexible serial interface supports LVDS standard, allowing direct connection to the FPGA device, reducing the number of pins and increasing EMC. The analog interface of the ADS1675 requires only an external low-noise and distortion differential amplifier for signal buffering and level shifting, and a high-quality reference voltage with the appropriate driving capabilities. All these features make it ideal for applications demanding high SNR, multiple channels, without a complex front-end signal processing design. In fig. 4 and in fig. 5 the ADC noise spectra and THD are shown; while the ADC is converting at 3.84 MSPS.

SYNCHRONIZATION



The A/D and D/A Clock tree is very complex. The mail clock (PPS@100 Hz) - coming from the IRIG-B signal – is multiplied up to 10MHz and sent to a PLL distributor that synchronizes this signal with a 491.52MHz SAW oscillator – to reduce the phase jitter – and used to feed six ADCs and, internally divided, six DACs. Moreover, a 100MHz clock enters into the FPGA for synchronizing the VIRGO timing system and collecting and distributing digital data via a dedicated optical link. Another 100MHz clock enters in the FPGA for feeding the transceivers for PCIe. The PPS signals is sent to the AMC connector for feeding the others Unit housed in the MicroTCA backplane, as others 10MHz and 100MHz clock, so that all the Units are synchronized with the same clock. Two PLL distributors are responsible to generate the clocks needed for the DSP (e.g. for the RAPIDIO)

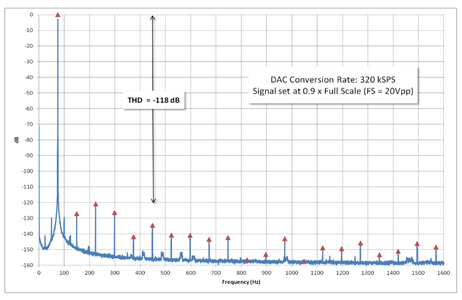


Fig. 2

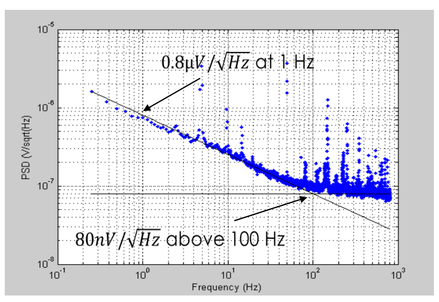


Fig. 3

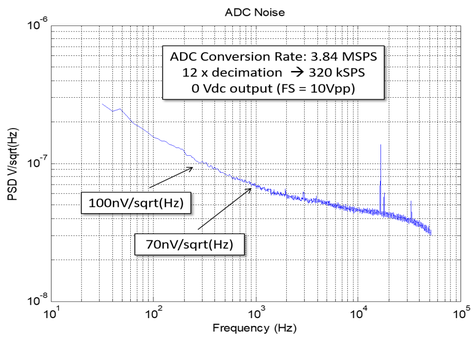


Fig. 4

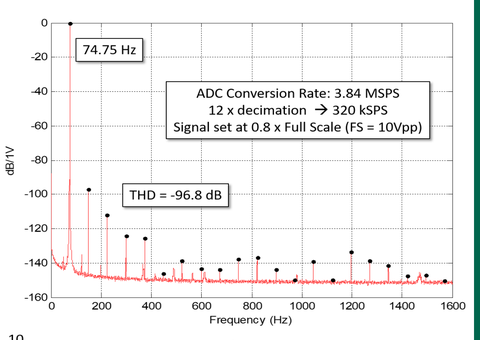


Fig. 5

Conclusion

The Advanced Virgo project has been completed in 2017. A new control electronics to manage the Advanced Virgo Super Attenuators has been designed and installed into the Virgo interferometer. The unit is very flexible, modular and suitable for the Advanced Virgo requirements, as well as for a wide range of applications requiring low noise and distortion and powerful signal processing capabilities as well as hard real-time feedback controls.

Acknowledgment

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