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TIMING SIGNAL DISTRIBUTION FOR SYNCHROTRON RADIATION EXPERIMENTS USING RF OVER WHITE RABBIT

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Abstract

In synchrotron radiation experiments, measurements such as nuclear resonant scattering, time-of-flight, and time-resolved measurements require an RF clock and fundamental revolution frequency (zero-address) signals synchronized with a storage ring accelerator as a light source. At SPring-8, these timing signals are delivered directly over dedicated fibers and cables from an accelerator timing station to each experimental station. Considering the upcoming internet of things (IoT) era, it is preferable to distribute these signals over a network using state-of-the-art digital technology. Consequently, I am building a proof of concept system (PoCS) that aims to achieve distribution of the accelerator RF clock (508.58 MHz at SPring-8) and the zero-address signals synchronized with the storage ring using RF over White Rabbit (RFoWR). The PoCS consists of a master node, which receives the RF clock and the zero-address signals from the accelerator, and a slave node, which reproduces these timing signals near experimental stations. Each node employs a Simple PCI Express FMC Carrier (SPEC) board and a new FMC DAC 600M 12b 1cha DDS (FMC DDS). The slave node generates the synchronous clock with the specified division rate and phase shift. This paper describes the achieved functions and performance of the PoCS.

MOTIVATION

Some measurements in synchrotron radiation experiments require high-precision timing signals synchronized with a storage ring (SR) accelerator, which is a light source for the experiments. These measurements include nuclear resonant scattering, time-of-flight, and pump and probe time-resolved measurements using laser pulses.

At SPring-8, a 508.58 MHz RF clock (F_{RF}) of the 8 GeV SR and a 208.8 kHz fundamental revolution frequency signal (F_{rev0}) called a "zero-address signal" are delivered using dedicated long-distance cables from the accelerator timing station to each experimental station. This requires precise timing signals. Here, 208.8 kHz is derived from F_{RF} divided by 2,436, which is a harmonic number of the SR.

To use these signals at the experimental station, long RF cables and electronics, such as divider modules and delay modules, must be deployed. These installations are costly and require experts to adjust the timing. In addition, these timing signals are available for very limited beamlines because use of the dedicated fibers/cables restricts expandability of the signals. To maximize experimental results, the precise timing signals must be easy and convenient to utilize. Considering the upcoming IoT era, it is preferable that these signals will be distributed as digital information over a network by using state-of-the-art digital technology.

RF over White Rabbit (RFoWR) technology [1-2] exactly fits this purpose. Considering there are some practical application plans using RFoWR, such as plans at CERN SPS and ESRF EBS [3], I will conduct timing signal distribution for synchrotron radiation experiments at SPring-8.

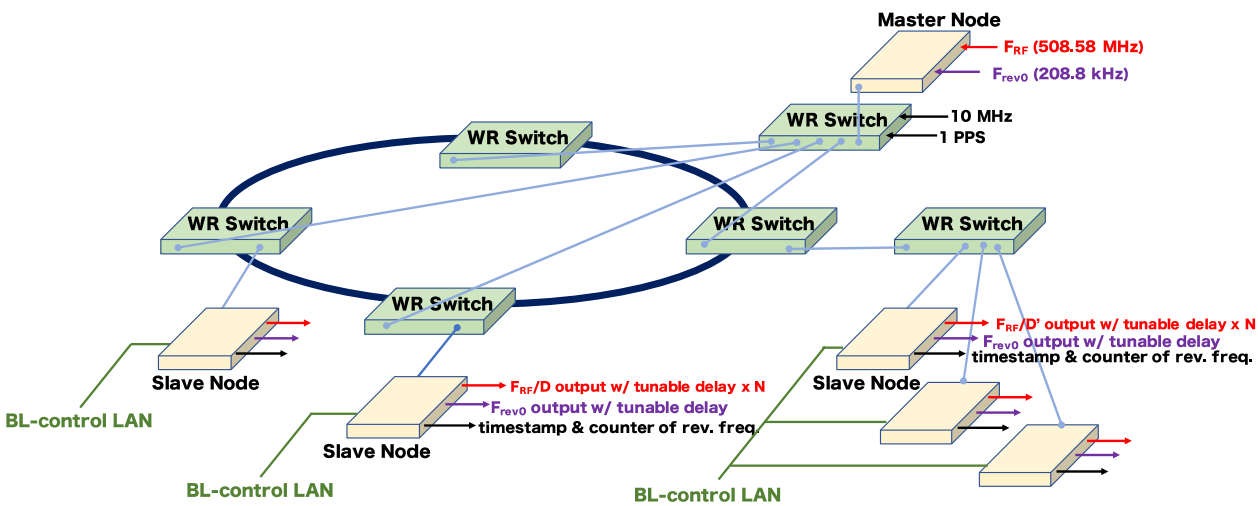

Figure 1: Conceptual design of new timing distribution system using RF over White Rabbit technology.

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GOALS

The goals of the new timing signal distribution system for synchrotron radiation experiment using RFoWR are to renovate the current timing signal distributions using dedicated fibers/cables and offer increased usability of the timing signals to the experimental users. Therefore, the new system must provide equal or better performance than that of the current distribution. Figure 1 shows a conceptual design of the timing signal distribution the new system offers. The master node settled in the accelerator timing station receives both F_{RF} and F_{rev0} signals from the accelerator timing system, and delivers these timing signals to slave nodes deployed near experimental stations through a network.

F_{RF} Distribution

Slave nodes should reproduce the synchronous signals with the same frequency as F_{RF} even though these signals are not utilized for the practical experiment. This is because the slave nodes can generate output signals with any frequency corresponding to the SR bunch filling by switching its divider values without changing the master node settings. The divider values, for example, are 6, 12, 84, and 348, which are common divisors of 2,436.

F_{rev0} Distribution

In addition to the F_{rev0} reproduction synchronized with the SR, the slave nodes should generate signals with frequencies dividing F_{rev0} by any number (e.g., 21, 54, 416, and 432).

Keeping Synchronization Against Slow Changes in F_{RF}

To compensate for the change in the SR circumference caused by tidal force, the F_{RF} frequency will be gradually altered in the range of ±500 Hz. The new system should keep synchronization against these slow adjustments.

Phase Adjustment

The new system should provide a phase adjustable function of the output signals for the experimental users to control the timing delay.

Distribution of Valuable Information

The new system can deliver timestamp and counter values related to the revolution frequency available as additional information attached to the experimental data.

Required Performances of Distributed Signals

In the case of 84.76 MHz (=F_{RF}/6) used for a femtosecond laser oscillator, which requires the most severe performance, the distributed signal at the slave node should fulfill the specifications listed below.

- Required jitter is less than 10 ps. (Current system is less than 8 ps.)
- Resolution of phase adjustment is less than 50 ps. (Current system is less than 1 ps.)
- Missing clock signal is not allowed.

BUILDING THE POCS

I have succeeded in acquiring internal funds to study the new timing signal distribution system over a network. These funds have been used to develop a proof of concept system (PoCS) to realize a new timing distribution system for synchrotron radiation experiments using RFoWR technology. Figure 2 shows a schematic diagram of the PoCS to be built, and Fig.3 is a photo of the completed PoCS. The system consists of a master node, a slave node, and a white rabbit (WR) switch. SPEC [4] boards equipped with FMC DDS [5] mezzanine cards were installed into both the master and slave nodes.

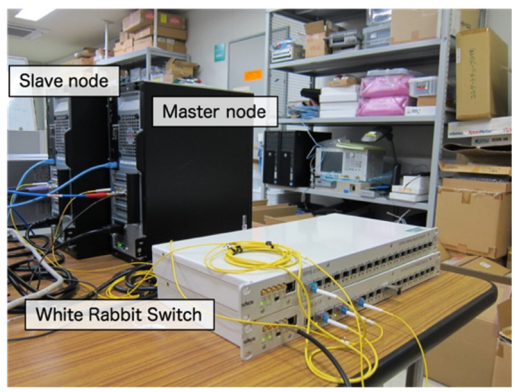

Figure 3: Photo of the PoCS.

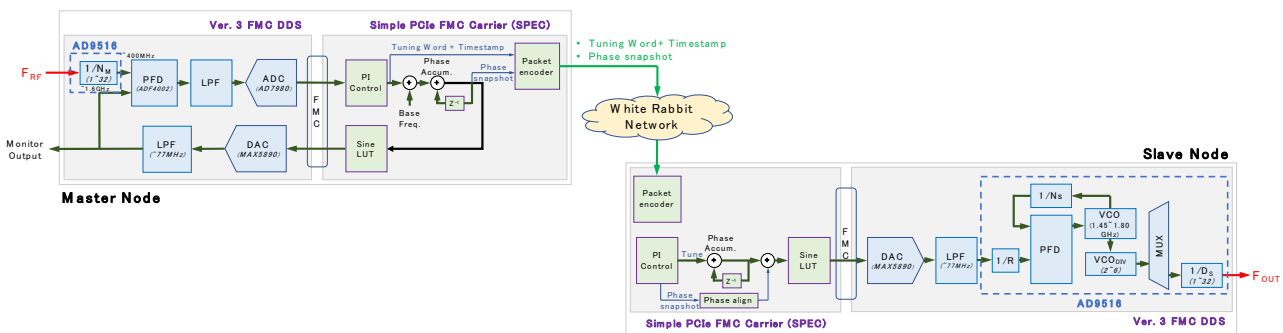

Figure 2: Proof of concept system.

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Fortunately, I was able to purchase version three FMC DDS mezzanines (Fig. 4) that had just been released at that time. Previous releases of the FMC DDS mezzanine could not provide enough output to reach the target frequency F_{RF} because AD9510 [6] combined with an external voltage-controlled crystal oscillator (VCXO) up to 500 MHz is equipped onto the mezzanine (Fig. 5). Furthermore, the performance of the previous release did not meet our requirements because the measured rms jitter (10 Hz-20 MHz) was about 16 ps as described in [1]. Meanwhile, version three FMC DDS is equipped with AD9516-4 [7] with an on-chip voltage-controlled oscillator (VCO) (1.45 GHz-1.8 GHz) as shown in Fig. 6 instead of AD9510 + VCXO (<500 MHz). Additionally, it can be expected to provide better jitter performance than the previous version.

Figure 4: Version three FMC DDS.

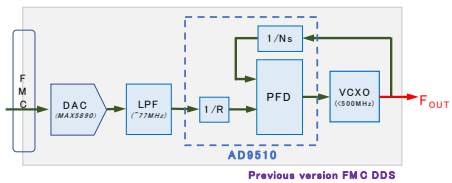

Figure 5: Output part of the previous release of FMC DDS.

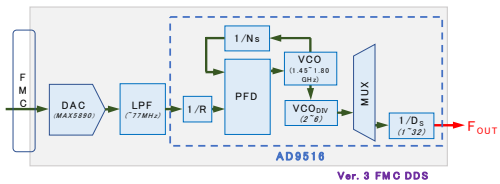

Figure 6: Output part of the version three FMC DDS.

As the version three FMC DDS was so new, the gateware and firmware to work it was not yet complete. Thanks to strong support from John Robert Gill at CERN, I was able to successfully modify both gateware and firmware for the previous mezzanine, which enabled me to carry out tests to check the function and performance of the version three FMC DDS. Figure 7 displays the observed F_{OUT} output from the slave node, which agreed with the expected result. Figure 8 illustrates the parameters set into both the master node and slave node. Here, 42.38 MHz was chosen as the DDS carrier frequency in the master node as the result of F_{RF} = 508.58 MHz being divided by N_M = 12. F_{OUT} results in 42.38 MHz synchronized with the input F_{RF} when N_S = 36, VCO_{DIV} = 3, and D_S = 12 are adopted in the slave node.

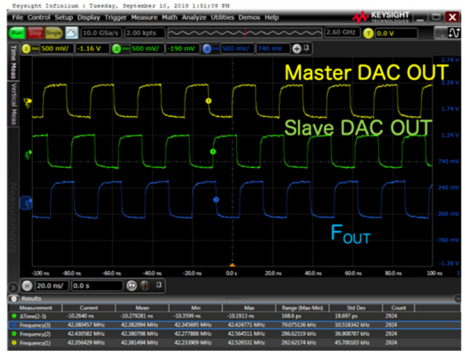

Figure 7: Observed 42.38 MHz F_{OUT} synchronized with F_{RF} (=508.58 MHz).

FIRST RESULTS USING THE POCS

The required function and performance for the synchrotron radiation experiments have been confirmed using the built PoCS.

F_{RF} Distribution

Parameters set of N_M = 12, N_S = 36, VCO_{DIV} = 3, and D_S = 1 resulted in generating F_{OUT} = 508.58 MHz synchronized with the F_{RF} = 508.58 MHz as shown in Fig. 9.

At present, only the AD9516-4 built-in dividers are available for the F_{OUT} division. The division rate for F_{OUT} can be applied from one to 64 by combinations of VCO_{DIV} and D_S. An F_{OUT} signal of 84.76 MHz (=F_{RF}/6) synchronized with the input F_{RF} can be observed using set parameters of N_M = 12, N_S = 36, VCO_{DIV} = 3, and D_S = 6. Other parameters set at N_M = 12, N_S = 36, VCO_{DIV} = 6, and D_S = 32 actually generate synchronous F_{OUT} with the frequency of 7.95 MHz (=F_{RF}/64).

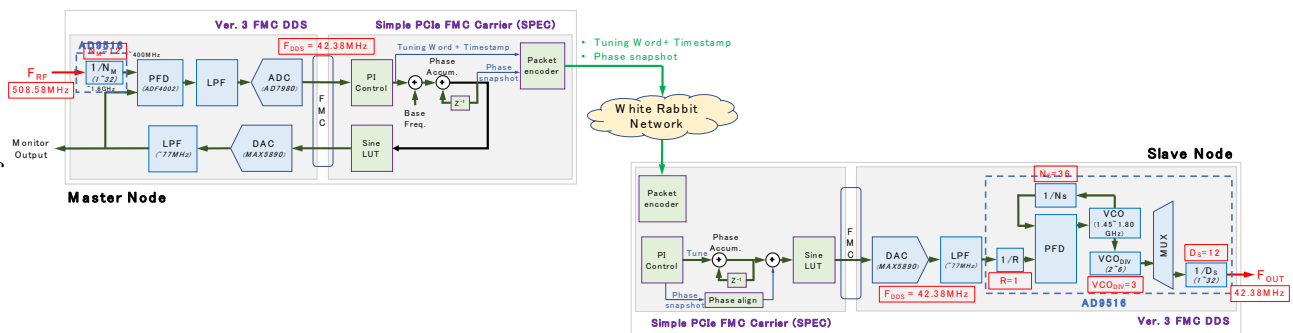

Figure 8: Parameters set to generate 42.38 MHz FOUT.

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Figure 9: Observed 508.58 MHz F_{OUT} synchronized with F_{RF} (=508.58 MHz).

Keeping Synchronization Against Slow Changes in F_{RF}

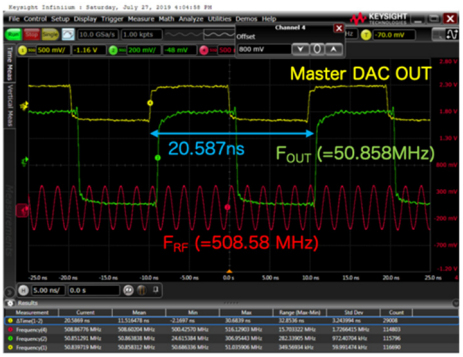
I gradually changed the F_{RF} frequency with a 1 kHz step from the 508.58 MHz center frequency while observing the F_{OUT} signal using an oscilloscope. Consequently, I found that the slave node continued to output F_{OUT} while keeping synchronization with the F_{RF} even if the offset frequency of F_{RF} was changed between ±10 kHz. Therefore, the system can accommodate the frequency change of the input RF signal within the range of ±500 Hz.

Resolution of Phase Adjustment

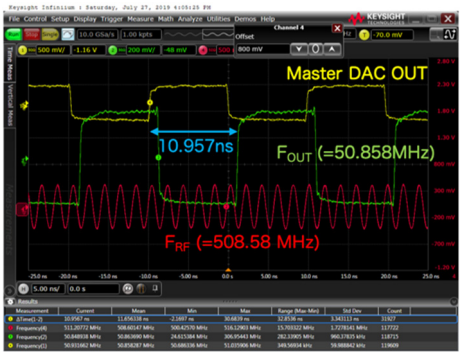
Because the FMC DDS possesses a phase accumulator with a length of 43 bits, the phase from 0 to 2π is expressed in 2^{43} states. Therefore, the phase of F_{OUT} is adjustable by adding an offset with the very high resolution of $1/2^{43}$.

I set +1,000 in the upper 11-bit of the phase-shift register with the length of 43 bits and observed a phase advance of 9.6 ns (=20.587 ns-10.957 ns) when F_{OUT} was 50.858 MHz (=F_{RF}/10) as shown in Fig. 10. This measured result completely agreed with the calculated value shown in Eq. (1).

$$\frac{1{,}000 \times 2^{32}}{F_{OUT}(= 50.858\ MHz) \times 2^{43}} = 9.65\ ns \qquad (1)$$



(a) F_{OUT} without phase offset.



(b) F_{OUT} with phase offset +1,000 in the upper 11-bit of the phase-shift register.

Figure 10: Observation of phase adjustment by adding a phase offset.

Jitter of Distributed Signals

I measured the jitter of F_{OUT} with a frequency of 84.76 MHz obtained by dividing F_{OUT} by six. The measured rms jitter is 6 ps (10 Hz-20 MHz) as shown in Fig. 11. This result showed that the version three FMC DDS successfully improved its performance as expected, and the distributed 84.76 MHz signal fulfilled the requirement specification as well.

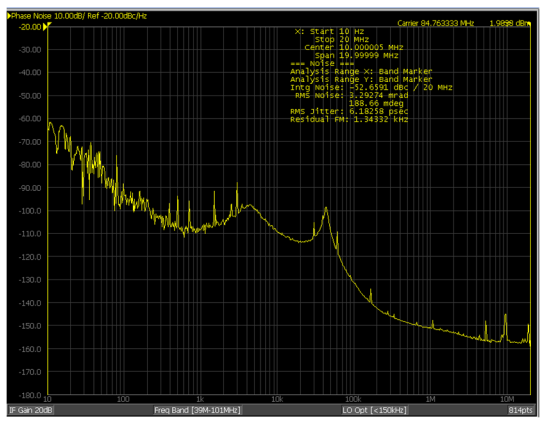


Figure 11: Measured single sideband (SSB) phase noise and rms jitter of the FOUT = 84.76 MHz.

STATUS AND PERSPECTIVE

Many tasks remain to complete the PoCS and reach the goal. However, they are all achievable. The main tasks remaining to be implemented are described below.

Implementation of F_{REV0} Distribution

Reproduction of F_{REV0} in the slave node will be implemented by counting F_{RF} up to 2,436 in the field programmable gate array (FPGA) on the SPEC board. Because the FPGA cannot count F_{RF} clocks directly, the clock will be counted up and divided by common divisors of the harmonic number 2,436 of the SR.

For example, the FPGA counts 17.54 MHz that is the result of dividing F_{RF} by 29, which is a common divisor of 2,436. Then, it outputs a signal when the counter reaches 84 (=2,436/29). To align this output signal with F_{REV0}, a timestamp recorded by the master node at the time the F_{REV0} signal inputs is utilized. The slave node resets the 17.54 MHz counter at the time described in the received timestamp when the slave DDS starts.

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This approach for F_{REV0} signal distribution is expected to further simplify the implementation of gateware and firmware, and to improve performance over the previous system [8].

Implementation of a Higher Division Rate Than 64

This function will be implemented in the same way as the F_{REV0} distribution described above.

For example, when a signal obtained by dividing F_{RF} by 384 is desired, the slave node counts a 17.54 MHz (=F_{RF}/29) clock and generates a signal every time the counter reaches 12.

If a divided signal of F_{REV0} is required, for example, in the case of a division rate of 21, the slave node counts a 17.54 MHz (=F_{RF}/29) clock and outputs the signal every time the counter amounts to 84 × 21.

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to John Robert Gill for his kind and continuous support for a new FMC DDS mezzanine and RFoWR.

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