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A CONTROL SYSTEM USING EtherCAT TECHNOLOGY FOR THE NEXT-GENERATION ACCELERATOR

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Abstract

The construction of a new 3GeV Light Source is in progress. Furthermore, we have an upgrade project of SPring-8 that we call SPring-8-II. We adopted EtherCAT technology as a network fieldbus for the next generation control systems. Currently, a low-emittance electron gun system and a digital control system with a magnet power supply have been built and bench-tested at for the 3 GeV Light Source. These systems are controlled from the MADOCA control framework via EtherCAT. Additionally, we are proceeding with the design of a new high-power RF (HP-RF) control system based on the HP-RF control system by SACLA and will introduce the system into the 3GeV Light Source. These new systems will be validated in a prototype accelerator for the 3GeV Light Source at the SPring-8 site, and will be installed in the 3GeV Light Source.

INTRODUCTION

Multiple fieldbus protocols have been used for data communications with remotely installed devices for over 20 years at SPring-8. Currently running remote I/O systems using a master/slave topology are as follows: a serial remote I/O (RIO) that was introduced at the start of SPring-8 operation, opt-VME [1] developed at SPring-8 in 2003, optical FA-link [2], and DeviceNET. These protocols are used with a magnet power supply control, a vacuum control, and an undulator control. However, products that work with RIO, opt-VME, and optical FA-Link have already been discontinued.

The construction of a new 3GeV Light Source is in progress. High-speed bus access, transfer of large amounts of data, and synchronization with a timing signal are required in the next-generation control system. As a network fieldbus, we adopted Ethernet for control automation technology (EtherCAT) [3]. Because its cyclic data transfer time is less than 1 ms, EtherCAT is suitable for a fast control and feedback system. As the control system using EtherCAT, a low-level RF (LLRF) system, a new standard in-vacuum undulator system at the SPring-8 storage ring, and a patter power supply with a kicker magnet at SACLA have been operating [4].

In this paper, we describe an improved way of handling an EtherCAT slave that requires a control sequence. We also describe the design and installation plan of the new control systems using EtherCAT technology for the 3GeV Light Source.

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CONFIGURATION AND COMMUNICATION

The EtherCAT master requires an EtherCAT network information (ENI) file for network initialization and configuration. An ENI file is generally generated from individual EtherCAT slave information (ESI) files by using a software configuration tool. An ESI file contains vendor and product information, initialization information, process data, a distributed clock synchronization configuration, etc. The main purpose of the EtherCAT master is cyclic exchange of process data with the configured slaves. There are two types of process data:

- Input process data object (Input PDO, data received from the EtherCAT slaves)
- Output PDO (Output PDO, data transmitted to the EtherCAT slaves).

Figure 1 shows a system configuration using EtherCAT. We adopted an EtherCAT master AdXMC1573 with an XMC form factor. EtherCAT communication is processed on the master protocol stack, and the operating system accesses PDO and service data object (SDO) via a shared memory mapped by the device driver of this module. We installed the EtherCAT master module into a VME, a MicroTCA.4 and a PC.

Overwrite of a Request

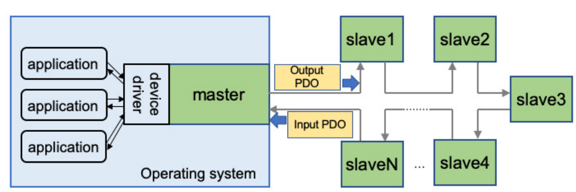

Figure 1: System configuration using EtherCAT.

We adopted a Melec F3200/EC as a motor controller. The F3200 has been used to control cavity tuners in the digital LLRF system [5] and to control undulator gap in a new standard in-vacuum undulator (IVU-II) [6]. In addition, the F3200 will be used in the 3GeV Light Source and SPring-8-II. In the MADOCA control system, at least two processes, an equipment management process (EM) and a data logging process (MDAQ), run on one host. When requests are issued from multiple processes to an EtherCAT slave, exclusive control may be necessary. Figure 2 shows the PDO map image of the F3200. The current pulse count and status of each axis can always be read from the input PDO without issuing a request. However, requests such as

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Output PDO	
Offset	Signal
+0	Control port
+1	X axis request code
+2	Y axis request code
+3	Z axis request code
+4	A axis request code
+5 ~ +8	X axis request data
+9 ~ +12	Y axis request data
+13 ~ +16	Z axis request data
+17 ~ +20	A axis request data

(request: +1 to +20)

Input PDO		
Offset	Signal	description
+0	Control status	Handshake status of request
+1	X axis status	always readable
+2	Y axis status	
+3	Z axis status	
+4	A axis status	
+5 ~ +8	X axis answer data	answer data of request
+9 ~ +12	Y axis answer data	
+13 ~ +16	Z axis answer data	
+17 ~ +20	A axis answer data	
+21, 22	X axis pulse counter value	Always readable
+23, 24	Y axis pulse counter value	
+25, 26	Z axis pulse counter value	
+27, 28	A axis pulse counter value	

(answer: +4 to +20)

Figure 2: PDO map image of F3200.

Input PDO		
Offset	Signal	description
+0	Control status	Handshake status of request
+1	X axis request code	Copy request code written into output PDO
+2	Y axis request code	
:	:	
+5	X axis status	always readable
+6	Y axis status	
:	:	
+9 ~ +12	X axis answer data	Answer data of request
+13 ~ +16	Y axis answer data	
:	:	
+25, +26	X axis pulse counter value	Always readable
+27, +28	Y axis pulse counter value	
:	:	

Offset	Signal	description
+33 ~ +36	X axis maximum pulse rate	always readable
+37 ~ +40	Y axis maximum pulse rate	
:	:	
+49 ~ +52	X axis minimum pulse rate	always readable
+53 ~ +56	Y axis minimum pulse rate	
:	:	

Figure 3: New input PDO map image of F3200.

receiving a pulse rate and setting an output pulse count require a handshake-type control sequence consisting of a request and a response. A process issues a request, the request is written on the output PDO, and an EtherCAT master sends the output PDO to the F3200. The F3200 writes the response data on the input PDO, and the process receives the input PDO via the EtherCAT master. However, when the F3200 was first introduced, there was a problem with process requests being over-written by other process requests. The conditions of over-writing of a request were as follows:

- The EtherCAT master transferred a PDO packet every 1ms.
- EM and MDAQ were asynchronously running. For example, EM issued a request to set output pulse count. MDAQ acquired data such as current pulse rate, current pulse count, and status with a cycle of several seconds.
- EM wrote a request on the output PDO map. Before the EtherCAT master issued the output PDO packet, MDAQ wrote a request on the output PDO map, overwriting the first request.
- EM could not detect the overwrite of the request. Therefore, EM judged that the request and the response were inconsistent.

To prevent the overwrite of a request, we immediately added a second check of control status for each process, and we reduced requests from multiple processes as much as possible.

As a permanent solution, we will modify the input PDO map structure as follows:

- Pulse rates are assigned to the always readable data area for each axis in the input PDO map. Therefore, it is not necessary to issue a request.
- The F3200 copies a received request to the input PDO map. The process can confirm that the response matches its request.

Figure 3 shows the new input PDO map image of the F3200. The added data area is indicated in blue. Currently the firmware of the F3200 is being updated.

INSTALLATION PLAN OF EtherCAT SYSTEMS

RF Control System

The 3GeV Light Source design will be based on the SACLA C-band accelerator. The RF control system at SACLA comprises 1) the LLRF control system that han-dles beam currents, beam positions, and the phase and am-plitude of the RF signals in synchronization with the beam operation cycle at the current maximum of 60 Hz, and 2) the HPRF control system that handles gradually varying signals such as power on/off and interlock status of com-ponents. Figure 4 shows a diagram of the RF control sys-tem at SACLA. In the LLRF control system, a trigger delay unit board, a DAC board, three ADC boards and a CPU board are installed in a VME crate for each RF unit. The HPRF control system uses PLCs for rigid controls such as PID control and local device interlock. The HPRF control system comprises a modulator PLC, an inverter PLC, a vacuum PLC, and a main PLC. They are linked with an optical FA link. The main PLC is the master and the other component PLCs are slaves. The main PLC is linked with the HPRF VME system through FL-net, which is a factory floor network protocol with masterless topology [7]. Addi-tionally, a graphic panel is connected to the main PLC via ethernet, and it can be used as a field terminal. The master and slaves of the optical FA link are con

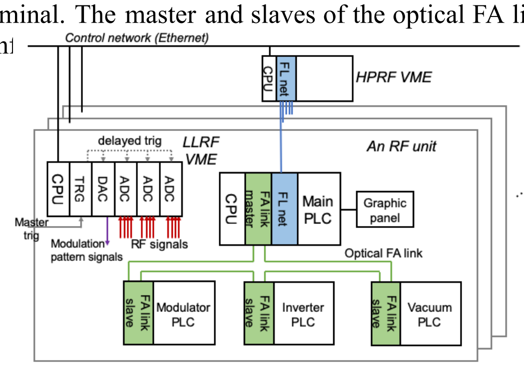

Figure 4: RF control system at SACLA.

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unit, and the HPRF VME system manages 12 RF units. The HPRF control system has the following problems:

- When a signal is added to a slave PLC, we have to modify a register map between the main PLC and the slave PLCs, and we have to update the ladder program of the main PLC. One master controlling everything is a heavy burden on management and cost.
- Each component maker has to prepare a sequence CPU module for a factory test.
- The optical FA link module has already been discontinued.

To solve these problems and introduce an RF control system to the 3GeV Light Source, we designed a new system using EtherCAT and MicroTCA.4 as shown in Figure 5. The main PLC and a VME system are replaced with MicroTCA.4. A new RF control system integrates an LLRF and an HPRF. The reduced number of computers will lower construction cost. In the LLRF, an advanced mezzanine card (AMC) digitizer, a signal-conditioning rear transition module (RTM), a trigger delay module, an EtherCAT master XMC module mounted on an XMC carrier module, a MicroTCA carrier HUB (MCH), and a CPU module (running Ubuntu 16.04 LTS configured with a low-latency kernel) are installed in a MicroTCA.4 crate for each RF unit. In the HPRF, each PLC has a sequence CPU module, an EtherCAT slave module, and a graphic panel; thus, a component PLC can run individually for local operation. New component PLCs will be based on component PLCs of SACLA HPRF. By using an EtherCAT slave supporting dynamic PDO, we can easily vary the communication protocol from optical FA link to EtherCAT, because dynamic PDO provides a flexible function with user-definable PDO contents.

Slave-to-Slave Communication

To improve convenience in local operation, we developed a display unit using slave-to-slave communication via EtherCAT. The display unit is currently used in an IVU-II at SPring-8. Figure 6 shows that the IVU-II control system contains an EtherCAT master implemented in a VME CPU board, a motor controller for gap control (F3200), main- and sub-absolute encoders for readout of the undulator gap position, and a display unit. The slave module connects to a graphic panel via serial connection. The display unit must be located downstream of main and sub encoders, because it receives encoders data contained in PDO from slave-to slave communication, calculates gap value and height from the encoders data, and displays them. The display unit is not operated from EM.

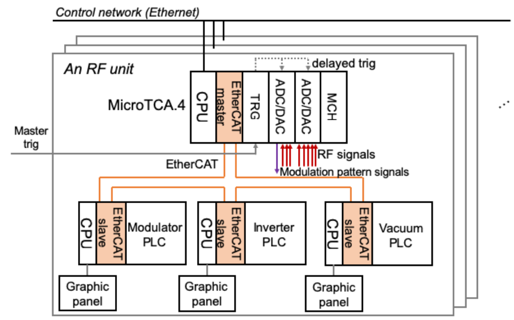

Figure 5: A new RF control system.

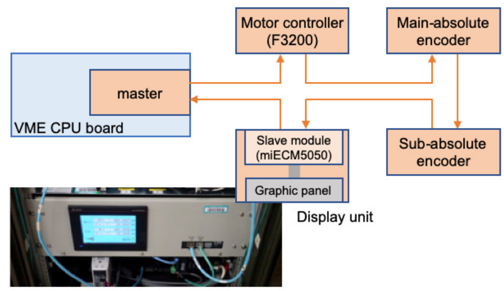

Figure 6: Diagram of EtherCAT modules for IVU-II. The photograph is a display unit.

Digital Control System with High Precision Magnet Power Supply

The magnet system of synchrotron radiation comprises various magnets with a wide range of output current. The multi-pole magnets are required a high-power power supply (PS) with driving current from 10 kW to 200+ kW and current precision of at least 20 ppm (pk-pk). Small current magnets, such as a steering magnet and a skew magnet, requires a small PS with current precision less than 50 ppm (pk-pk). To handle these various PSs with a unified concept, a new digital control system with a high precision ADC circuit and a feedback circuit implementing FPGA were developed [8]. The current magnet PSs at SPring-8 are linked with a VME system through opt-VME or RIO. Control commands such as “on/off power”, “set current value”, “get current value”, and “get status” are issued from the VME system.

However, opt-VME and RIO have already been discontinued. We adopted EtherCAT instead of these protocols. Figure 7 shows a digital control system with high precision magnet PS. Currently, the high-power PS and the PS for steering magnets have been bench-tested. Each PS has a control unit equipped with PLC modules, and the control unit communicates with the VME system via EtherCAT. We will introduce a PC instead of a VME system in the 3GeV Light Source.

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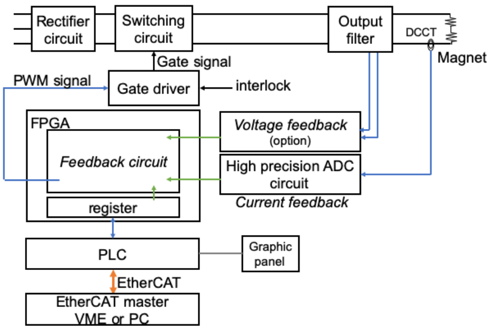

Figure 7: A digital control system with high precision magnet PS.

Low-Emittance Electron Gun System

A simple and compact electron gun system comprised a 50-kV thermionic gun with a gridded cathode and a 238-MGz RF cavity has been developed for the 3GeV Light Source [9]. Currently, the test bench is constructed to confirm the beam performance. A 238 MHz amplifier control unit and a vacuum control unit equipped with PLC modules and a graphic panel are implemented. Control commands such as "on/off cathode heater", "open/close vacuum gate valves", and "get vacuum pressure" are issued from a VME system via EtherCAT. Figure 8 shows a 238 MHz amplifier control unit in a rack. Additionally, a 476 MHz amplifier control unit and a gun high-voltage control unit will be in Fall 2019.

SUMMARY

The construction of a new 3GeV Light Source based on the C-band accelerator developed by SACLA is in progress. We adopted EtherCAT technology as a network fieldbus for the next-generation control system. Communication with an EtherCAT slave that requires a handshake-type control sequence becomes reliable by devising a PDO map structure. Currently the accelerator components such as the gun, RF, and magnet PS have been tested at the SPring-8 site. These accelerator components are operated from the MADOCA control system via EtherCAT.

Figure 8: A 238 MHz amplifier control unit at the test bench. Upper photo is a 238 MHz amplifier control rack. Lower photo is the rear of a 238 MHz amplifier control unit.

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