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COMMISSIONING OF THE 352 MHz TRANSVERSE FEEDBACK SYSTEM AT THE ADVANCED PHOTON SOURCE*

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Abstract

With the success and reliability of the transverse feedback (TFB) system installed at the Advanced Photon Source (APS), an upgraded version to this system was commissioned in 2019. The previous system operated at a third of the storage-ring bunch capacity, or 432 of the available 1296 bunches. This upgrade samples all 1296 bunches which allowed corrections to be made on any selected bunch in a single storage-ring turn. To facilitate this upgrade the development of a new analog I/O board capable of 352 MHz operation was necessary. This paper discusses some of the challenges associated in processing one bunch out of 1296 bunches and how flexible the system can be in processing all 1296 bunches. We will also report on the performance of this system.

INTRODUCTION

The Advanced Photon Source (APS) experiences beam instabilities in both the transverse and longitudinal planes. In the past, the P0 Feedback (Transverse Feedback) system, in its initial version, has corrected transverse instabilities in a bunch pattern that has up to 24 bunches. This is accomplished by using a pick-up stripline, drive stripline, four drive amplifiers, a 3-tap comb filter for front-end signal conditioning, and an Altera PCIe Stratix II GX FPGA-based development board coupled with a Coldfire CPU. The Coldfire CPU uses EPICS [1] with RTEMS [2] for all the remote monitoring and control. However, the P0 Feedback was unable to perform during a 324-bunch pattern. This paper discusses the addition of the 352MHz TFB system, its performance, added features and modifications, and possible future plans.

SYSTEM CONFIGURATION

The current system consists of a pick-up stripline, a front-end signal-processing unit, an Altera PCIe Stratix II GX FPGA-based development board (P0 Feedback), a Terasic TR4 Stratix IV commercial board (352MHz TFB), drive amplifiers, and a driver stripline. This system has been described in detail [3, 4]. Figure 1 shows a block diagram of the current system without the remote DAC hardware. At the core of the P0 Feedback system contains an FPGA processor that utilizes 864 32-tap FIR filters running at 117.3 MHz. The new Transverse Feedback system utilizes 2592 32-tap FIR filters running at 352MHz. The algorithm used in the filter is based on the least square fitting method to determine filter coefficients [5].

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The diagrams do not show both TFB systems in parallel with each other, but figure 2 shows how the new TFB has been integrated into figure 1 using splitter/combiner for both the inputs and outputs.

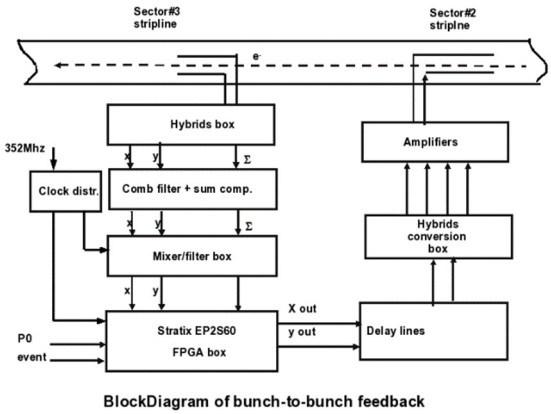

Figure 1: Block diagram of the feedback system.

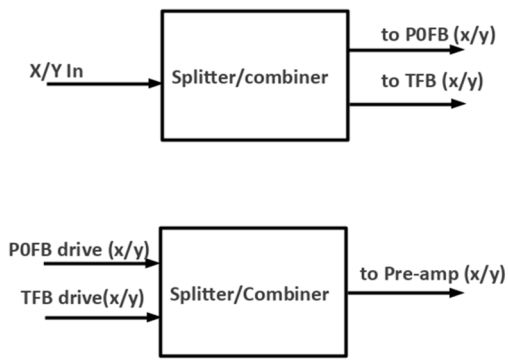

Figure 2: Block diagram of the integration of the new TFB system.

The pickup and drive striplines are located in different locations of the storage ring, which is a major issue for the X-channel since the distance between pickup and drive is seven sectors, or about 188 m, apart. A remote DAC linked to the main transverse feedback system via high-speed fiber optic cable utilizing a real-time data transfer protocol. Figure 3 shows the addition of the transceiver in the main transverse feedback chassis used to connect the remote DAC chassis.

PREVIOUS SYSTEM AND LIMITATIONS

The old PO Feedback FPGA system described above has been very successful for the Advanced Photon Source as it has been detailed in a previous paper [6]. This system is limited to 324 or 432 buckets depending on the operating frequency of 88 or 117.3 MHz when configured for a

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particular bunch pattern. This was too difficult to switch between frequencies, a transverse feedback system that can encompass all 1296 buckets was needed. This would require the system to operate at the full storage ring frequency of 352 MHz. At 432 buckets, the system is operating at 117.3 MHz, which is near the limitation of the ADC/DAC interface to the FPGA. The previous ADC has a maximum sample rate of 125 MHz while the DAC can perform at 150 MHz. The previous FPGA (Stratix II GX) is limited to a maximum transceiver rate of 6.376 Gbps of which 2.3 Gbps is needed to transport data to the remote DAC at system clock rate of 117 MHz. To transport data to the remote DAC with a system clock rate at 352 MHz, the transceiver needs to triple its transmission rate from 2.3 Gbps to 7.04 Gbps, which is beyond the Stratix II GX chip's capabilities.

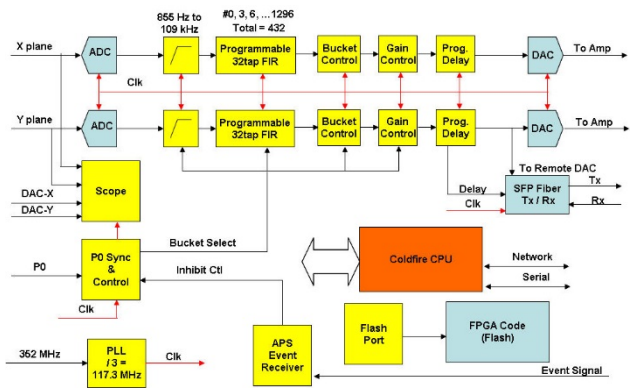

Figure 3: FPGA block diagram of the P0 feedback.

HARDWARE UPGRADES

With the Altera development boards, it was only possible to use the HSMC Data Conversion Board, which is a single HSMC board that has two ADCs (125MHz) and two DACs (150MHz) because they were single ended lines. The single ended lines allowed up to four chips with a 14-bit buses to connect to the HSMC connector. But the speeds required for operations at 352MHz requires differential data lines, or LVDS signals, limiting the HSMC connector to only one ADC and one DAC. It was obvious that two HSMC boards was necessary to maintain a two-channel system with two ADCs and two DACs for 400MSPS operations. Discovered an alternative main board that had more than two HSMC connectors and it was the Terasic TR4 FPGA Development Kit [7], which also has a Stratix IV GX chip installed on it. This board has six HSMC connectors, which provided the flexibility of installing two 400MSPS Data Conversion boards. The remaining four connectors configured for a Coldfire CPU board, a Transceiver to SMA board, an eight cage SFP board [7] and then an Event Receiver interface board.

The 400MSPS boards were specially designed for this project and System Level Solutions, Inc. (SLS) did the engineering. Four main components that is installed on this board are, ADC (ADS5474), DAC (DAC5675A) and two Clock Jitter Cleaner (SI5317A) chips. The clock jitter cleaners also provide a nice means to adjust the clock phase to fine-tune the ADC or the DAC to the FPGA fabric.

UPGRADE HARDWARE ISSUES

The Terasic TR4 board has a Stratix IV chip on it as the main component and according to the specs is more than capable to handle 352MHz. The board has the extra HSMC connectors needed for this application and as it turns out five of the six are being used. When SLS designed our 400MSPS Data Converter daughter board for us they borrowed one of our Terasic TR4 boards for development. They selected the best port to do their development on but the project need two daughter boards attached to this TR4 board. A second port that was idea for the 400MSPS board used, but, unlike the first port which had true LVDS for both input and output pins to the FPGA, about half the pins attached to this second port did not have true LVDS from the FPGA. Terasic provided a way to add resistors to each of the data pins to emulate LVDS. This emulation had a reduced data rate of 500MHz, so at first this seemed doable, but later discovered that having a mix of true LVDS with emulated LVDS was not meeting timing. The only other HSMC port with true LVDS pins was under the first 400MSPS Data Converter. This presented a problem since the SMA connector was straight, it needed to be changed to a right angle. Replacing these was a challenge due to the multilayer board, so we only modified five of the nine boards.

Initially the SMA clock connector wasn't going to be used because the original plan was to use the installed Silicon Labs Si5317 chip which is a clock jitter cleaner. The clock signal was originally going through the HSMC connector to the Si5317 chip. The chip performed well, however, there was no way to program any phase adjustments so every time there was a power down a phase adjustment had to be performed again when it powered back up. It was decided that an external clock would drive the DAC chip.

A problem was discovered with sampling of the ADCs. "The polarity of ADC chip Data Ready (DRY) signal with respect to the sample N data output transition is undetermined because of the unknown startup logic level of the clock divider that generates the DRY signal (DRY is a frequency divide-by-two of CLK input). Either the rising or the falling edge of DRY will coincident with sample N and the polarity of DRY could invert when power is cycled off, on or when the power-down pin is cycled." [8] With this in mind a means of lining up two separate ADC and syncing the data to the correct bucket required additional circuity. The solution uses a FIFO for each ADC data to correct this issue on power-up. The FIFO's are only 32 words deep and both FIFO's do not have the read enabled until both FIFO's reached half-full. Once both FIFOs reach half-full status the read enabled is set which allows the data to pass through. From this point forward, the FIFOs will maintain their depth count, that is to say, they will never go empty or full. If either case happens this will indicate something is failing. In normal operations the FIFOs have been recorded as being two clocks apart to as much as 12

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clocks apart. While this may seem to unaligned the data with the bucket number associated with its data, high level software can scan the data relative to the P0 bunch marker (revolution clock). Once found an offset is made to the bucket scan list and the scan record is modified to reflect this offset.

Now that the TFB can scan all 1296 buckets a request to add a secondary scope function of 262144 words per channel was added. The input waveform contains important information of the beam, such as external and internal noises, beam instabilities, and transverse tunes. With the extended waveform of 262k samples, we can measure 24 bunches tune of 24 singlet fill pattern with a resolution of 0.0001 (40.2ms of data or 10,923 turns). For 324 singlet fill pattern we can get a resolution of 0.001 (2.98ms of data or 809 turns). We may be able to use the system to identify couple-bunch instability modes with post processing.

SOFTWARE IMPROVEMENTS

The two system are controlled through separate MEDM main control screens, which have very similar interface features. Figure 4 shows the MEDM screen for the TFB system.

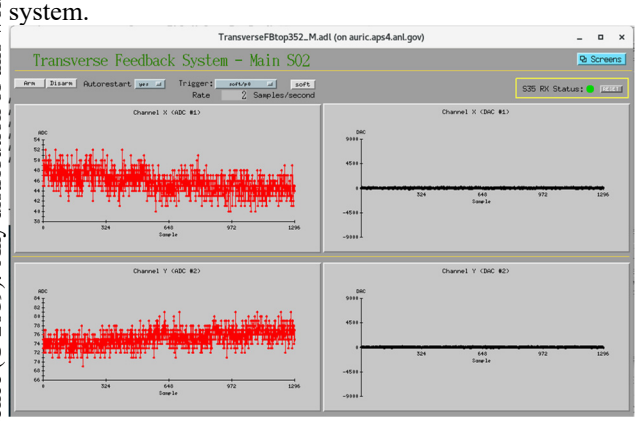

Figure 4: Main control screen for the TFB system.

The screen shows the sampled input waveform and processed output digital waveform for both x and y channel. Some sub-screens show the configuration details such as, gain array, sample pattern, output delay and front-end delays, etc. Since program of the system is mainly through high-level programs these displays are mainly for status monitoring.

High Level Applications

High-level applications include the generic Save/Compare/Restore, a GUI based TFBControl (TransverseFeedbackControl) application. This application has similar functions and controls with the existing P0FeedbackControl application. We only describe TFBControl here.

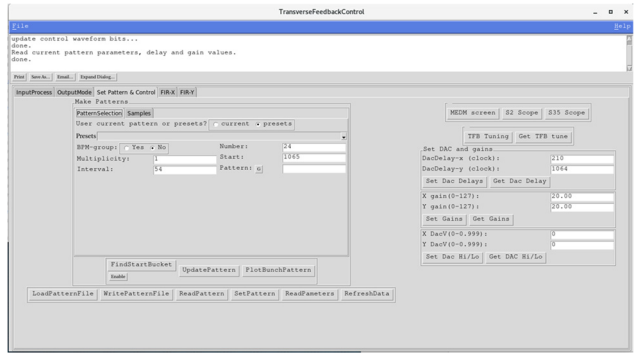

Figure 5: Main screen of TFBControl application.

Figure 5 shows the main screen of the TFBControl app. The "Set pattern & control" tab provide most of the control functions, including program of the bunch sample pattern (must match to the fill pattern in the ring). The output put pattern (which defines output pulse width and shape, and display waveform), setting of DAC output delays (in sample clock units), loop gains (range 0 to 128, with 0 as open-loop), and fixed DAC output level (when programmed for fixed amplitude pulse output for testing purposes).

Scope Signal

The system provides scope display of the attenuator output of the stripline kicker, which contains both beam induced signals and drive signal from the amplifiers. The attenuators are 40dB. The signals are important for aligning the DAC output with the beam arrival time. They are also used to measure the beam induced voltage and drive power of the amplifiers. The scope screens are remotely displayed via vnceviewer [9].

FIR Filter Generation

At the core of the system is a FIR filter, which provides the algorithm of loop processing. The filters are a 32-value array and loaded via waveform PV (process variable) of the EPICS. Figure 6 shows the interface that generate the FIR. There are two panels: the left panel controls how the filters are generated, the right panel displays the results and the existing FIR filter in the FPGA.

We generate the FIR filter from APS storage ring operational model lattice file, which is always selected as default. Twiss parameters, location of the kicker and pick-up striplines are loaded by pressing "Load Twiss Parameters" button. The Update button generates a new FIR filter, which is shown in the display panel but not loaded into the FPGA. Optional parameters are: target fraction tune, which allows to use a different tune for FIR computation, order (number of turns or taps), delay turns, phase adjustment (not used normally), and polarity of the filter, which switch between damping and excitation.

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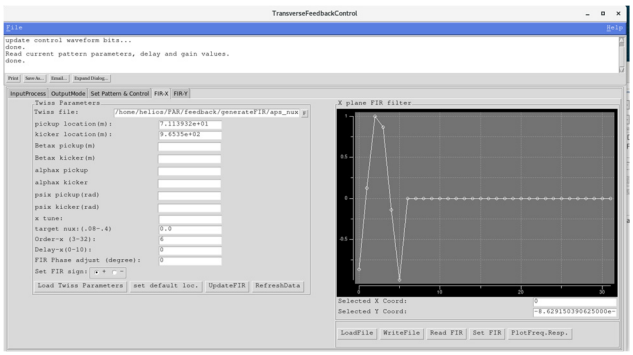

Figure 6: Control screen for FIR generation.

There are several optimization or tuning must perform in order for the feedback system to work correctly. The following functions explained in detail. Figure 7 shows the feedback system-tuning screen.

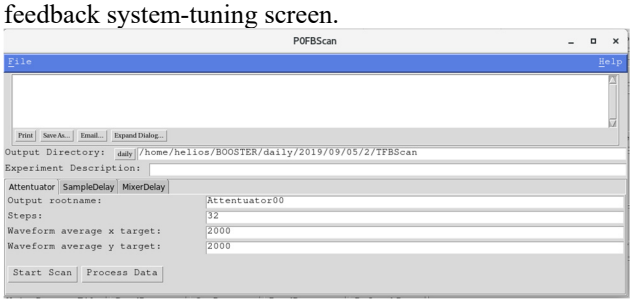

Figure 7: TFB Tuning Screen.

FindStartBucket

The TFB system is synchronized to the storage ring revolution via a P0 signal that is transmitted via a single mode fiber. Various delays exist in both signal and timing channels. Therefore, alignment of the timing must be performed after each machine maintenance period, or bunch pattern switching. To do that we need to fill the beam with the target pattern with some beam with loops open and press the "FindStartBucket". The process will set the correct start bucket number, which matches the bucket 0 of the storage ring.

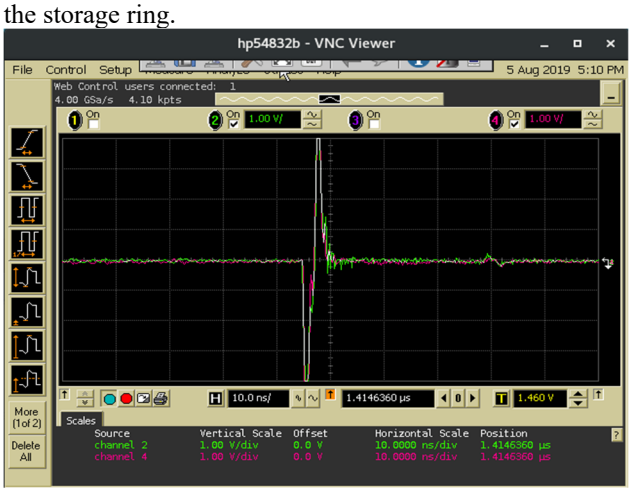

Figure 8: S35 scope signal showing x-plane beam & drive signals.

Attenuator Scan

The input signal of the TFB is a combination of x- or y-plane signals with sum signal of the same channel. Add or subtracting sum signal is necessary to compensate for the orbit signal, which has harmonics of revolution frequency of the ring. Without compensation, a large offset can cause saturation of both front-end circuit and input ADC. To scan the attenuator, fill the ring with the target pattern with as much beam that can be stored with the loops open and then run the scan. The process will run through the attenuator range and look for an average input ADC reading of 2000 counts (or user specified counts), and sets the attenuators.

Mixer Delay Scan

The front-end circuit down-converts input signal, which is broadband, into baseband (100 to 176 MHz). It does so by mixing a 352 MHz RF signal and the input signal. Maximum signal is achieved when the beam timing aligns with the RF signal zero crossing. The mixer scan function performs this alignment. To do the scan, open the feedback loops, fill the target pattern beam with as much beam that can be stored with loops open and run the scan. The process will show the results and sets the mixer delays.

Sample Delay Scan

The input signal to the TFB system is a bell-shape pulse. When the ADC sample clock is located on the shoulder of the pulse any timing jitter of the input and sample clock is amplified in the sampled data. When the sample clock is located at the top flat part of the input pulse the effect of timing jitter is minimized. To do this scan, open the loops and fill the ring with target pattern with as much charge that can be stored, and run the scan. The process will show the scan result and sets the delay to optimized values.

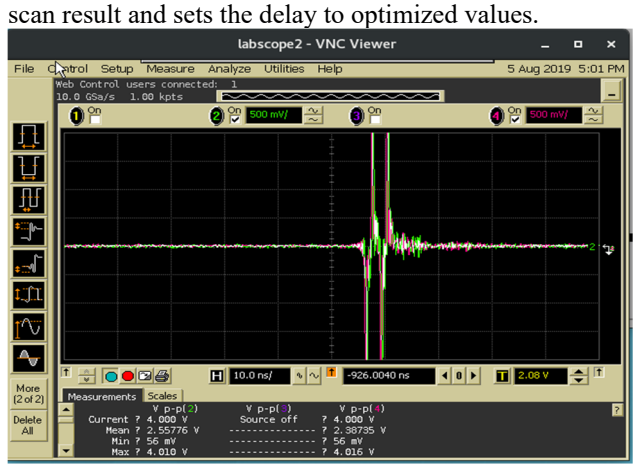

Figure 9: S2 scope signal showing y-plane beam & drive signals.

DAC Output Delay Adjustment

The output signals must arrive at the stripline at the same time as the beam bunches. The DAC delays are designed for that purpose. The delay can only be adjusted in clock units, which is 2.84 ns. To adjust the DAC delay, bring up the vnc screen for the S2 (y-plane) and S35 (x-plane) scopes. Manually adjust the DAC delay counts to center the

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beam signal (which is two narrow pulse with opposite polarity) to the first half pulse of the output drive signal (which is two pulses with flattop positive and opposite polarity).

Tuning the System with Beam

The system tuning process establishes the basic condition for the system to work. However, we still need to adjust the physics parameters in order to stabilize beam. These includes adjustment of the gains and FIR filter parameters.

We fill the target pattern beam with the loops open to the level when efficiency drops to very low. We start working on one plane at a time. Here are the steps:

1. Close the loop with a gain of 1 to 5.
2. Set the standard filter with positive (+) polarity.
3. If the scope signal and output waveform oscillate with large amplitude, reverse to negative (-) polarity.
4. Retest with increased gain to ensure that there is clear distinction of damping and excitation.
5. Set the gain to normal values (10 to 20 for 24-singlet fill, and 6 to 10 for hybrids fill).
6. Use the "Get TFB Tune" [10] to take tunes. If the tunes show clear peak at tune location the system is set correctly.
7. Continue to fill to 102mA and run top-up.

Figures 8 and 9 show the typical scope signal with correct timing alignment.

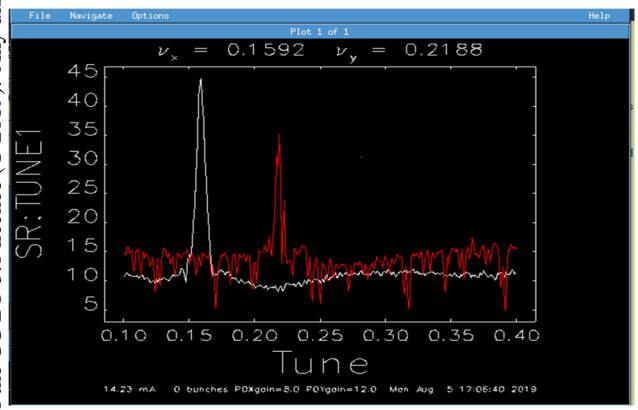

Figure 10: Tune plot of hybrids fill pattern when the loops are optimized.

BEAM TEST RESULTS

We performed beam test for 24 singlet and 1+8x7 hybrids fill pattern. We were able to fill the beam to 102mA with the normal operational chromaticity settings and maintained a stable beam. For the hybrids fill pattern the maximum single bunch limit is around 17.5 mA, which satisfy the requirement for user operations. Figure 10 shows a typical tune spectrum when system is optimized for hybrids fill.

FUTURE PLANS

We are looking to expand the TFB to include a DAQ function. The Advanced Photon Source Upgrade (APS-U) has developed a Data Acquisition (DAQ) System due to the high data volume that is expected. To accomplish this task the Coldfire CPU will need to be replaced with an EPICS Soft IOC. A typical soft IOC at the APS is Linux based running from the main server. This IOC would interface to the TFB through the DAQ network. The TFB would simply use one of the spare SFP cages where an RJ45 module would be installed. Inside the fabric an Ethernet to Avalon bridge would be created to replace the Coldfire bridge to access all the function that is part of the TFB. A second Ethernet port is required for the DAQ functions. At the APS-U a dedicated network port is required for DAQ function due to the large amount of data expected on this network, hence the need for a separate network port for the DAQ interface.

CONCLUSION

We successfully completed the development and testing of transverse feedback system that upgraded the sample rate to 352 MHz, allowing the system to run in all three user operational fill patterns (24 singlet, 1+8x7 hybrids and 324 singlets) and other patterns for machine studies. Both control screens and high-level applications are completed now for user operations.

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