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CONTROL SYSTEMS DESIGN FOR LCLS-II FAST WIRE SCANNERS AT SLAC NATIONAL ACCELERATOR LABORATORY*

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Abstract

One of the primary diagnostic tools for beam emittance measurement at the Linac Coherent Light Source II (LCLS-II), an upgrade of the SLAC National Accelerator Laboratory's Linac Coherent Light Source (LCLS) facility, is the wire scanners. LCLS-II's new Fast Wire Scanner (FWS) is based on a similar mechanical design of linear servo motor with position feedback from an incremental encoder as that for LCLS. With a high repetition rate of up to 1MHz from the superconducting accelerator of LCLS-II, it is no longer sufficient to use point-to-point EPICS-controlled moves from wire to wire, as continued exposure will damage the wires. The system needs to perform on-the-fly scans, with a single position versus time profile calculated in advance and executed in a single coordinated motion by Aerotech Ensemble motion controller. The new fast wire scanner control system has several advantages over LCLS fast wire scanner controls with the capability to program safety features directly on the drive and integrate machine protection checks on an FPGA. This paper will focus on the software architecture and implementation for LCLS-II Fast Wire Scanners.

INTRODUCTION

For measuring the electron beam profile, wire scanners (Fig. 1) are the primary tool used at the LCLS. The fast wire scanner system is comprised of a linear motor stage with an incremental linear encoder for closed loop position feedback [1]. The movable stage which has limits switches at the end of travel of the stage (Fig. 2) holds a wire card. Beam loss monitor readings obtained during a scan of the wire card through multiple bunches of the beam, helps provide the cross section of the beam. With the correlation of the wire positions from the encoder feedback and the beam loss monitor readings beam sizes, beam emittance, energy spread, or bunch length can be determined [2].

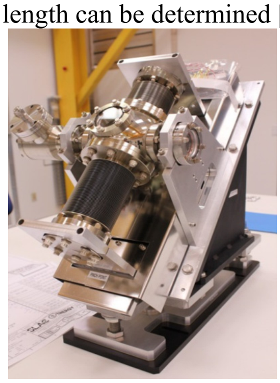

Figure 1: Wire Scanner at SLAC [1].

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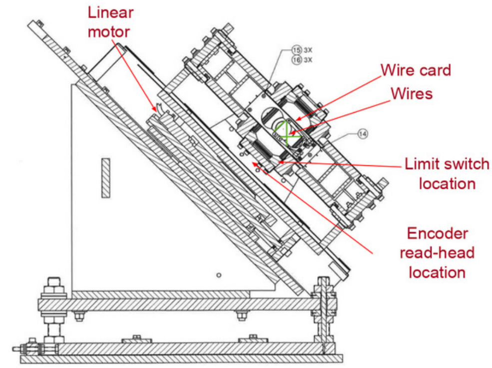

Figure 2: Wire scanner schematics showing the motor, encoder and limit switches.

CONTROL SYSTEM

Architecture Overview

The wire scanner controls electronics are housed in support buildings with long haul cables running to the hardware in the tunnel [2]. The servo motion control and PID (Proportional, Integral and Derivative) feedback is done with an Aerotech Ensemble CP20 Motion Control drive. The controller chassis enclosure supports two channels of wire scanners with independent Ethernet interfaces to the EPICS control system. The beam loss monitor signal and the external position encoder readings are recorded through a SLAC-standard common platform ATCA crate, housing a carrier card with a Xilinx FPGA. Readings are acquired beam synchronously with the inclusion of the central timing system through the crate [3]. The FPGA on the ATCA crate performs checks on the speed of the wire scanner and relays the information to Machine Protection System to prevent destruction of the wires during continuous-wave beam operations [2]. A block diagram of the system design is presented in Fig. 3

Aerotech Motion Controller

The 3U Aerotech controller chassis includes control for 2 servo motor axes by way of 2 individual Ensemble CP20 Motion Control drives. The Ensemble CP20 offers extensive tuning tools for an extended PID delivering nearly optimal performance, observable using the built-in Digital Scope [4]. Each CP20 axis supports up to 20 Amps peak (10 Amps continuous) at 160VDC, satisfying the hefty requirements of the wire scanner system, while also providing high-precision control with kilohertz-level servo tasks and high current-resolution output.

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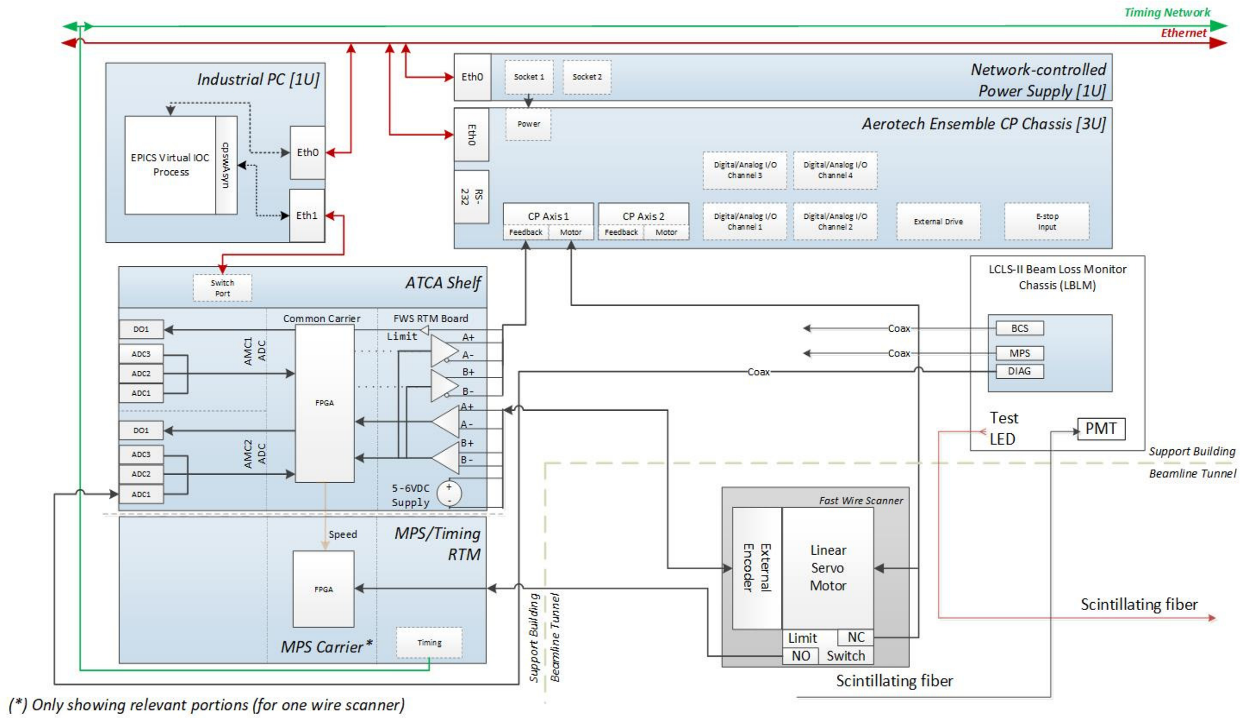

Figure 3: Controls System Architecture of Fast Wire Scanner at SLAC.

On top of that, controller offers the ability to customize many aspects of a process by programming up to 5 cyclic tasks. The wire scanner uses one of these to handle the homing routine, consisting of retracting the stage to hit the lower limit switch and setting that position as the known home position, or “0 position”. Separately, a fault handler and a recovery operation are run on another two continuously running tasks.

Faults such as over-current, over-temperature conditions and feedback are actively monitored at kilohertz rates and cause appropriate recovery actions to happen, such as homing and disabling of the wire-scanner motor. Finally, a wire scan routine is set up as the fourth task on the controller, in which an S-curve trajectory is programmed to be used for smooth motion when triggered via EPICS.

Motor Controls in EPICS

The controller is connected to the EPICS control system through Ethernet over TCP/IP using a simple ASCII-based protocol. When a wire scan is requested from EPICS, relevant parameters like speed and wire positions will be sent to the Aerotech motion controller from EPICS.

The interface is implemented using EPICS collaboration`s asyn based motor record support (Fig. 4). For non-standard EPICS motor information, such as diagnostic information, a Stream Device custom protocol file is used to side-channel this information to EPICS records. A software motion trigger sent through EPICS will cause the motion controller to send the wire scanner through its pre-planned trajectory. Upon a request of a wire scan, a State Notation Language (SNL) program is executed on the EPICS Input/Output Controller (IOC) to initialize the servo motor. The initialization process consists of several steps:

1. Check if wire scanner faults program is running on the controller. If not (which can happen during a hard reset of the controller), start the program.
2. Turn on motor torque
3. Run the motor home command.
4. Set encoder initialization process complete flag.

A retract and timeout SNL program is also continuously run if a timeout is enabled for the servo motor. This process turns off the motor torque if the wire scanner is left turned in an active state for a significant amount of time. This is to reduce the electrical noise generated by the PWM control of the servomotor in the tunnel, which has been known to affect nearby sensitive devices.

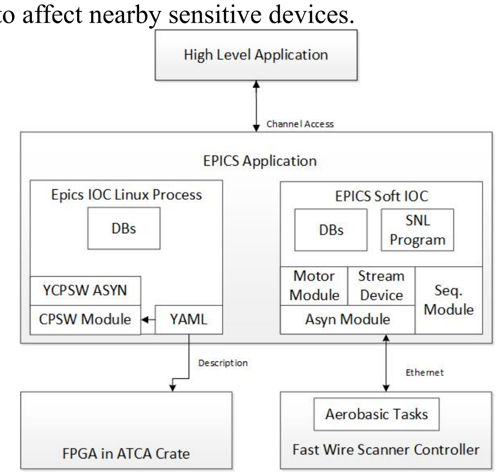

Figure 4: Software Architecture of the Fast Wire Scanner.

FPGA Controls

The incremental quadrature linear encoder of the wire scanner system provides 1 μm position resolution [1].

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Real-time position capture is done through a common platform carrier board with an FPGA on an ATCA crate. The ATCA crate is shared between different subsystems. The data is read in from a rear transition module (RTM) specific to an application (see Fig. 3). The captured data is put in a ring buffer and processed by the EPICS virtual IOC running on the real- time Linux machine (LinuxRT). The FPGA intercepts and re-transmits the encoder signal back to the motion controller to close the feedback loop. The position data is processed by the beam synchronous acquisition (BSA) system on the FPGA. The common platform system allows for the installation of AMC cards (high speed- digitizers) which can provide application-specific functionality to interface with the FPGA. The wire scanner system utilizes one of these standard AMC cards that provides 3 channels of 350Ms/s 16-bit ADC card through which beam loss monitor signal is read into the system in a beam-synchronous manner.

The FPGA on the ATCA crate performs checks on the speed of the wire scanner to prevent the destruction of the wires during continuous wave beam operations. For LCLS-II high beam repetition rates which may reach up to 1MHz the wire should move faster than a prescribed minimum speed in order to ensure that no more than 100 consecutive bunches hit the wire and yet slow enough that a sufficient number of bunches hit the wire to reconstruct the transverse profile [5].

The machine protection application for the FWS is to protect the wires, high-level application (HLA) software will make a determination for the minimum speed requirements based on bunch charge and repetition rate at the time the scan is requested, and transmit this value to the FWS firmware [6]. The FWS firmware will measure the wire speed approximately 1 ms before the wire intercepts the beam and send a message to the MPS to abort the beam if the minimum speed is not met.

Integration of FPGA Controls in EPICS

The Common Platform Software (CPSW) provides an interface for EPICS to the FPGA [7]. Definitions of registers and required parameters are defined in a YAML file. Asyn based EPICS module called YCPSWASYN is used for FPGA register access and asynchronous messaging.

High Level Application

A Matlab application is used to configure and initiate a scan. The wire scan application selects the wires and appropriate speed of the motor based on beam rate. The wire scanner moves at a maximum possible speed between wires and at the requested scan speed around the nominal wire positions. A snapshot of the high level graphical user interface along with a wire scan trajectory is shown in Fig. 5. The high-level application also calculates the beam profiles and transverse emittance with the synchronously acquired position and beam loss data [1].

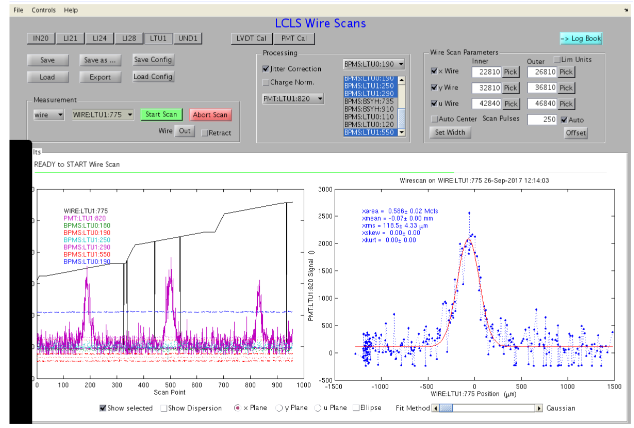

Figure 5: Matlab High Level Application depicting a wire scan.

CONCLUSION

The control system for LCLS-II Fast Wire scanner system marks a significant upgrade to the motion control drive of LCLS wire scanners, with increased performance, throughput, and safety features. Five wire scanners in LCLS have been successfully upgraded to LCLS-II style motion control system as of the final run of LCLS in December 2018.

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