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TIMING SYSTEM UPGRADE FOR MEDICAL LINEAR ACCELERATOR PROJECT AT SLRI

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Abstract

A prototype of 6 MeV medical linear accelerator has been under development at Synchrotron Light Research Institute (SLRI). Several subsystems of the machine have been carefully designed and tested to prepare for x-ray generation. To maintain proper operation of the machine, pulse signals are generated to synchronize various subsystems. The timing system, based on the previous version designed on Xilinx Spartan-3 FPGA, is upgraded with better timing resolution, easier configuration with more timing channels, and future expansion of the system. A new LabVIEW GUI is also designed with more details on timing parameters for easy customization. The result of this new design is satisfactorily achieved with the resolution of 10 nanoseconds per time step and up to 15 synchronized timing channels implemented on two FPGA modules.

INTRODUCTION

Synchrotron Light Research Institute (SLRI) has been developing a prototype of the 6 MeV medical linear accelerator for cancer treatment. This project has been proposed to help increase the availability of low-cost radiotherapy machines in Thailand. The already-designed linear accelerating structure of the prototype has operating frequency at 2,998 MHz, a 3.1 MW magnetron driven by a solid-state modulator, and a hot-cathode electron gun. The prototype has a fixed-position drive stand without gantry to provide housing for the modulator cabinet for magnetron, electron gun, and an automatic frequency control (AFC) system in order to provide resonant frequency tuning. All of the subsystems, including a collimator motion control system [1], are connected to the Main Control System in a private network as shown in Fig. 1.

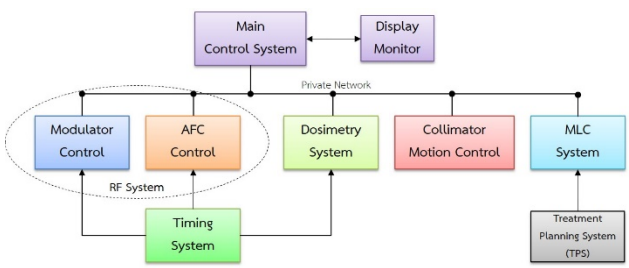

Figure 1: Network diagram of the machine prototype [1].

In order to produce X-rays to obtain the properties of the beam needed for cancer treatment using the prototype, it is necessary to produce the electron beam with the appropriate properties. The process of producing good electron beams depends on the synergy of all the subsystems, from the electron source, RF source, dosimetry system, and error detection and interlocking system. The timing system that provides synchronization of all of the machine subsystems is indispensable, with appropriate accuracy of the timing signals connecting the subsystems. All timing signals required for individual subsystems have their specific time domain requirements. If there are no such signals, it will be very difficult to set other machine parameters in order to produce the required electron beam. This has a direct impact on the quality of cancer treatment as well.

In order to generate the required timing signals one needs to be able to adjust the resolution of the pulse width (in microseconds) and delay time. Signal period can be adjusted to determine the frequency of the main clock. Analog output voltage level can also be determined as needed with enough number of channels as required by the subsystems. Configuration of all timing signals is also important. All of these requirements can be achieved by an easy-to-use GUI that is appropriately designed to communicate with users. Existing timing system [2] has been used for testing the operation of the medical linear accelerator prototype for some time with satisfactory result.

Recently, a new timing system has been designed to achieve better performance and to serve more requirements of the machine tests. In this paper all major upgrades of the timing system for this project are described. System design, both hardware and software, is explained in the next section. Installation and result are presented in the final section.

SYSTEM DESIGN

This section describes the main upgrades and implementation, both hardware and software, of the new timing system developed in this project. New timing signal characteristics and time-domain requirement settings of the signals are also explained in details.

Hardware

The main hardware platform for the new timing system is the Xilinx's Spartan 3 FPGA development board [3, 4], which is based on the same platform chosen for the existing system. The system main clock of the FPGA main board runs at 50 MHz providing the resolution of 20 nanoseconds for time domain characteristics of the timing signals. This main system clock is multiplied by 2 in this new system so that the resolution is doubled to the order of 10 nanoseconds in order to set up the timing signals whose pulse width and delay time are of better resolution. The time-domain characteristics of individual timing signals can be set independently at the outputs of each timing module.

One FPGA module has a maximum capacity of 8 timing outputs. The parameter adjustment on the FPGA depends on serial communication via RS-232 with the single board

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computer as an intermediary between remote personal computer and the FPGA module. The remote personal computer which runs the GUI program communicates with the single board computer via Ethernet 10/100 Mbps. Synchronization between multiple FPGA modules can be done by connecting one output signal of one FPGA module as an external trigger to another FPGA module. In this development we have chosen to implement 2 modules connected in cascaded configuration to each other as shown in Fig. 2. The last output (CH8) of FPGA module 1 is chosen to be a trigger signal to FPGA module 2 for synchronization purpose. Therefore, by utilizing this synchronization configuration, the system effectively generates the total of 15 independent timing signals. In addition, both FPGA modules can communicate independently with the single board computer via their own RS-232 ports.

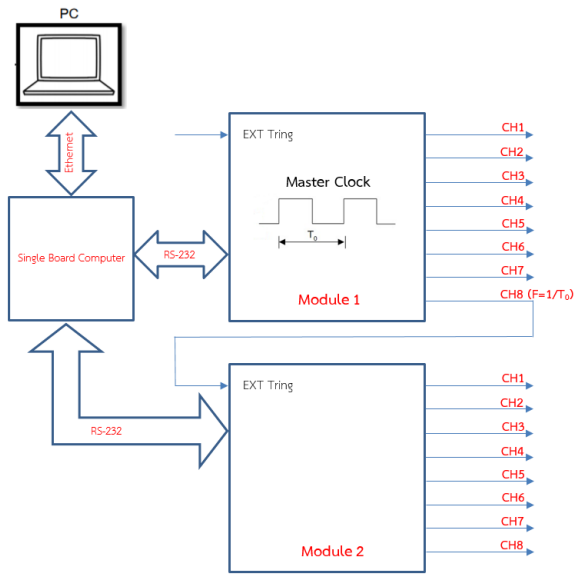

Figure 2: Timing system diagram.

The following characteristics are summarized for the timing signals generated from this system implementation:

- Parameters of the signal from each channel can be determined independently from each other.
- The output impedance of the desired channel can be chosen either 50 Ω or 1 kΩ.
- Fundamental period (T_0) for determining the frequency of the main clock signal can be specified for the frequency from 0.0002 Hz to 10 MHz.
- Delay time for shifting the desired timing signal can be independently chosen for each channel, which must be referred to the main clock signal, with a resolution of 10 nanoseconds per adjustment step.
- Pulse width of each desired channel has a resolution of 10 nanoseconds per adjustment step.
- For the channels with 50 Ω impedance output, the amplitude can be set between 2 and 20 volts.
- For the channels with 1 kΩ impedance output, the amplitude can be set between 1 and 10 volts.
- External trigger option can be enabled or disabled for individual FPGA modules (EXT Trig Channel).

The FPGA modules including a single board computer and other electrical parts are installed in a standard 19-inch equipment box. Figure 3 shows the installation of one FPGA module whose 8 timing signals and the trigger signal can be selected from SMA connectors at the back of the equipment box shown in Fig. 4.

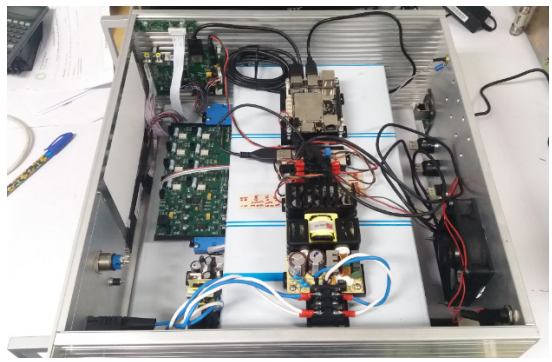

Figure 3: Installation of the timing system hardware.

Figure 4: The back side of the timing system hardware.

Software

The main software design is focused on user interface in order to set the required timing parameters of the desired timing signals. The reference design is chosen based on the existing timing system which was developed in [2] using LabVIEW 2015. Figure 5 shows the new LabVIEW GUI for the new timing system.

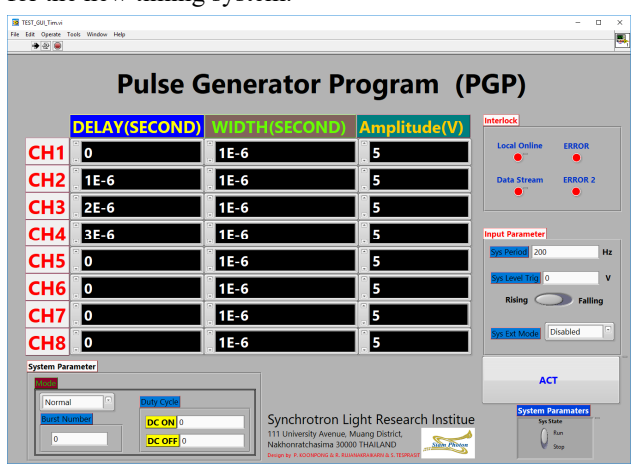

Figure 5: A new GUI of the timing system.

User can input the determined pulse width, delay time, and amplitude of the timing signal for each channel via this GUI. These parameters are subsequently transmitted via Ethernet communication to the single board computer to perform conversion and manage various interlock signals

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of the system before being sent to the FPGA modules. As discussed earlier, FPGA module 1 and FPGA module 2 communicate with the single board computer via RS-232 port 1 and port 2, respectively. Standard Commands for Programmable Instruments (SCPI) is used as a basic international standard to generate commands for communication in order to create the timing signals for this system.

The timing period T_0 is created within the FPGA module to be used as a reference for all channels. Delay time and pulse width are limited to be smaller than T_0. A VHDL function is designed and implemented in the FPGA modules to support a rate of 0.0002 Hz to 100 MHz at 10 nanoseconds resolution. It also supports Burst Mode from 1 pulse to 9,999,999 pulses on the time-base basis. The outputs of the system can be chosen as a single pulse mode or burst mode, with additional information on duty cycle. The external trigger is also supported in the FPGA modules. The trigger input can handle the maximum frequency of 100 MHz. Rising-edge or falling-edge mode for the external trigger signal can be easily chosen with the maximum voltage of 15 Vdc.

INSTALLATION AND CONCLUSION

Figure 6 shows the installation of all hardware cabinets and other necessary electrical equipments in a standard 19-inch rack. The overall performance and time-domain characteristics of the timing signals generated from this system are satisfactorily achieved as desired. The concurrent operation of the multiple timing channels including the pulse width and delay time can be obtained similarly to the existing system. With this new design the timing resolution of 10 nanoseconds for each step size adjustment is achieved as expected. The output voltage level of all timing channels can be easily customized. In addition, the synchronization option of two FPGA modules provides us flexibility to select and utilize more timing signals which will be required as the medical linear accelerator with multiple subsystems can be expanded, either for system test or commissioning purposes, in the future.

Figure 6: Timing signal module installation.

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