The European Synchrotron

# REFURBISHMENT

# OF THE ESRF ACCELERATOR SYNCHRONISATION SYSTEM

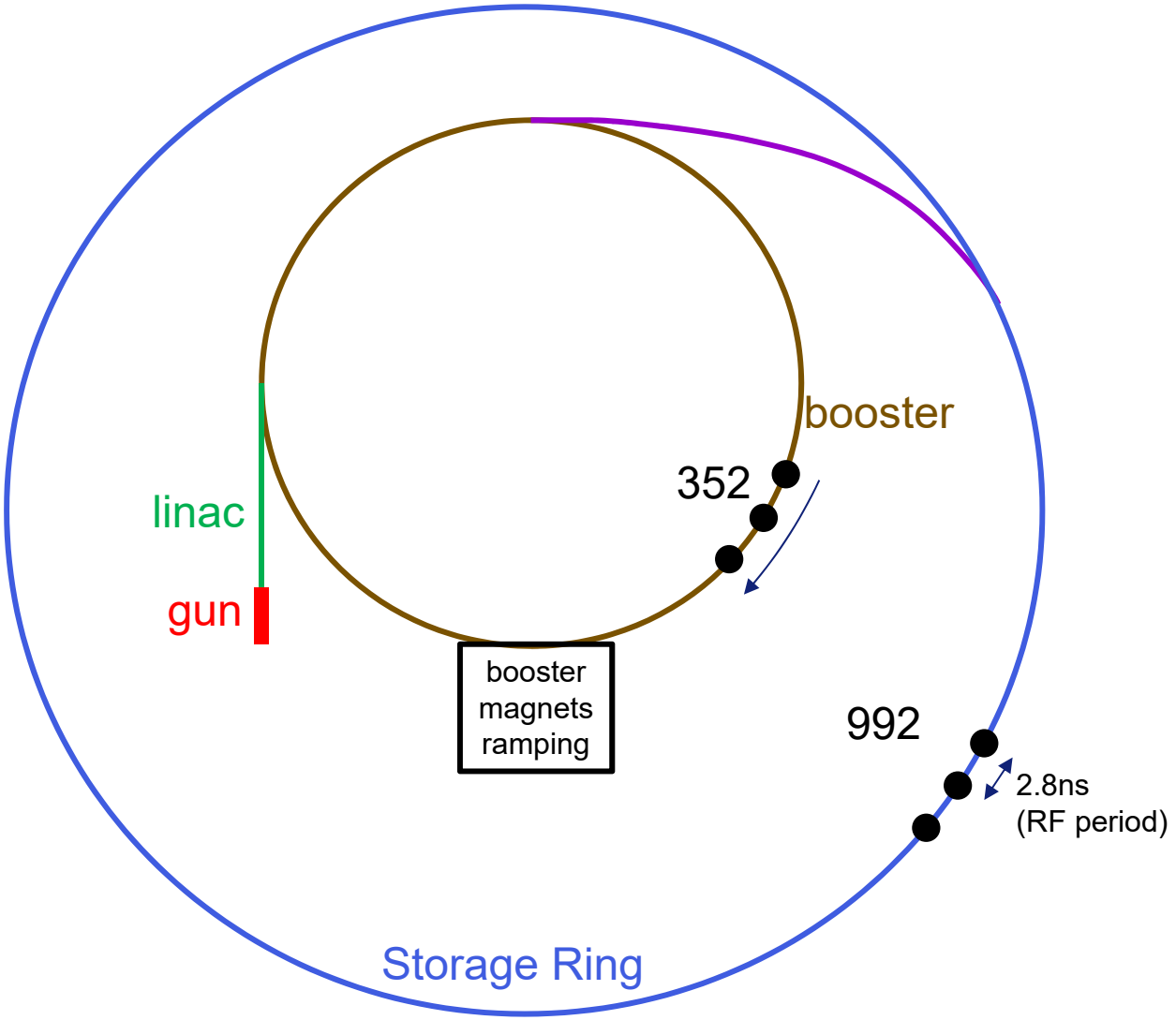
# USING WHITE RABBIT

G.Goujon, N.Janvier, A.Broquet - ESRF

# OUTLINE

- ESRF SYNCHRONISATION & TIMING SYSTEM
- DESIGNING A NEW SYSTEM
- WHITE RABBIT BASED SOLUTION
- NEW HARDWARE: THE WHIST MODULE
- FORESEEN ARCHITECTURE
- FIRST RESULTS
- CONCLUSION

## THE SYNCHROTRON TIMING SYSTEM



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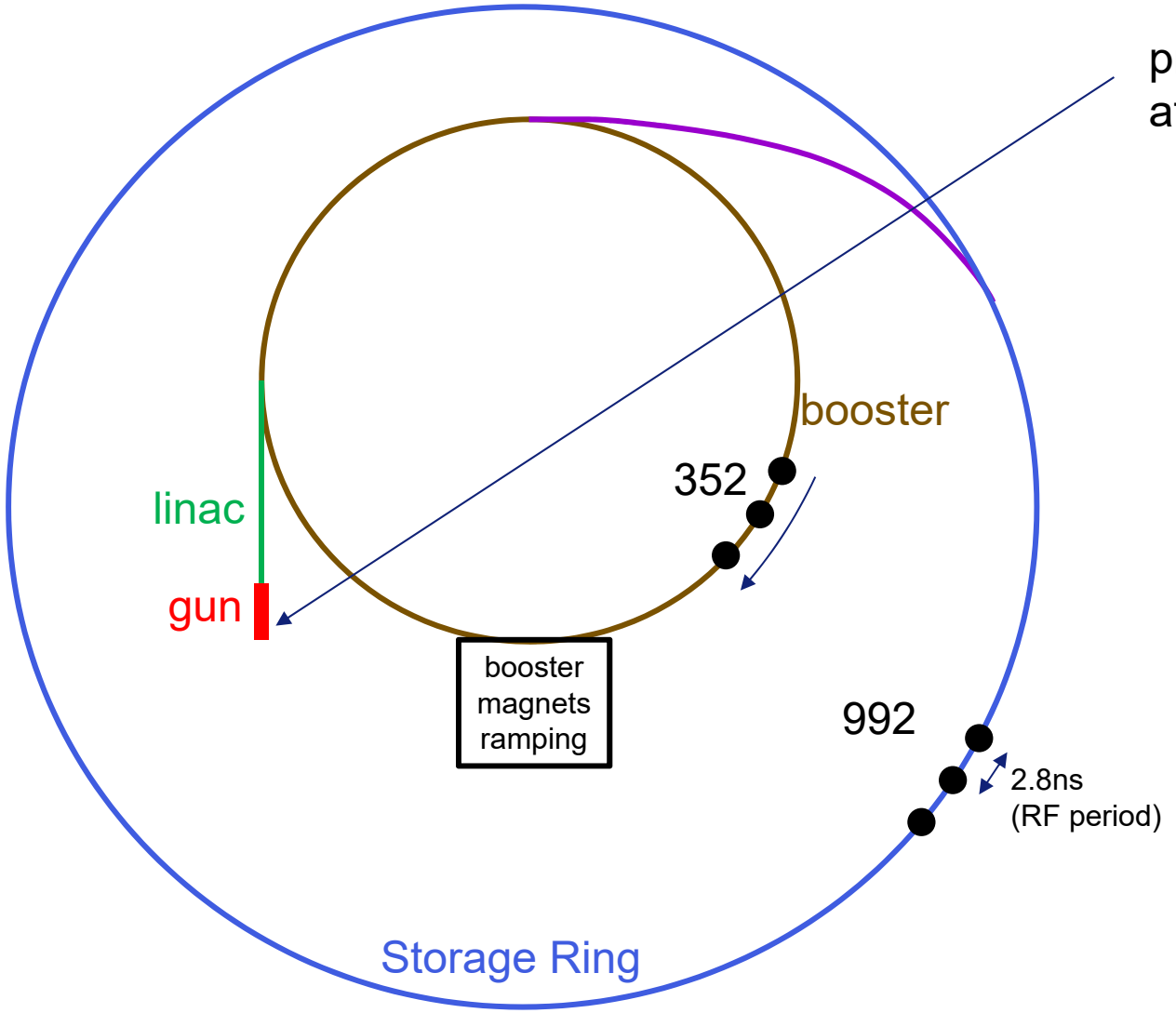

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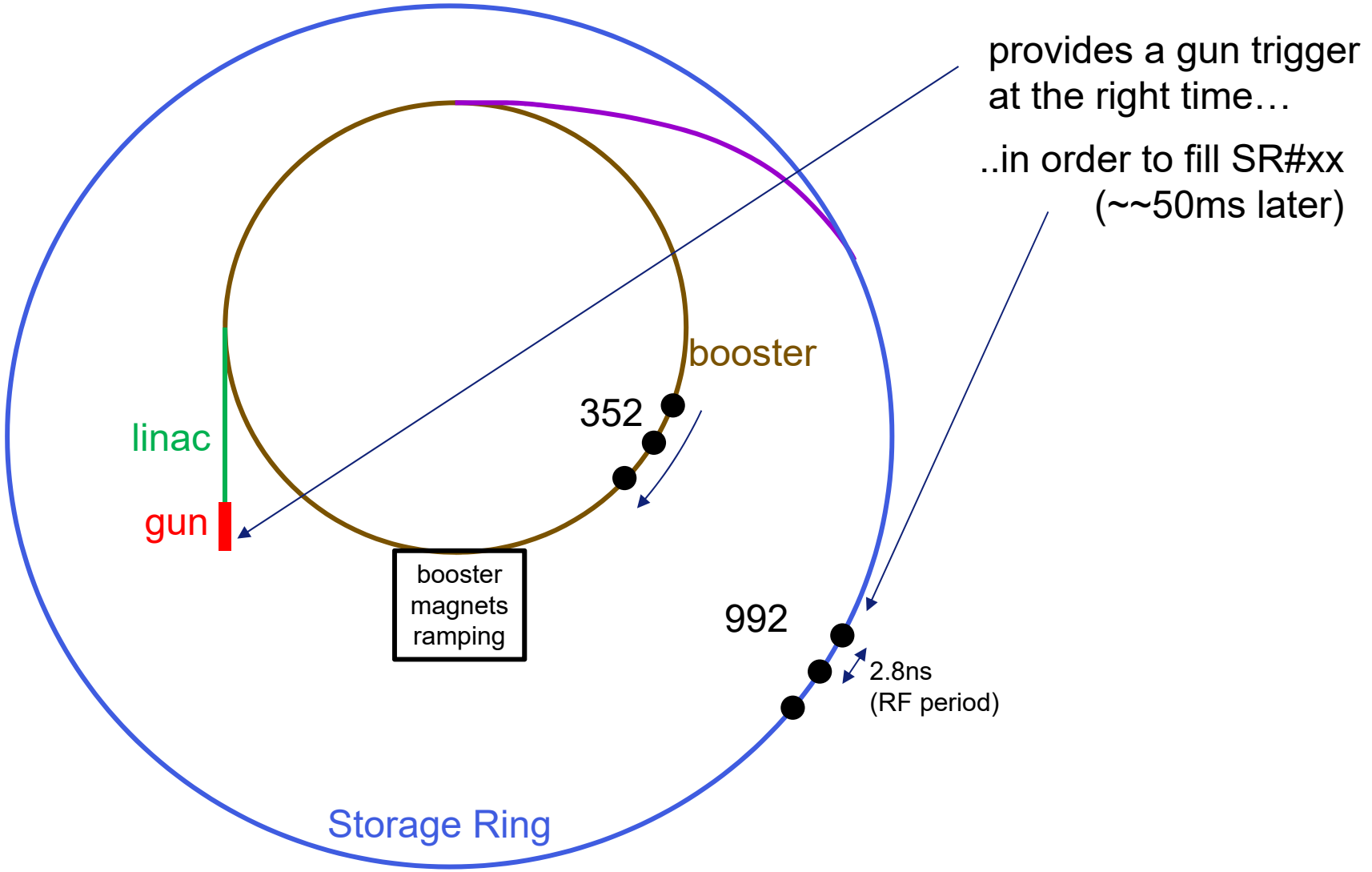

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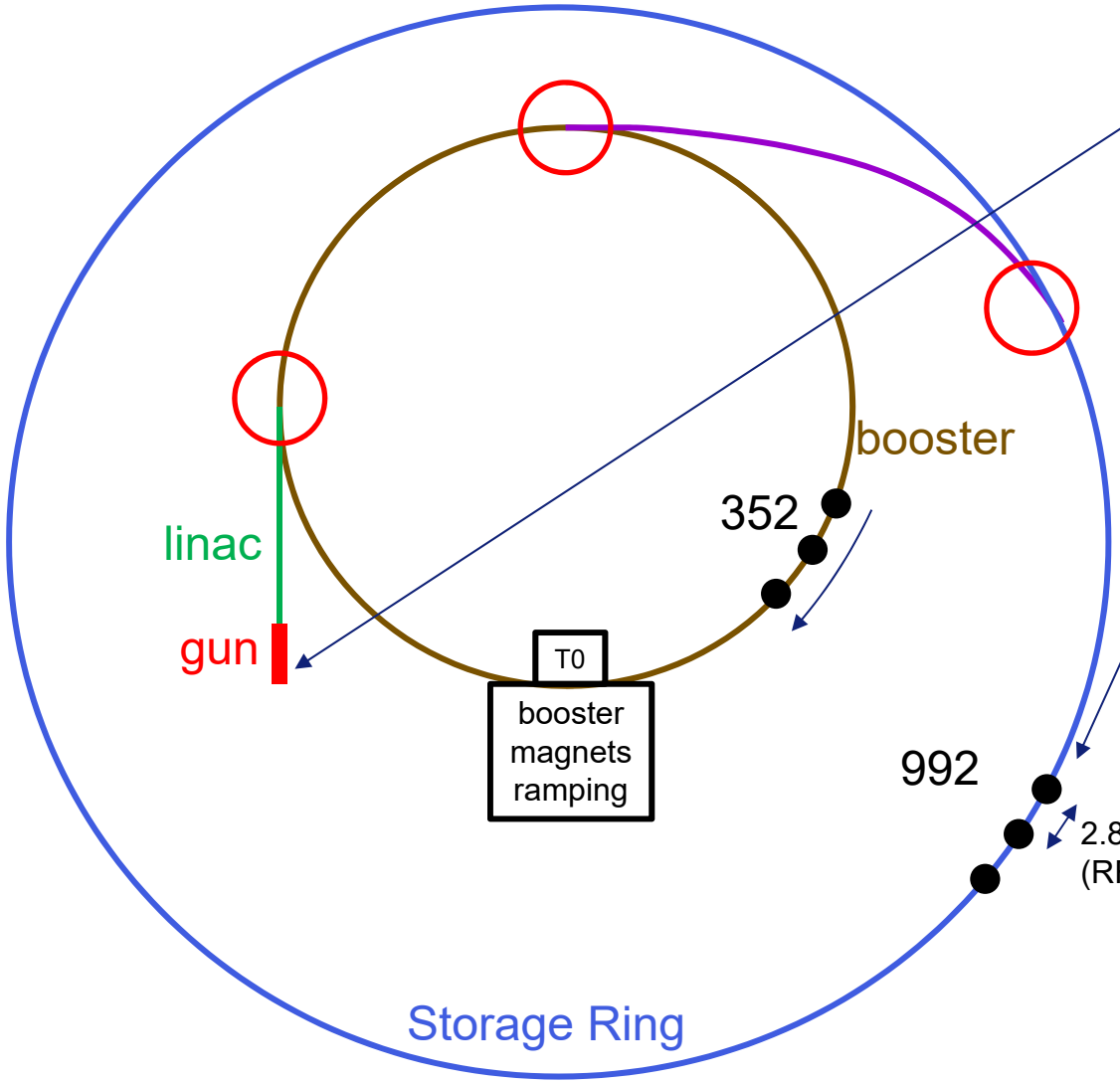


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taking care of :
transfer locations
booster_ramp_start (T0)

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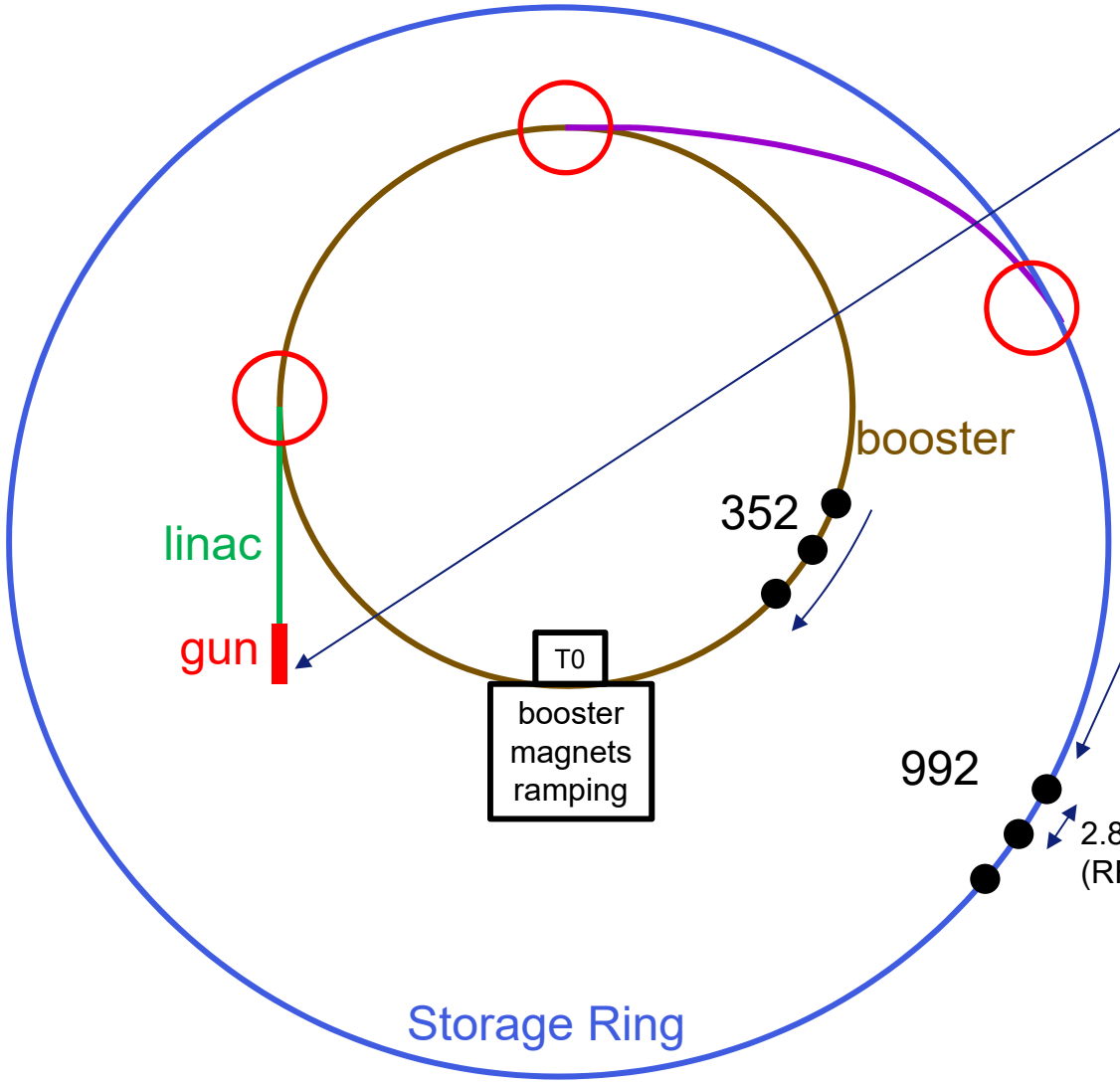


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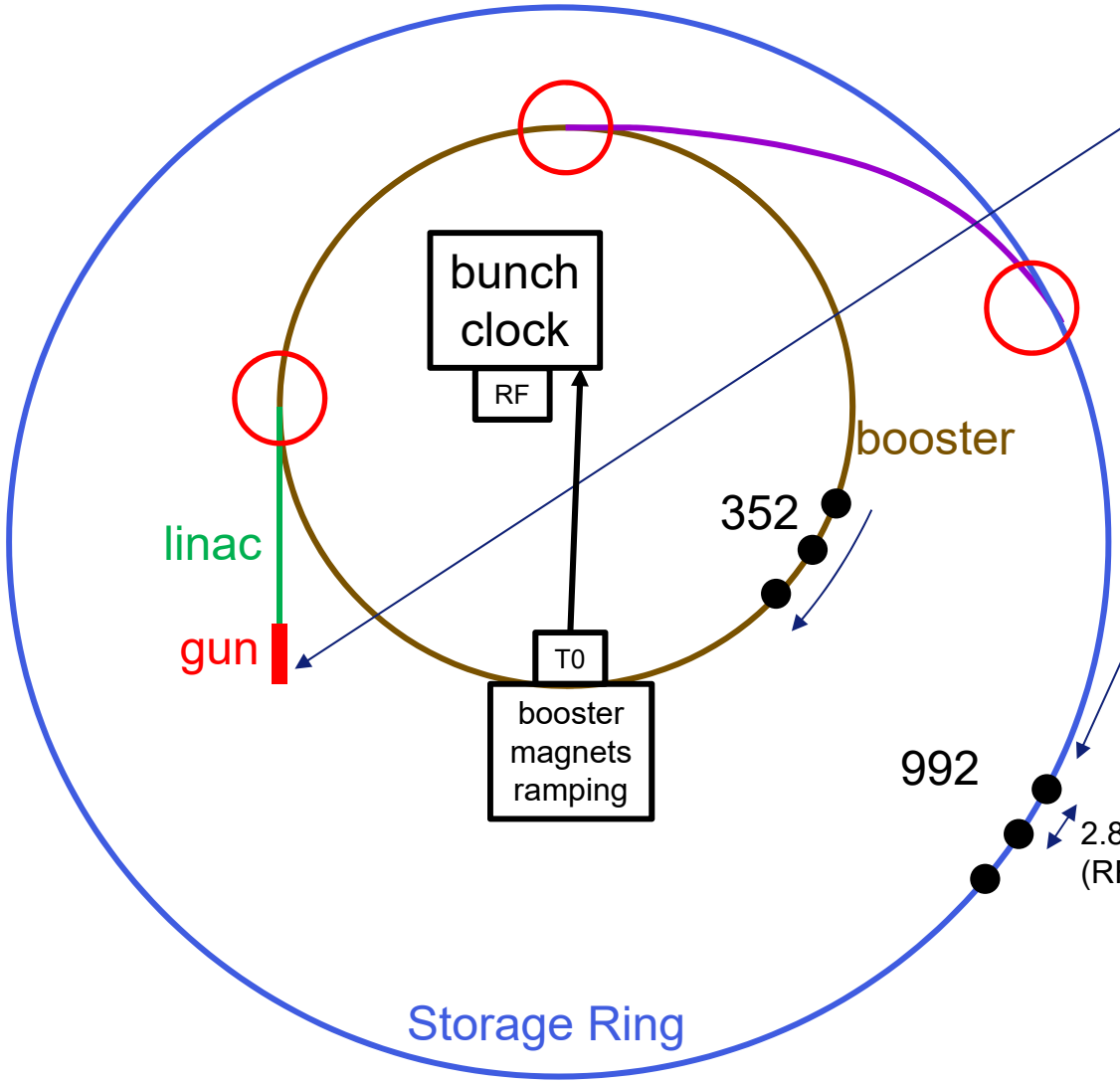


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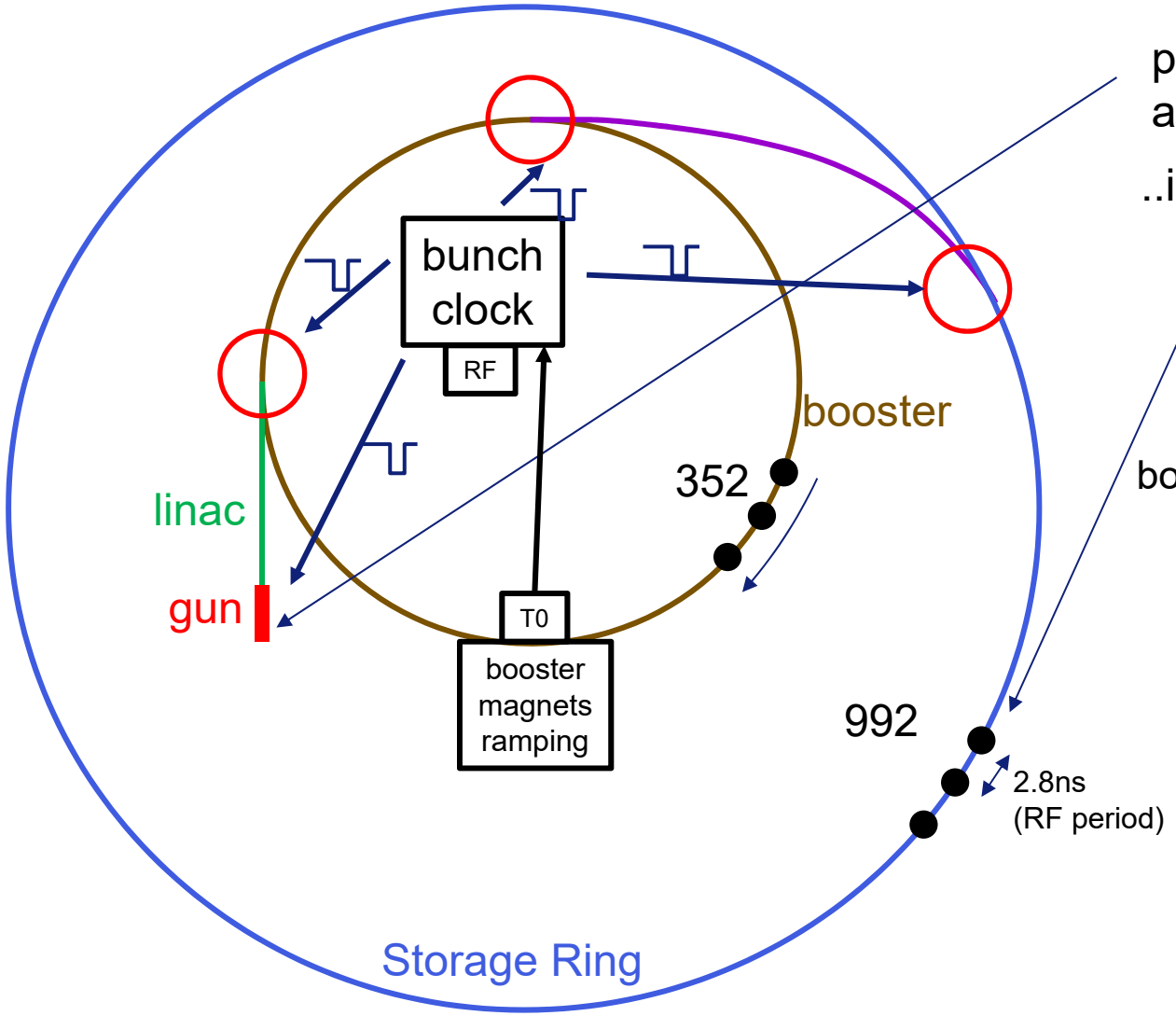


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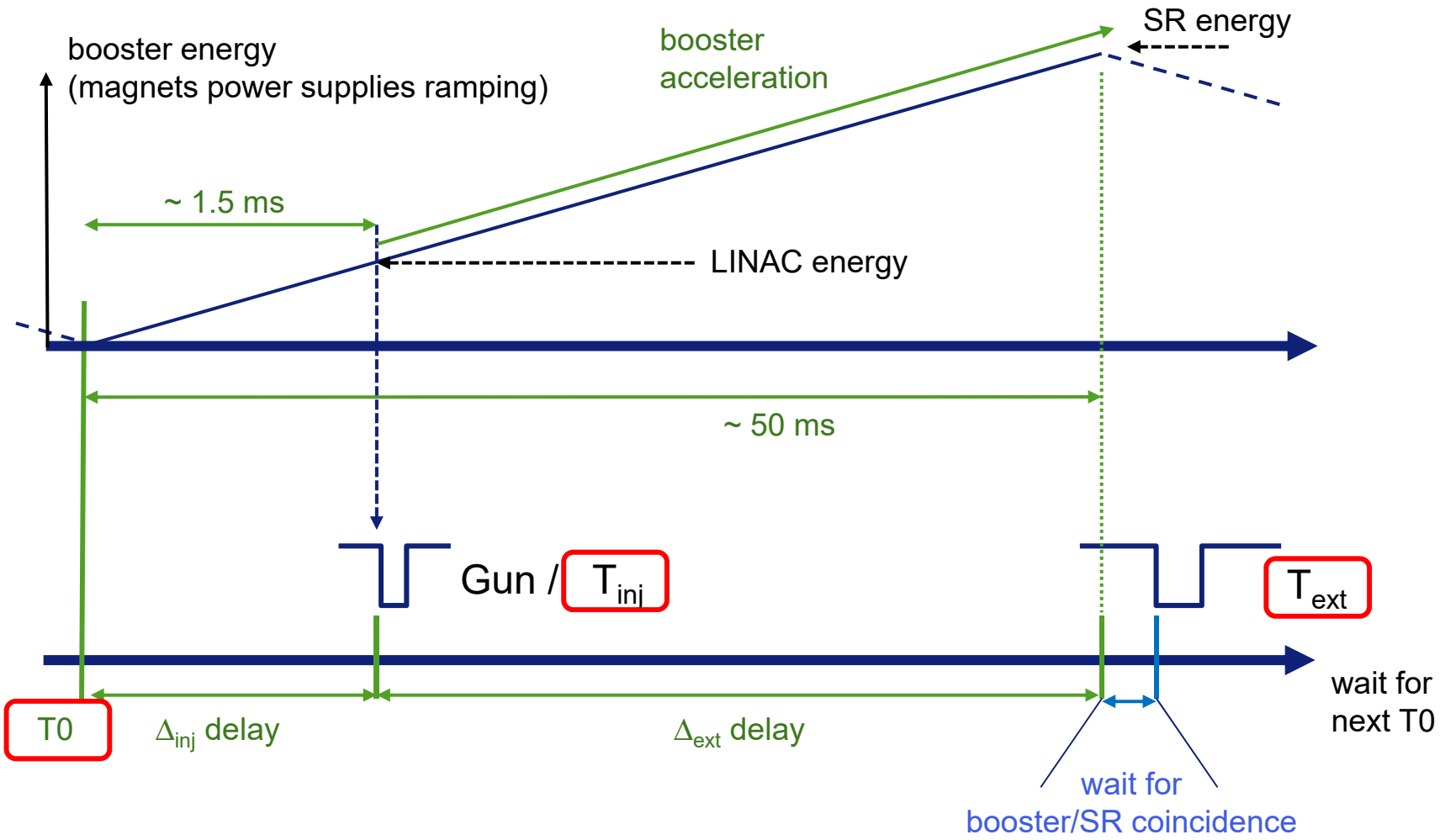
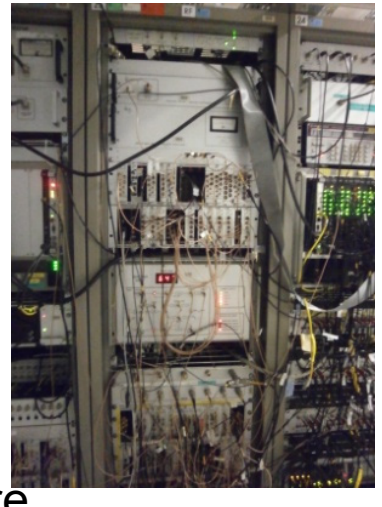
. trigger pulses distributed copper links

# ESRF SYNCHRONIZATION AND TIMING



# WHY A NEW SYSTEM ?



## THE PRESENT SYSTEM IS PROVEN TO BE RELIABLE , BUT …

## GETTING OBSOLESCENT & PRESENTS LIMITATIONS

- frozen design : no new feature possible
- 1 signal = 1 cable : no flexibility
- new needs for synchro signals = specific electronics everywhere
- no time stamping of events (faulty device, beam lost etc)

## EMERGING NEEDS FROM THE BEAMLINES

- accelerator related gating (stop data acquisition during top up injections)
- synchronous detection for S/N improvement
- time stamping

# WHITE RABBIT BASED NEW TIMING SYSTEM

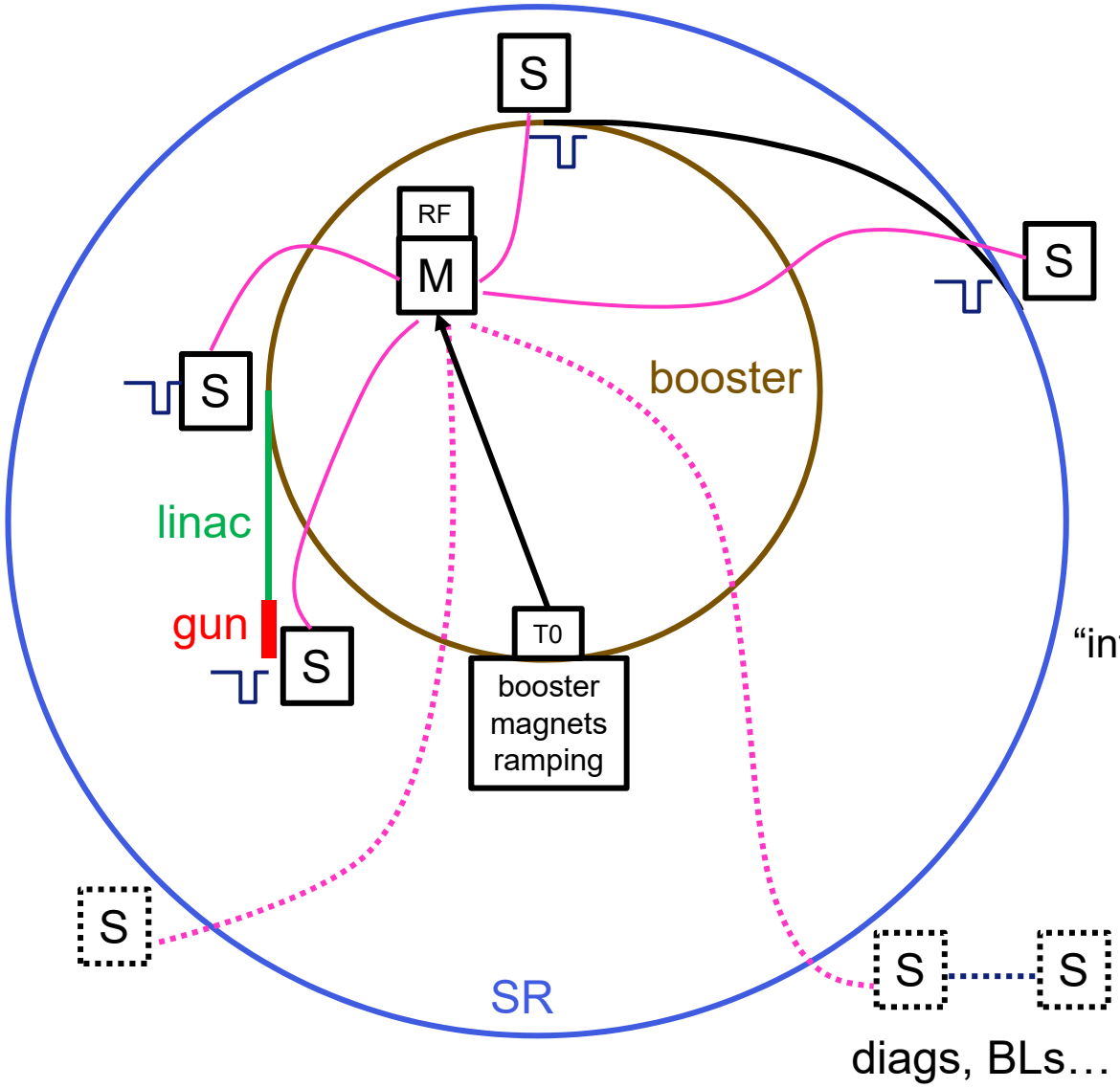
## White Rabbit SELECTED FOR ESRF REFURBISHMENT

- High flexibility
- Outstanding  time stamping capabilities for ESRF needs
- Compatible optical fibre network already in place
- Available hardware allows “simple” in-house development -> WHIST module
- FPGA flexibility to add specific new features
- Open-Hardware - multiple suppliers

## White Rabbit SOLUTION BUILDING BLOCKS

- SPEC boards / large FPGA (SPARTAN-6 LX100T)
- “RF over ETHERNET” (Distributed Direct Digital Synthesis / D3S)
  **highly efficient support from CERN**
- FMC-DDS mezzanine boards available for RF over Ethernet evaluation

# WHITE RABBIT ESRF ARCHITECTURE




**optical fibre network** :
1 master (CTRM)
+ satellite slaves
*(WR switches not shown)*

**MASTER** manages
RFoE
“booster_ramp_start” (T0)

“intelligent” **SLAVES** manage :
time (RF+UTC)
time stamping of inputs
main sequencer
local pulse production

# SPECIFICATION

- **ONE UNIQUE STAND-ALONE MODULE FOR MASTER & SLAVE**
  - 19 inch 1U

- **EXISTING SEQUENCER EMBEDDED**
  - preserve fine delay adjustment (10ps steps) on some outputs

- **INPUTS/OUTPUTS**
  - as many outputs per module as possible (ideally => 12)
  - ESRF standards : TTL + ECL

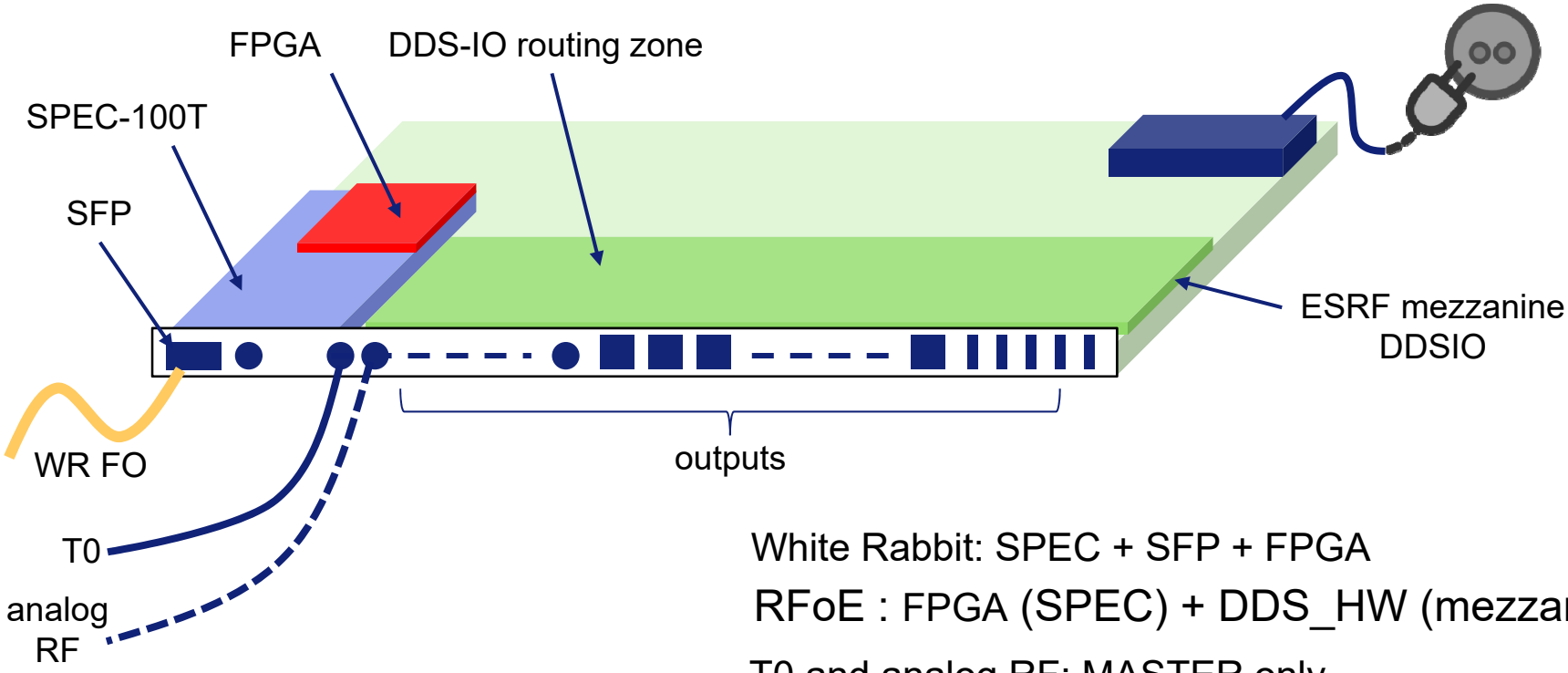
- **DISTRIBUTED ARCHITECTURE**
  - The main sequencer is duplicated **locally** (in all slaves)
    - local pulses are programmed from common sequencer main parameters :
      . T0, Inj and Ext triggers

    - RF counters (= RF time base) in phase everywhere

  - Allows "HOT PLUG" of a new module in a running network

    *auto alignment of local RF counter to network RF counters*

# WHIST STAND-ALONE MODULE




White Rabbit: SPEC + SFP + FPGA

RFoE : FPGA (SPEC) + DDS_HW (mezzanine)

T0 and analog RF: MASTER only

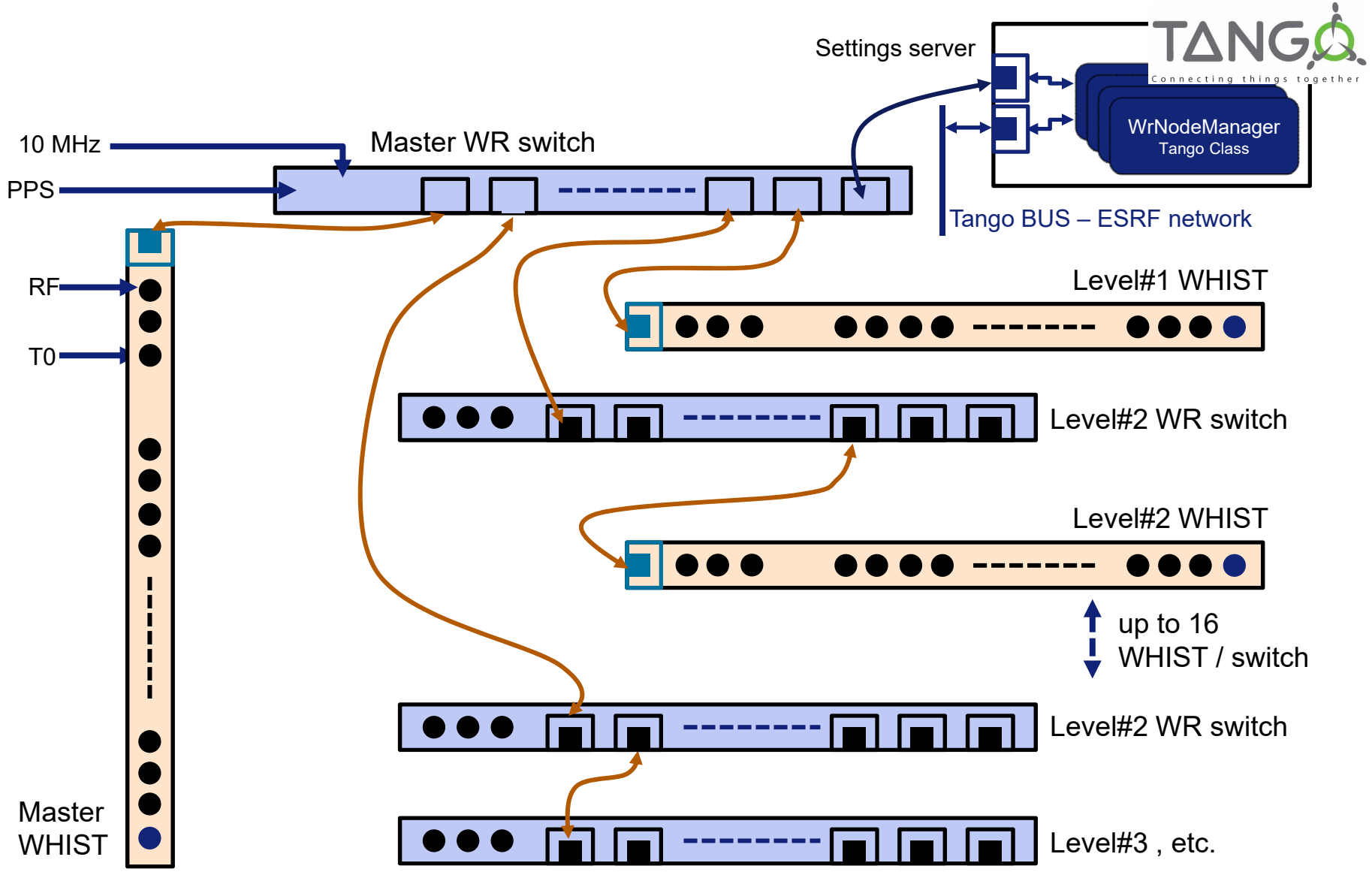
## DDS-IO ELECTRONICS:

- Duplicates FMC-DDS open hardware
- Has its own power supplies
- Saves FMC connector pins by reallocating fine delay bus ➔ I2C
- Provides 12 programmable Outputs (TTL / translated ECL) & 4 inputs

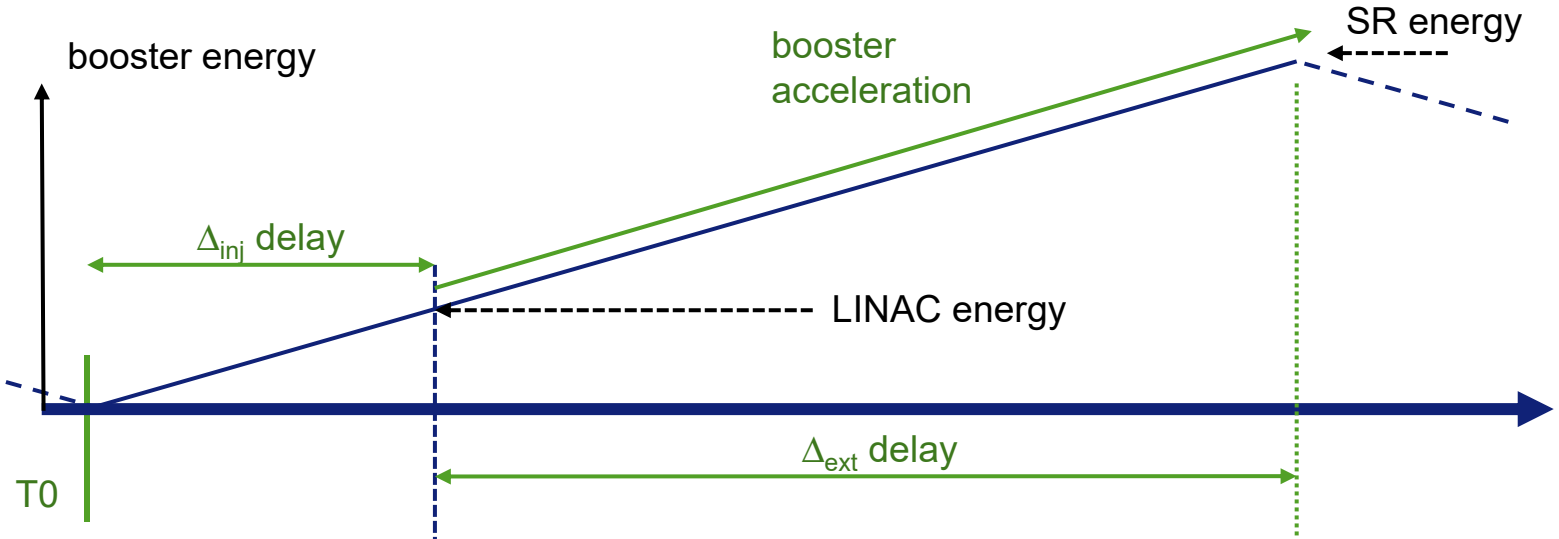
# WHIST MODULE


- Dedicated RF input
- 4 inputs (2xSMA; 2xLEMO) supporting time stamping (RF or WR clock domain)
- RF and RF/n outputs (from PLL : optimum phase noise)
- 12 programmable outputs
  - “translated ECL” (50 Ω to GND terminated) : SMA connector
  - TTL : LEMO connector. (some are duplicated : ECL+TTL)
- Pulse programming :
  - polarity
  - delay with respect to : T0 / Injection / Extraction
  - pulse width

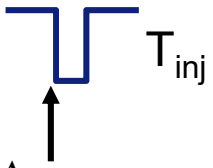
# WHITE RABBIT ESRF – FORESEEN ARCHITECTURE



$\Delta_{inj}$ , $\Delta_{ext}$ = network configuration parameters

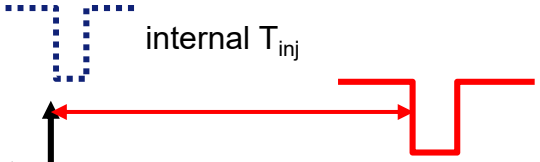



master :
stamps T0
broadcasts “T0_stamp”
calculate T0-stamp + $\Delta_{inj}$
RF_counter = T0_stamp + $\Delta_{inj}$

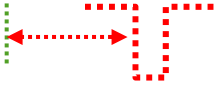




slaves :
receive T0_stamp
calculate T0_stamp + $\Delta_{inj}$
RF_counter = T0_stamp + $\Delta_{inj}$



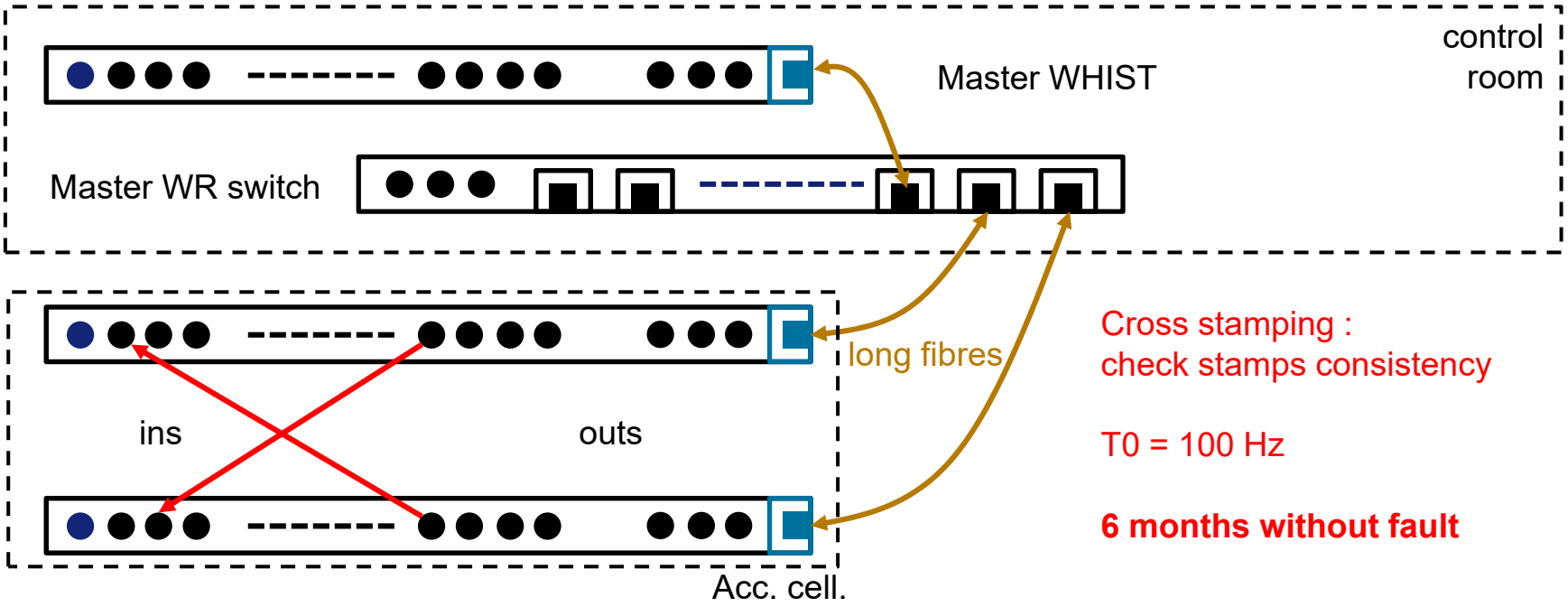

output pulse : programmed delay & width ($/T_{inj}$)



output pulse / $T_{ext}$

# SOME RESULTS

## VALIDATION TESTS




Cross stamping :
check stamps consistency

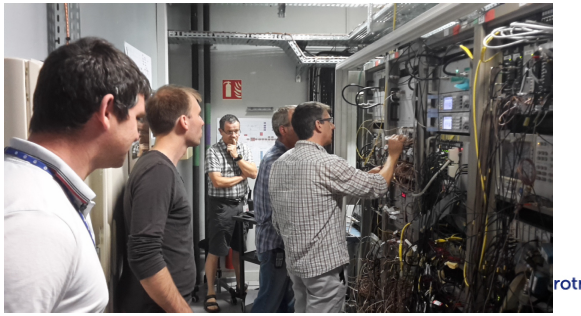
T0 = 100 Hz

**6 months without fault**

## PHASE NOISE

measured on clock outputs : =< 10 ps RMS (10 Hz – 1 MHz)
to be improved  with WHIST V2.1 RF PLL

## FIRST BEAM SUCCESSFULLY INJECTED





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# CONCLUSION

- **White Rabbit SELECTED FOR ESRF SYNCHRONISATION SYSTEM**

- **MORE VALIDATION STILL TO BE PERFORMED**

  . Test / implement all SR filling patterns
  . Validate full compatibility with existing cabling
  . Test / validate new TANGO application

- **REFURBISHMENT PLANNING**

  - phase#1 : replace the “Bunch Clock” core : H1 2018 ➔ ESRF still in operation
  - phase#2 : install the full new network during EBS shutdown
  - restart in 2020 with phase#1 configuration then switch networks
  - next: extend new network to Beamlines

**A BIG THANKS to Javier SERRANO and his team for the active collaboration !**

# THANK YOU FOR YOUR ATTENTION