Timing System at ESS

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The European Spallation Source (ESS) timing system is based on the hardware developed by Micro-Research Finland (MRF). The main purposes of the timing system are: generation and distribution of synchronous clock signals and trigger events to the facility, providing a time base so that data from different systems can be time-correlated and synchronous transmission of beam-related data for for different subsystems of the facility. The timing system has a tree topology: one Event Generator (EVG) sends the events, clocks and data to an array of Event Receivers (EVRs) through an optical distribution layer (fan-out modules).
The event clock frequency for ESS will be 88.0525 MHz, divided down from the bunch frequency of 352.21 MHz. An integer number of ticks of this clock will define the beam macro pulse full length, around 2.86 ms, with a repetition rate of 14 Hz. An active delay compensation mechanism will provide stability against long-term drifts. A novelty of ESS compared to other facilities is the use of the features provided by EVRs in μTCA form factor, such as trigger and clock distribution over the backplane. These EVRs are already being deployed in some systems and test stands.

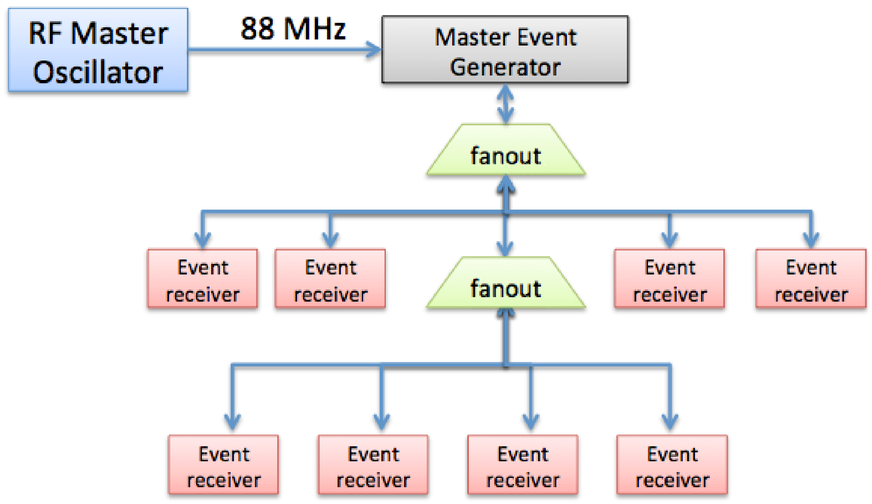
Timing system functionality

- Trigger event distribution: Trigger events define the accelerator sequence timeline. EVRs act based on these triggers, by driving outputs high and low, or triggering them with user-defined width, delay and polarity.
- Data distribution: Beam-related information for each pulse is broadcasted before the actual pulse is emitted. Devices can prepare for each individual pulse, and even raise a flag if they are not ready for it.
- Timestamping: A timestamping mechanism distributes a common ”wall-clock” time to the whole facility. This time is used for timestamping events and actions, and is derived from GPS. It is incremented internally but periodically re-synchronised with GPS to avoid drifting too far away from the GPS-defined time.
- Distribution of clock signals: Up to 8 RF-synchronous clock signals can be distributed globally or created for an individual EVR. They are sampled at half the event clock frequency.
- Delay compensation: An active delay compensation mechanism provides stability against long term drifts caused mainly by thermal changes.

Technical details

Data item	Value
Proton beam pulse frequency	14 Hz
Proton beam pulse max length	2.86 ms
RF master clock frequency	352.21 MHz
Timing event clock frequency	88.0525 MHz
Timing event clock period	11.357 ns
Timing clock ticks in one proton beam cycle	6289464

Timing system architecture



Beam parameter data

Data item	Format
Beam repetition rate	Unsigned integer (Hz, 1-14)
Beam present	Boolean
Accelerator mode	Enumerated integer
Beam envelope mode	Enumerated integer
Pulse length	Float (ms)
Proton energy	Float (MeV)
Raster pattern	Enumerated integer
Target segment	Unsigned integer

Accelerator mode

Name	Description
Shutdown	Ion source, most components off, except non-hazardous systems. Tunnel access possible.
RF Power	RF systems could be on, but proton production off. Intended for RF test.
Source	Source plasma on, no beam extraction. Access to tunnel (but not source cage) possible.
Studies Dump	P-beam to Tuning dump; tunnel closed. Access to LoS instruments only if primary shutters closed.
Studies Target	P-beam to target. Target areas and tunnel ”searched and locked”; no access to LoS instruments.
StartUp Target Test	Same as Studies Target.
StartUp Low Power	Same as Studies Target
StartUp Ramping	Same as Studies Target.
Production	Same as Studies Target. Neutron production.

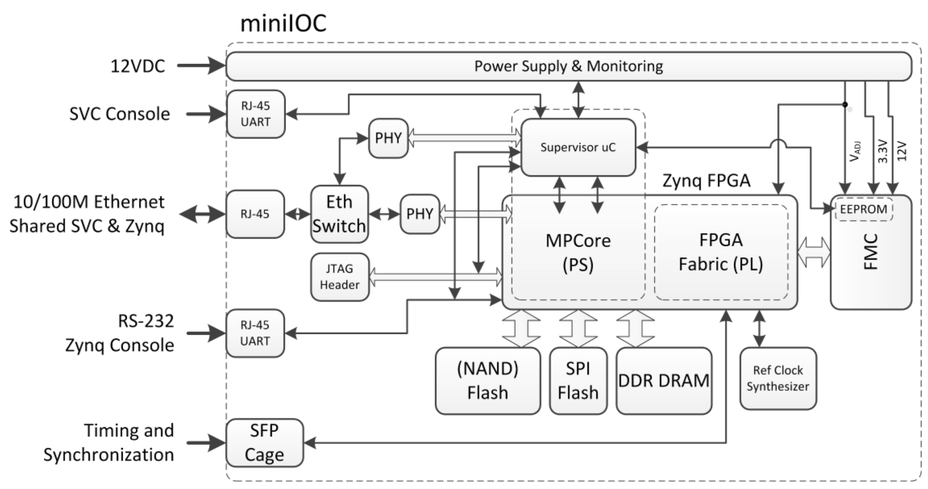
Beam envelope mode

Name	Description
No beam	
Probe beam	0 to 5 μs, 0 to 1Hz
Fast tuning	0 to 5 μs, 0 to 14 Hz
Slow tuning	0 to 50 μs, 0 to 1 Hz
Long pulse verification	2.86 ms, 1/30 Hz
Shielding verification	Low power, 30 kW
Production	2.86 ms, [1-14] Hz, 5MW

Other characteristics

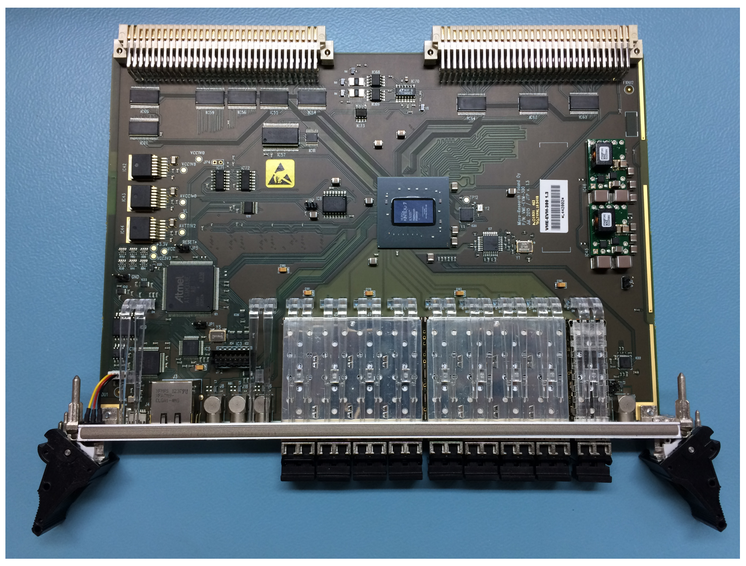
- EPICS integration: the Experimental Physics and Industrial Control System (EPICS) is used at ESS; the EPICS integration of the timing system is realised by the *mrfioc2* driver.
- Standalone mode: the MTCA-EVR-300 and PCIe-EVR-300DC EVRs have a sequencer implemented, which is usually triggered by prescalers that divide down the frequency generated by a fractional synthesizer that is present in the EVR,to provide a 14 Hz event that mimics the beam cycle, which is used to trigger different outputs. Harmonics of this frequency are usually also implemented.
- Uplink stream: it is used as a fast communication mechanism to inform the EVG mainly about hardware or other type of failures and trigger the *post mortem* functionality. The events are triggered from the EVRs’ TTL inputs, specially by the machine protection system and interlock system.

Mini-IOC

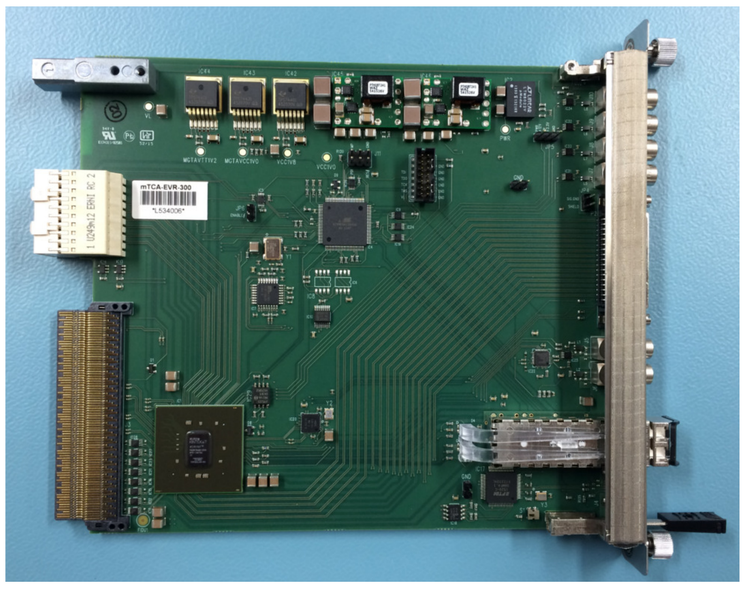


Hardware

VME-EVM-300



MTCA-EVR-300



PCIe-EVR-300DC