



A REAL-TIME, DISTRIBUTED POWER MEASURING AND TRANSIENT RECORDING SYSTEM FOR ACCELERATORS' ELECTRICAL NETWORKS

E. Freddi, O.O. Andreassen, K. Develle, J. Lahaye, I. Mätäsaho, A. Rijllart
CERN, CH-1211, Geneva 23, Switzerland

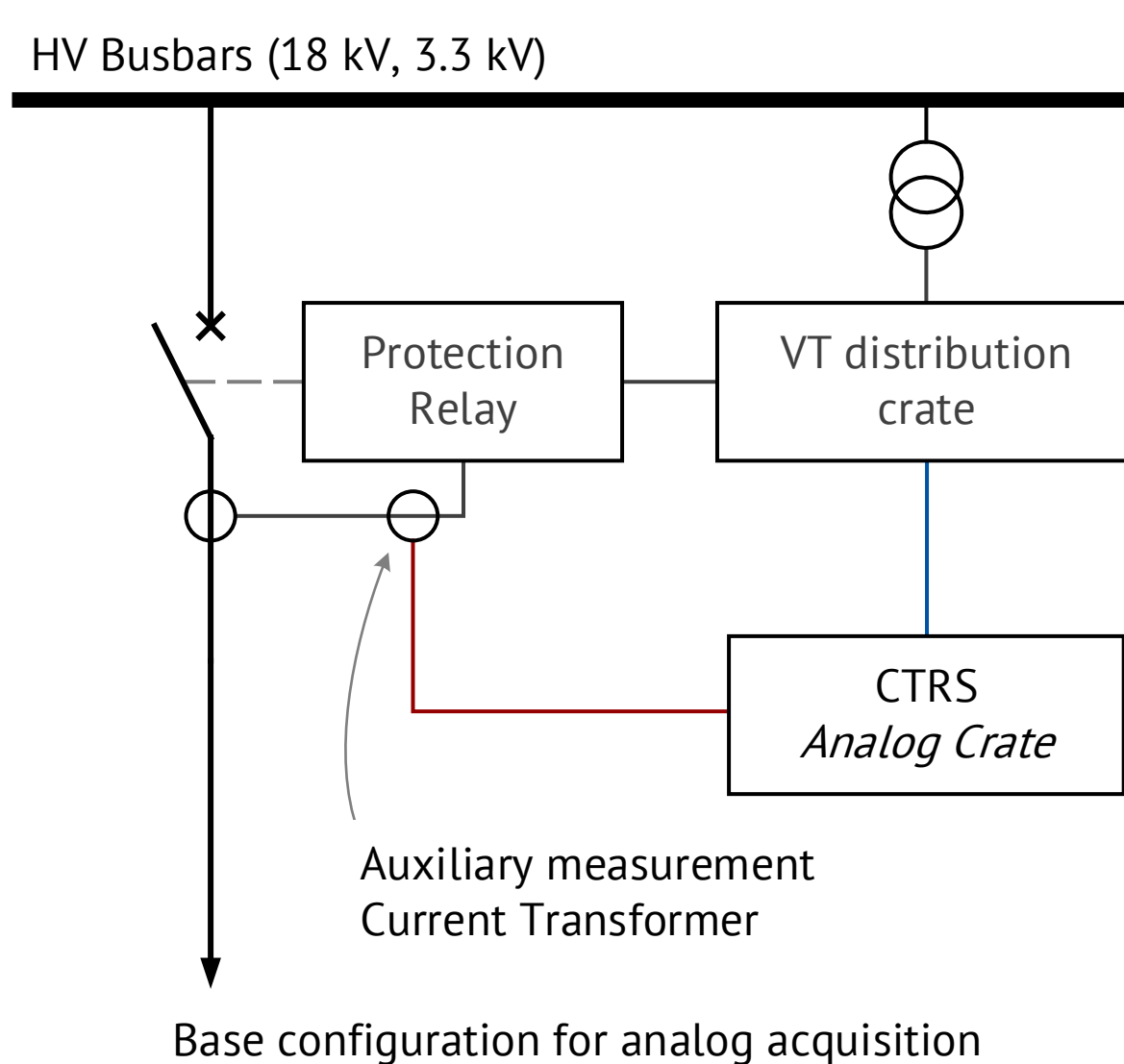
ABSTRACT

Particle accelerators are complex machines with fast and high power absorption peaks. Power quality is a critical aspect for correct operation. External and internal disturbances can have significant repercussions causing beam losses or severe perturbations. Mastering the load and understanding how network disturbances propagate across the network is a crucial step for developing the grid model and realizing the limits of the existing installations. Despite the fact that several off-the-shelf solutions for real time data acquisition are available, an in-house FPGA based solution was developed to create a distributed measurement system. The system can measure power and power quality on demand as well as acquire raw current and voltage data on a defined trigger, similar to a distributed oscilloscope. In addition, the system allows recording many digital signals from the high voltage switchgear enabling electrical perturbations to be easily correlated with the state of the network. The result is a scalable system with fully customizable software, written specifically for this purpose. The system prototype has been in service for two years and full-scale deployment is currently ongoing.

HARDWARE SETUP

Connection to the Power System

In its base configuration, the CTRS acquires three phase voltages and currents directly from the voltage and current transformers already installed in the cubicles. It is capable of recording binary inputs such as circuit breaker statuses.



Short-circuit withstand is mainly achieved by using a measurement CT whose saturation limits the thermal stresses on the transducers.

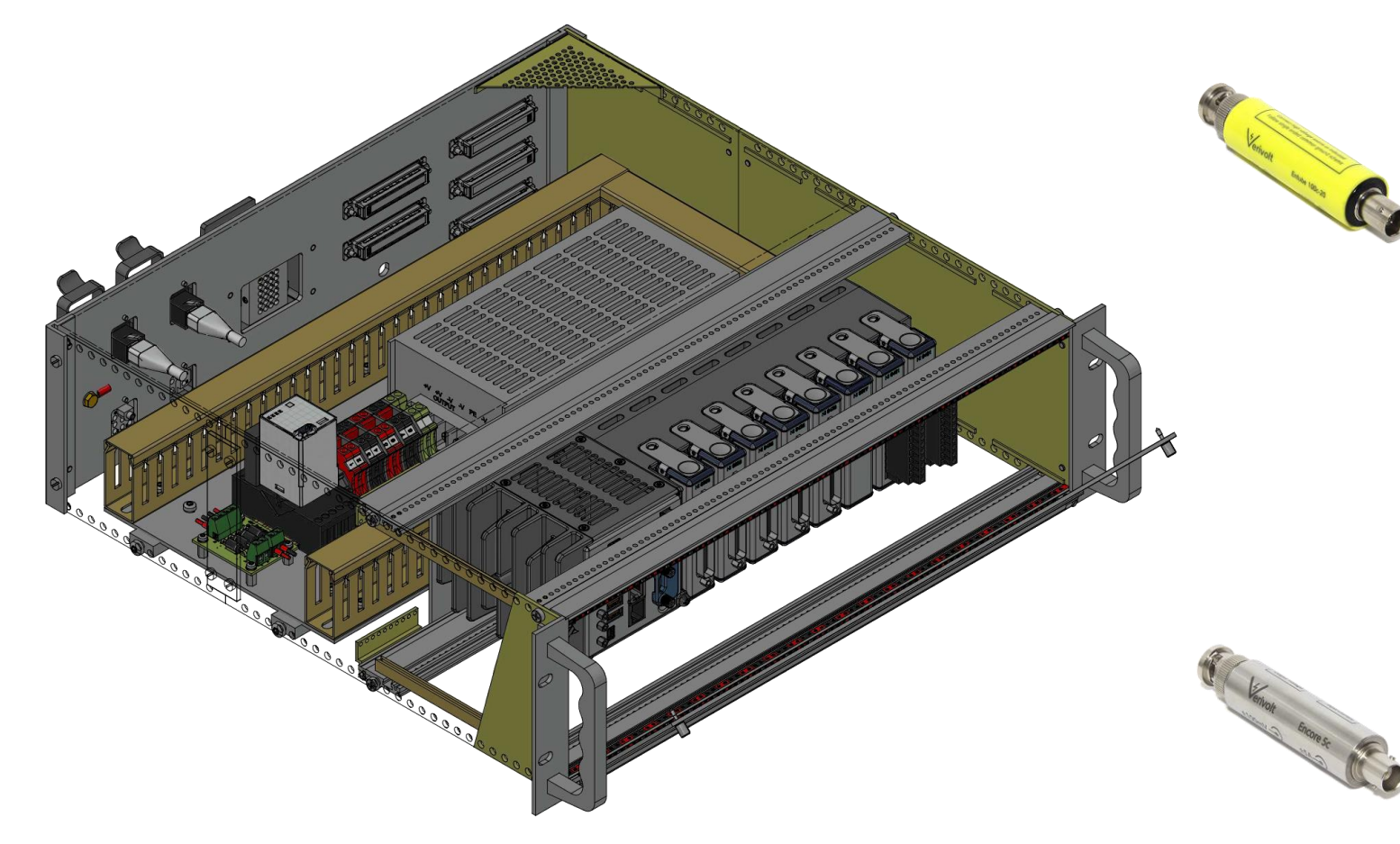
Overvoltage withstand is ensured by the transducers that tolerate up to 500 V for 10 s. A low-pass second order filter tuned at 5 kHz is implemented in the voltage probes.

Sampling frequency
7.8 kHz

Synchronization accuracy
< 2 ms

Global triggering delay
< 10 ms

Data rate
1.25 Mb/s



Voltage channels count
32

Voltage rating / withstand
100 V / 500 V_{10s}

Digital inputs / outputs count
96 / 8

Current channels count
32

Current rating / withstand
1 or 5 A / 70 A_s

DAQ Chain

The analog input crate is engineered to collect up to 32 current signals and 32 voltage signals. The installed transducers convert the current inputs to voltage and scale down the voltage input to a suitable level for the ADC. The digital input crate allows optical isolation of the acquisition module. The acquisition unit, located within a dedicated crate, interfaces with the analog and digital input crates, as well as the CERN Technical Network for control and communication.

SOFTWARE ARCHITECTURE

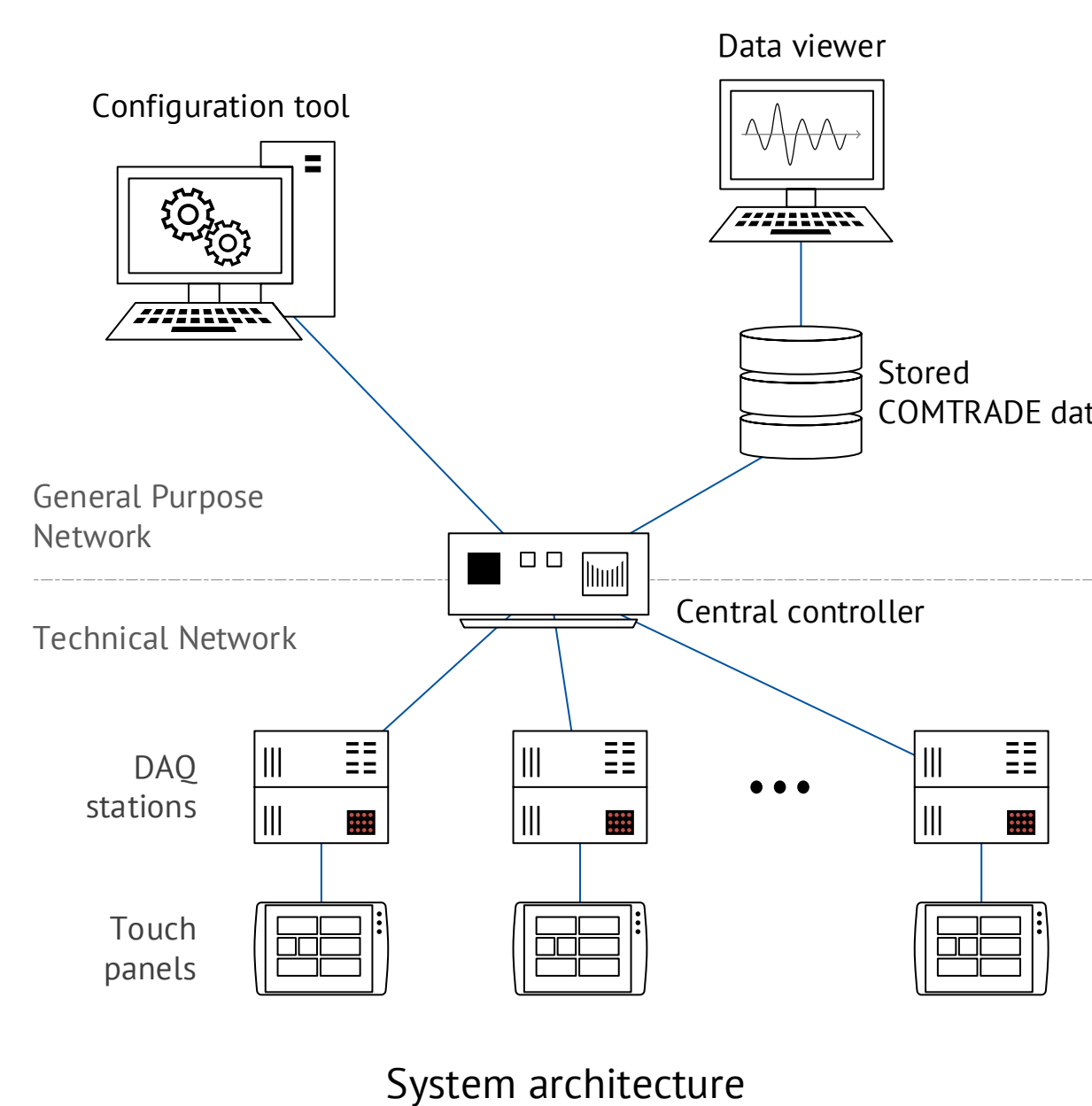
Software Features

Each DAQ station is equipped with an on board processor, allowing for continuous sampling, filtering and data processing, featuring:

- Sampling rate of 7.81 kHz, able to detect spikes and quick events
- Continuous acquisition cycle, with trigger-dependant storage
- Inter-trigger between units over Ethernet
- Configurable recording window of up to 10 s, with settable pre and post triggers
- Real-time FFT analysis
- Remote configuration and programming capabilities
- Export data in COMTRADE format

System Architecture

The CTRS has a distributed architecture, connected on the Technical Network. To access the system from the General Purpose Network, a central controller interfaces with the DAQ.

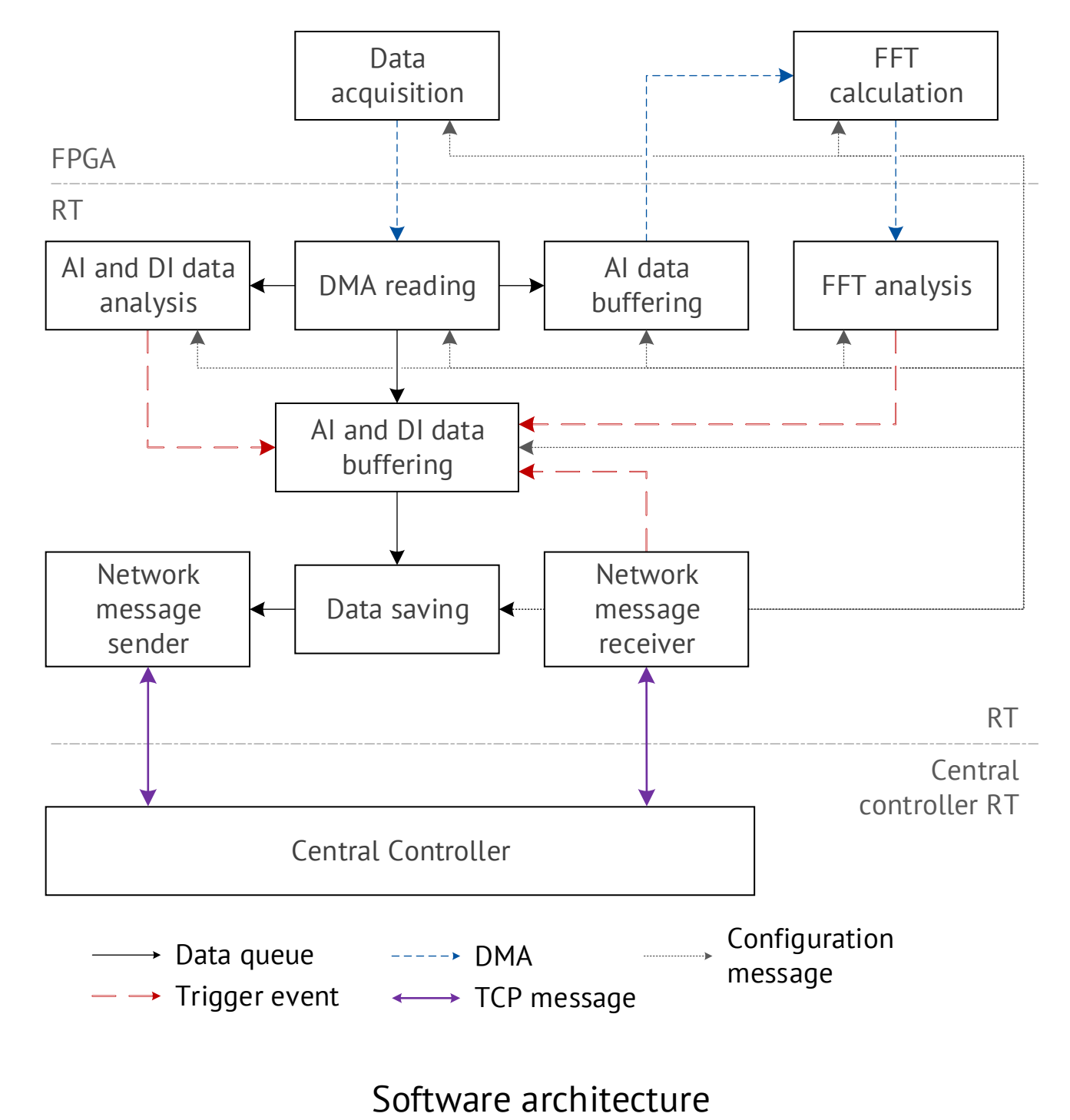


Software Architecture

The FPGA acquires raw data, buffer and transfer it to the RT application. It can control different relay outputs to give information of the cRIO status. The FPGA also performs FFT calculation, taking advantage of its high speed.

The Real Time application analyses the raw signals received from the FPGA, maintains a data buffer in order to save the data in case of trigger and communicates with the central controller. To reduce FPGA memory overhead, the RT application buffers some data before sending it back to the FPGA for FFT calculation.

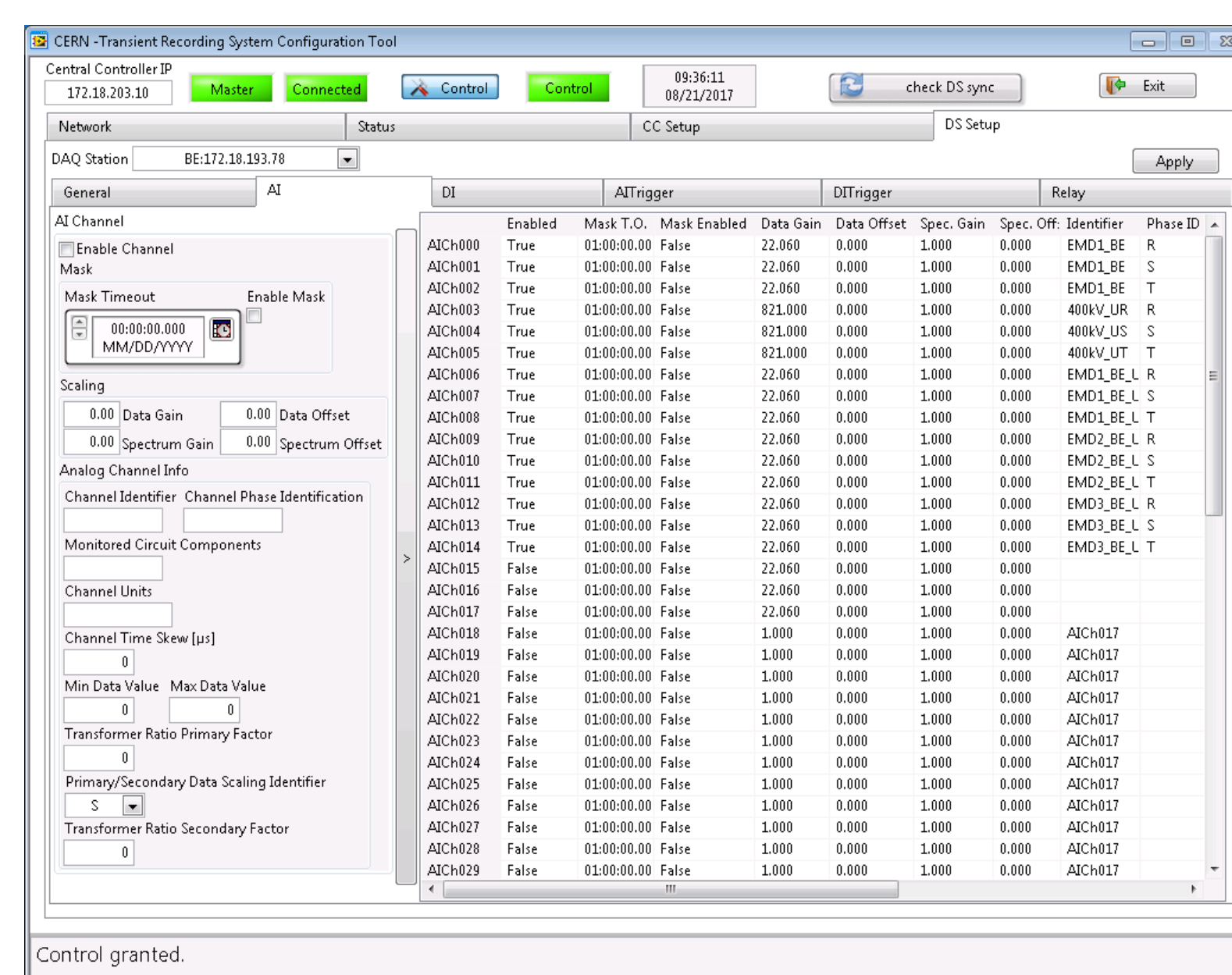
All the DAQ stations can be configured remotely. The system features channel-specific triggering: maximum or minimum instantaneous value, maximum or minimum RMS value in a cycle (50 Hz), over- and under-frequency, harmonics content. Triggering can be propagated over the different DAQ stations.



USER INTERFACE

Configuration tool

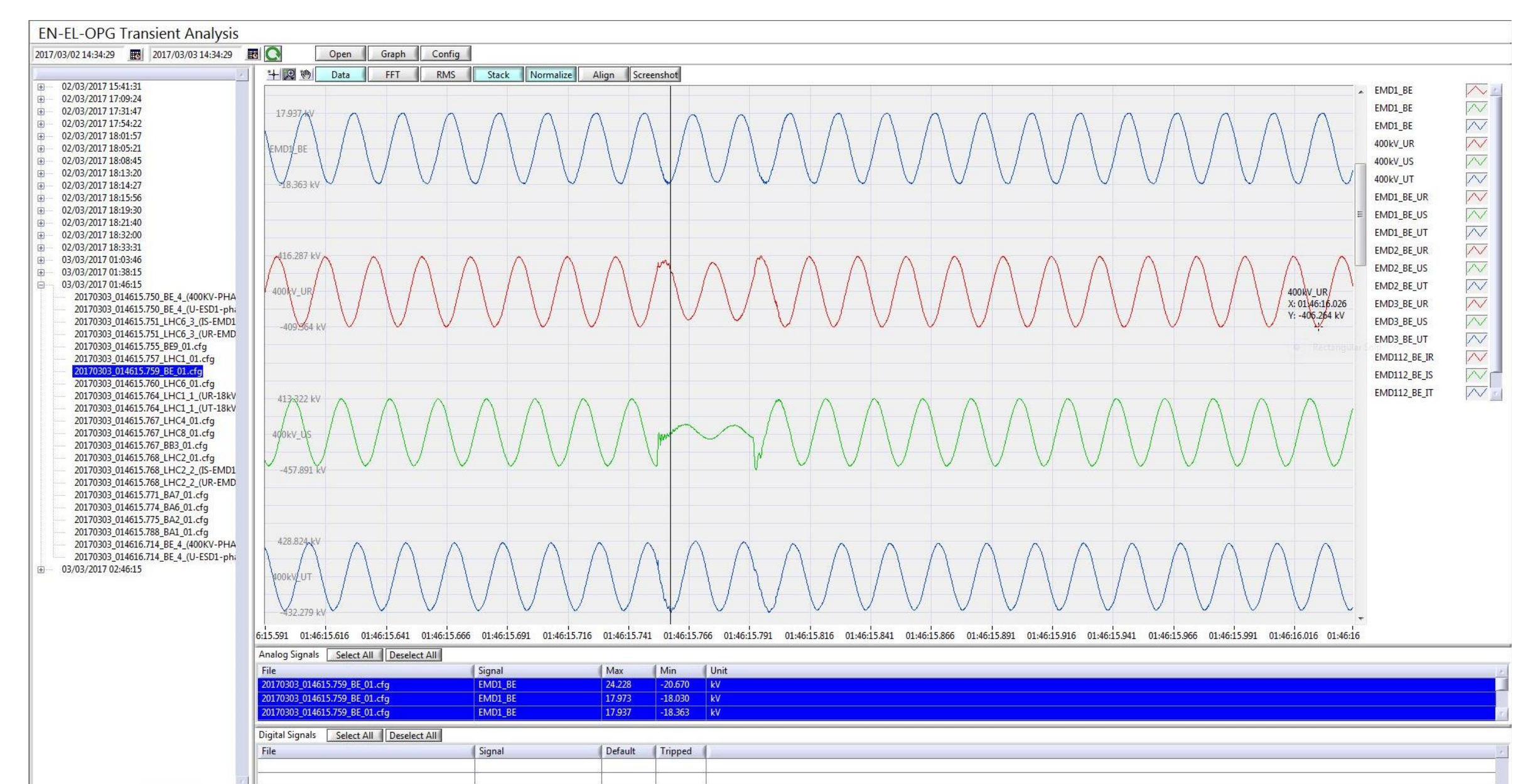
The configuration tool allows setting up each channel of every DAQ station. Setup includes gain, offset, trigger thresholds and trigger types. The configuration tool communicates directly with the central controller, and it can be used to send a general trigger to all the DAQ stations at once.



Configuration tool interface

Transient viewer

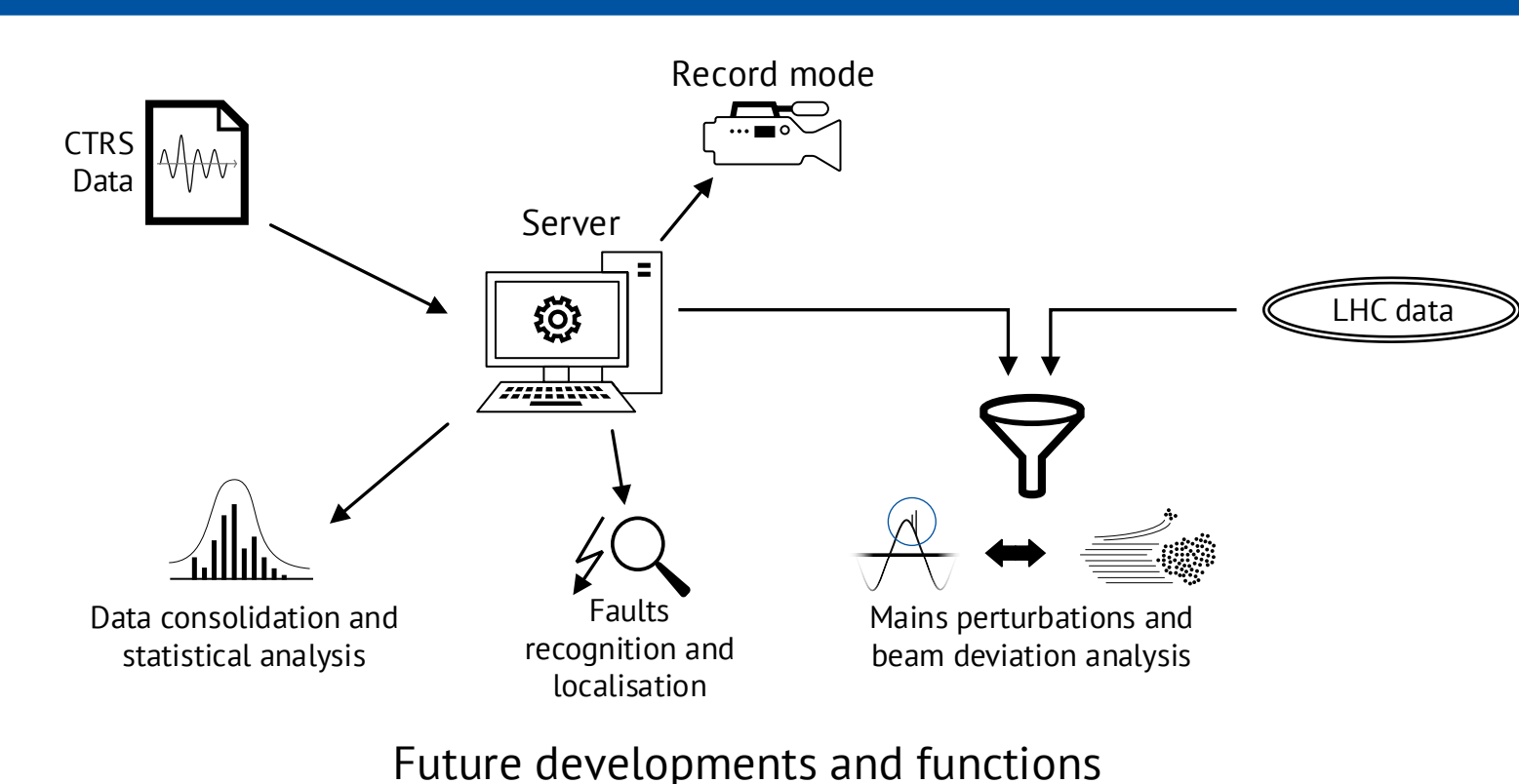
The data viewer is a COMTRADE file reader with searching and filtering capabilities for files on the storage server. Despite the fact that the files recorded by the CTRS can be read by any COMTRADE compatible software, the data viewer is embedded in the electrical SCADA system and it is particularly suited for filtering the many recordings available after an event.



Transient viewer interface – perturbation on the main 400 kV incoming line

FUTURE DEVELOPMENTS

- Improving of the automatic disturbance type recognition for statistical analysis and data consolidation;
- Automatically linking the electrical perturbation on the network to the accelerators' behaviour (RF and magnets) during the run in order to discover and potentially prevent incipient failure modes;
- Improving the data viewer capabilities to allow advanced COMTRADE file analysis, automatic selection of the most relevant recordings after a network fault or disturbance to help the operation teams to better identify the type and the cause of the problem;
- Implementing a continuous acquisition and storage mode with scalable base time, e.g. hourly, daily or weekly.



EN
Engineering Department

ICALEPCS 2017
Barcelona · Spain, October 8-13