Concept of Cavity Simulator for European Spallation Source

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ABSTRACT

At the European Spallation Source it is foreseen to use around 80 superconducting cavities. Each cavity will require an individual LLRF control system, that needs to be tested before the installation inside the accelerator.

Testing of all systems using the real superconducting cavities would be very expensive and in case of a failure can lead to serious damages. To lower the testing cost and avoid potential risks it is planned to design and build a device that simulates the behavior of a superconducting cavity.

The cavity simulator will utilize fast data converters equipped with an RF front-end and a digital signal processing unit based on a high performance FPGA. In this paper conceptual design of hardware and firmware will be presented.

SIMULATED SYSTEM

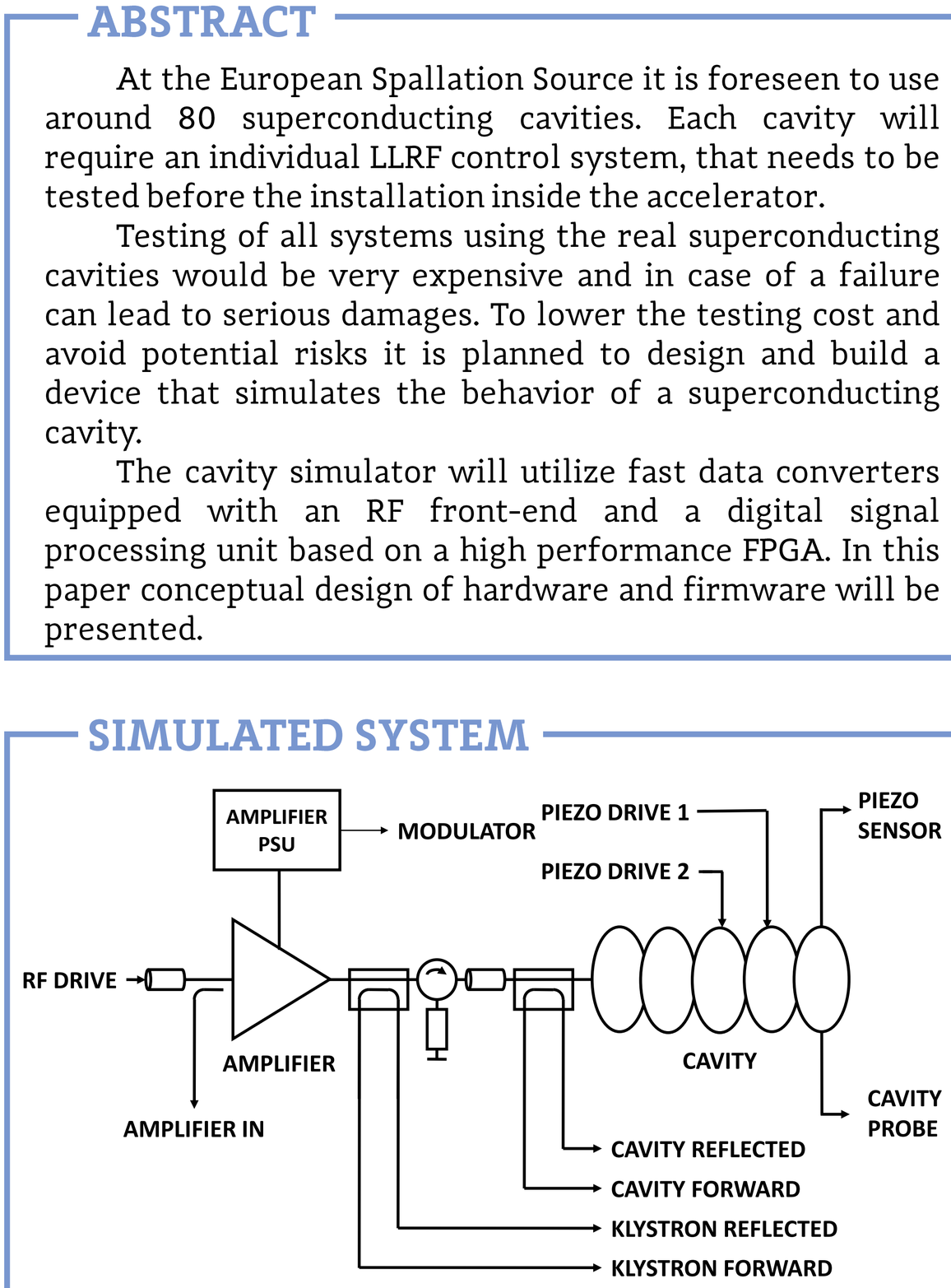

Figure 1: The block diagram of system simulated by the Cavity Simulator.

Among others, the device simulates the following phenomena:

- cavity dynamics,
- cavity detuning,
- beam current,
- piezo compensation,
- lorentz force detuning,
- beam current,
- influence of the amplifiers power supply modulator.

BLOCK DIAGRAM

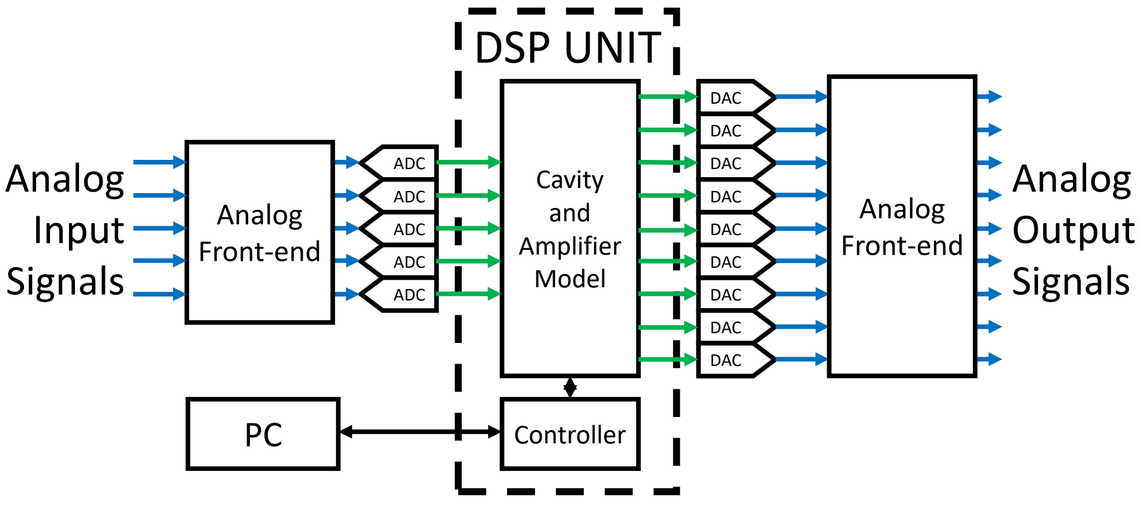

Figure 2: The simplified block diagram of the Cavity Simulator.

HARDWARE

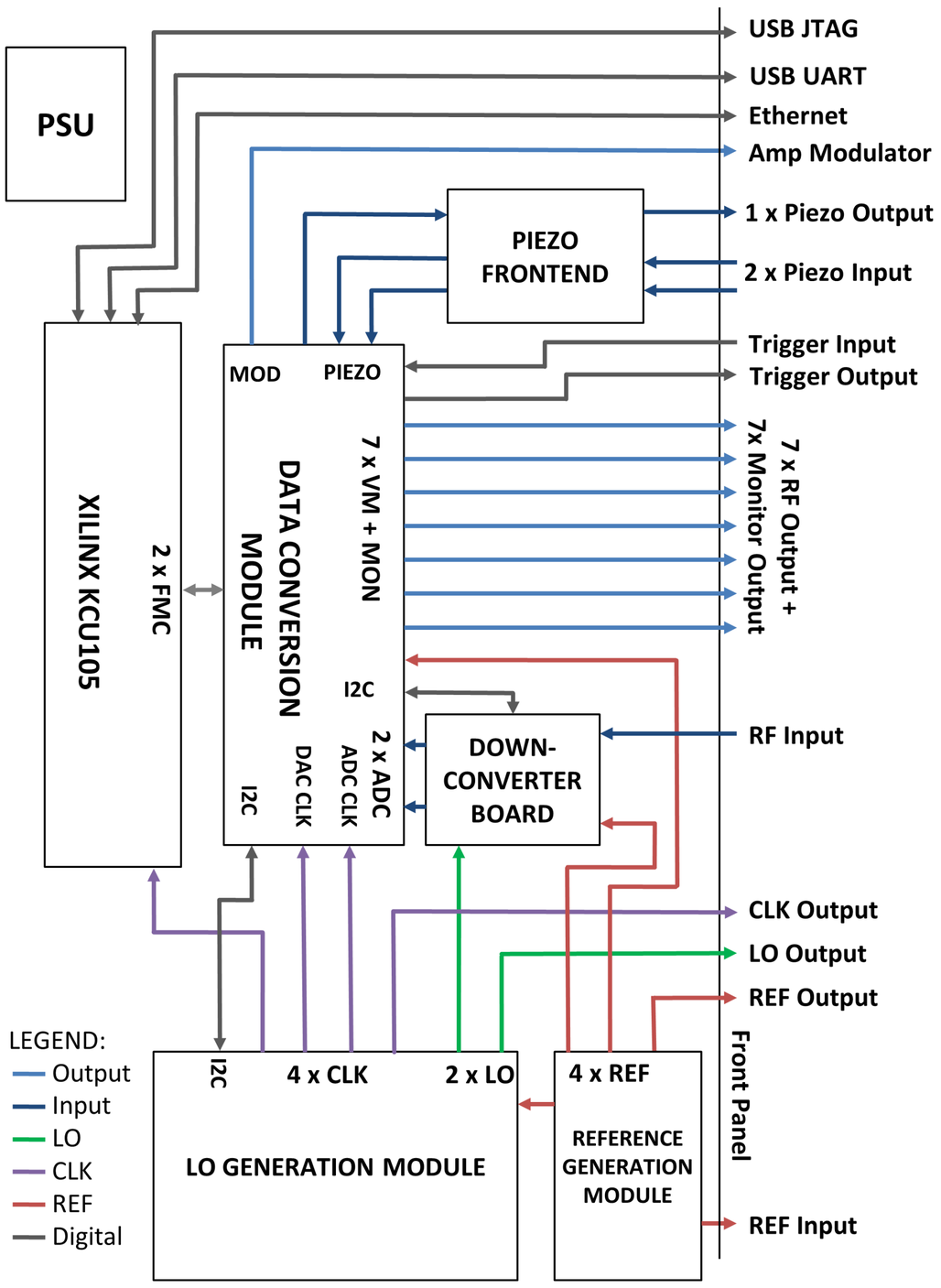

Figure 3: The block diagram of Cavity Simulator Hardware

FIRMWARE

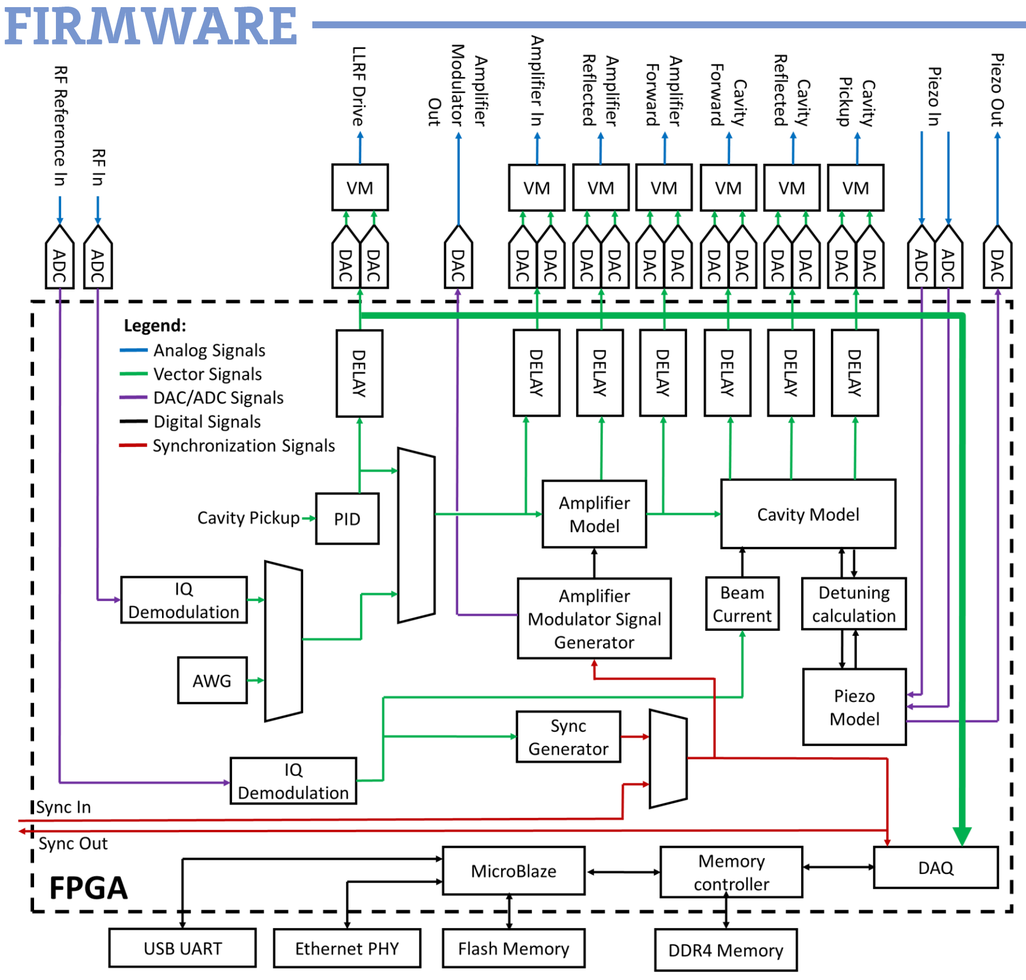

Figure 4: The block diagram of Cavity Simulator Firmware

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