THE INTERLOCK SYSTEM OF FELICHEM

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Abstract

The design of the interlock system of FELiChEM is based on EPICS. The interlock system is made up of the hardware interlock system and the software interlock system. The hardware interlock system is constructed with PROFINET and redundancy technology. The software interlock system is designed with an independent configuration file to improve the flexibility.

HARDWARE INTERLOCK SYSTEM

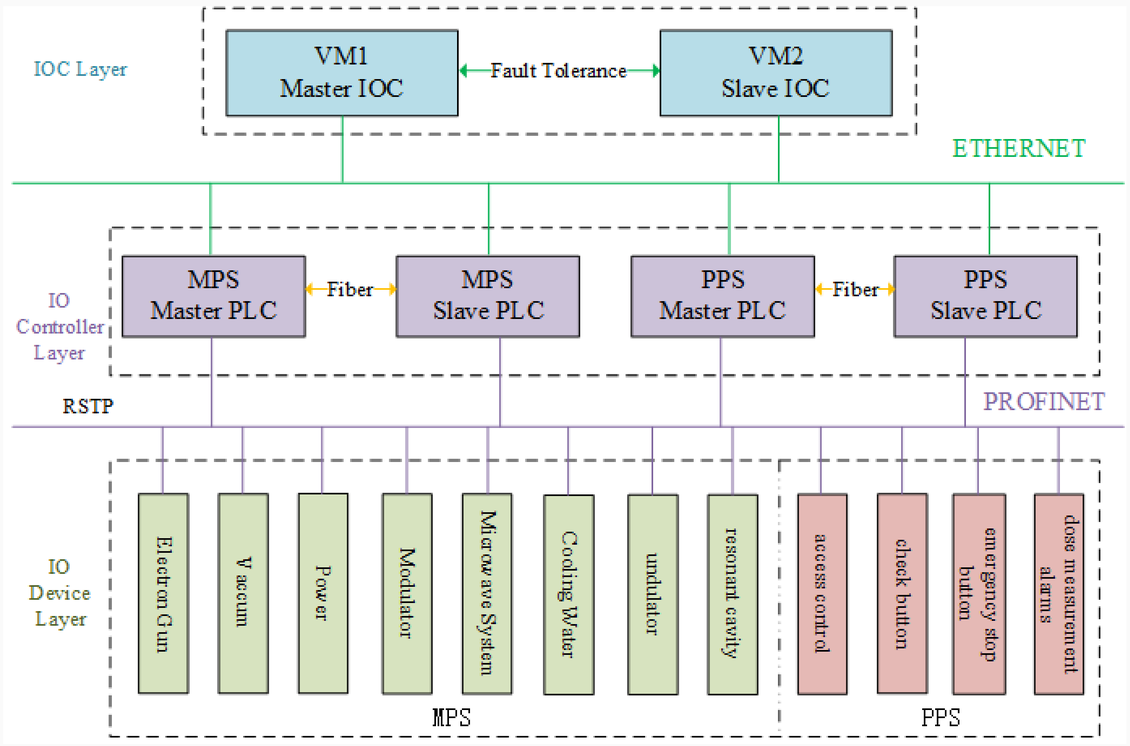

Fig. 1: Architecture of the Hardware Interlock System

HIS has two parts: Machine Protection System (MPS) and Personal Protection System (PPS). MPS has 3 layers: IOC layer, PROFINET IO controller layer and PROFINET IO device layer.

1. *IOC layer:* It has 2 IOCs running on 2 VM for redundancy. By Fault Tolerance (FT) mechanisim, it can achieves zero downtime and zero data loss.
2. *PROFINET IO controller layer:* It has a pair of redundant PLCs. The master PLC and the slave PLC synchronize data via fiber.
3. *PROFINET IO device layer:* It defines MPS and PPS. MPS part has 8 sub-systems and PPS has 4 sub-systems.

TEST OF PROTOTYPE HARDWARE INTERLOCK SYSTEM

Response time and redundant switch-over time are the key parameters in HIS. We establish a prototype system for measuring these parameters.

1. *Test of Response Time:* The test result of oscilloscope is shown in Figure 2. It is about 6ms.
2. *Test of Switch-Over Time:* We use Wireshark to get the switch-over time. The average test result is 6.229ms.

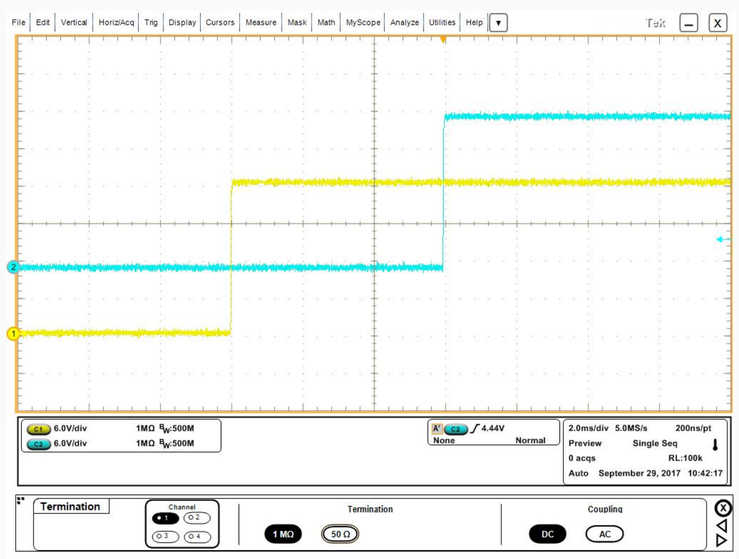

Fig. 2: Test Result of Oscilloscope

SOFTWARE INTERLOCK SYSTEM

SIS is more flexible and configurable than HIS. We use a independent configuration file (JSON) to define the interlock logic.
Fig. 3 is the flow chart of SIS. After program start, it will process interlock logic in monitor list according to the JSON file. If all the process results are true, software interlock system will read action list and process interlock action.

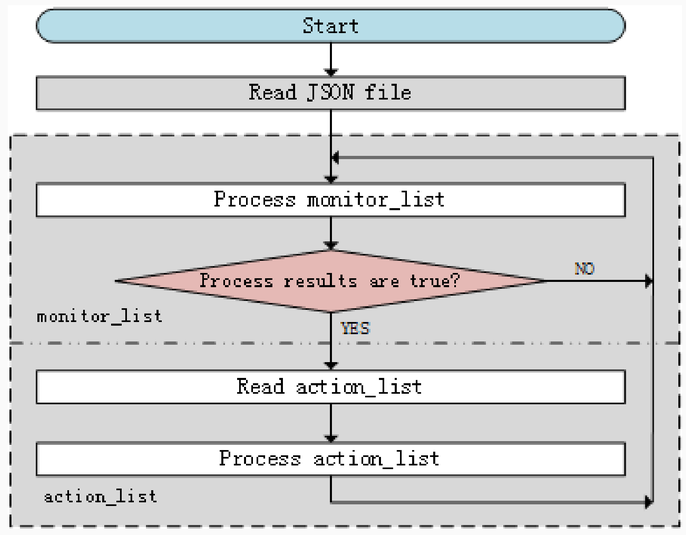

Fig. 3: The logic diagram for SIS Test

And Fig. 4 is a example of JSON file.

```
{
   "interlock_unit":{
      "monitor_list":[
         { "pv_name":"PV_IN_1","compare_operator":">=","design_value":4},
         { "pv_name":"PV_IN_2","compare_operator":"==","design_value":3}
      ],
      "action_list" : [
         { "action" : "set", "pv_name" : "PV_OUT_1","set_point" : 0 },
         { "action" : "delay", "delay_time" : 5},
         { "action" : "set", "pv_name" : "PV_OUT_2", "set_point" : 0.5 }
      ]
   }
}
```

Fig. 4: JSON File of Software Interlock System

TEST OF SOFTWARE INTERLOCK SYSTEM

By the *camonitor* command, we test the response time of SIS. The test result is 434.572ms. Comparing the response time (6ms) of hardware interlock system, software interlock system is obviously slower.

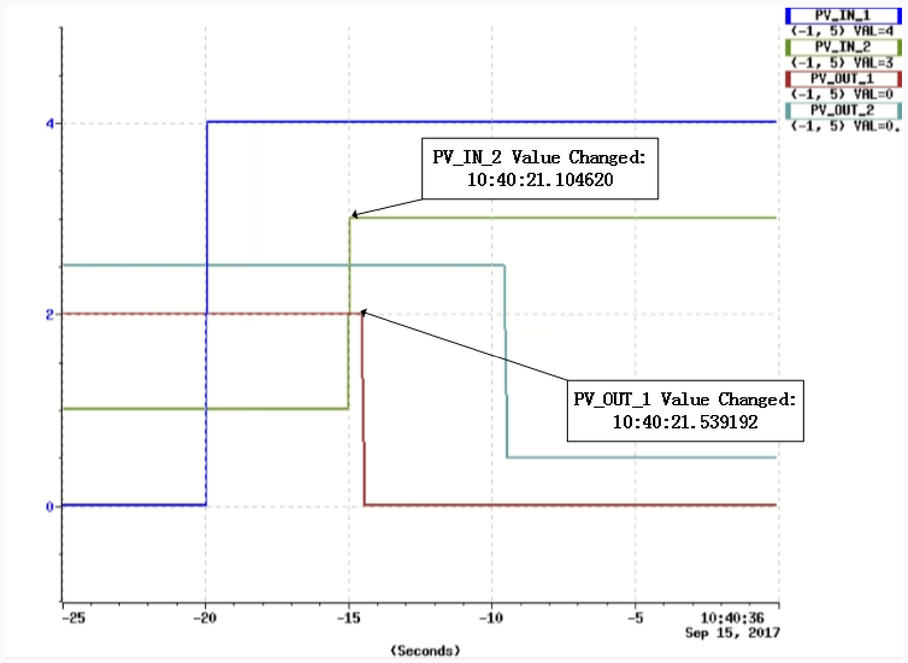

Fig. 5: Execution Result of SIS

Conclusion

1.The hardware interlock system bases on PROFINET and adopts redundancy configuration.
2.Based on the prototype system of HIS, the response time is 5.980ms, the switch-over time of PLC is 6.229ms.
3.We design the software interlock system to increase flexibility which separates interlock program and configuration files.