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THE MACHINE PROTECTION SYSTEM FOR THE INJECTOR II *

Yuhui Guo†, Yi Cheng , Yuting Liu, Shuai Zhan, Haitao Liu, Jing Wang, Hai Zheng, Ting Liu
Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou, China

Abstract

The IMP takes the responsibility for the development of Injector II. The target energy index of it is 25Mev, which is an intense beam proton accelerator with high operation risk. In order to implement cutting the ion source beam in time when the beam position offset happened, the Injector II Machine Protection System is developed based on FPGA controller and PLC. This system aims to prevent device damage from continuous impact of intense beam, as well as obtains and stores status data of key devices when failures occur to implement failure location and analysis. The whole system is now operating stable in field, and the beam cutting time is less than 10μs.

INTRODUCTION

The ADS injector II is a Chinese Academy of Sciences pilot special linear accelerator pre-research device [1] [2]. Its acceleration chamber mainly consists of an RFQ accelerating chamber and four CM superconducting cavities. CM1 and CM2 were installed with six HWR010 cavities respectively, CM3 was installed with five HWR015 cavities, and CM4 was installed with six SPOKE021 cavities provided by the Institute of High Energy Physics Chinese Academy of Sciences. The final beam energy (acceleration value) of the injector II proton linear accelerator is 10-25MeV.

During the design process of machine protection system (MPS) for the injector II, our physicists have defined that the response time of the fast machine protection system (FMPS) must be within 10μs based on the thermal power numerical simulation analysis of the niobium and copper materials and the highest beam power value of the injector II operation. It means that the process from reading fault signal inputs to issuing protection action outputs has to be completed within 10μs. In this case, the possible damage of the accelerated cavity equipment on field could be prevented from strong beam continuous bombardment. Therefore, we decided to build the injector II machine protection system using FPGA technology and PLC system design.

When the acceleration beam position is abnormal or the beam loss of the rear beam line is too large, the FMPS has to cut off the beam quickly and reliably by the ion source equipment, and at the same time, the corresponding power sources, power supplies, vacuum valves and other equipment along the beam line have to be shut down as well to achieve the safety protection of the field equipment.

OVERALL STRUCTURE OF THE SYSTEM DESIGN

The most important feature of the protection system should be fastness. According to the requirements from our physicists, The FMPS design must meet the protection response time within 10μs, which is between the point when the fault signal is received and point the shutdown signal is issued. In order to improve the signal immunity of the whole system, the optical fiber is used for all the signal transmission of the injector II fast protection system. Therefore, the 10μs time also includes the inherent delay time of light transmission in the fiber. In the case of glass fiber, for example, the average refractive index of glass is about 1.5, so the propagation speed of light in glass fiber is approximately

$$v = \frac{c}{n} = \frac{3\times10^8 m/s}{1.5} = 2\times10^8 m/s.$$

It shows that light travels about two hundred meters in 1μs. Since the transmission time of light in optical fiber cannot be avoided, the time left for FMPS to make logical judgments is less than 10μs. Of course, the shorter the judgment time, the better for the system to meet the requirement of the response time.

Because there are many equipment needed to be protected in the injector II and they are scattered, and the field electromagnetic interference is also serious, we adopt the distributed network architecture [3] [4] for the machine protection system. In order to ensure the stability and reliability of the system operation, we use the MIS system, developed by Shanghai Institute of Applied Physics, as the main control system, which is responsible for the collection of key equipment status, logical judgment and the output of the beam cut-off action. The front-end FPGA controller is designed by ourselves and is responsible for the collection and preprocessing for the equipment's fault signals. The photoelectric conversion module is located at the low level of the device, which make the fault state of the device to split into two parts, one for cutting off the beam and the other for the PLC interlocking system. Thus, the redundancy of the control link can be achieved and the reliable operation of the whole system can be ensured. The whole structure of the protection system is shown as Fig. 1.

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†guoyuhui@impcas.ac.cn

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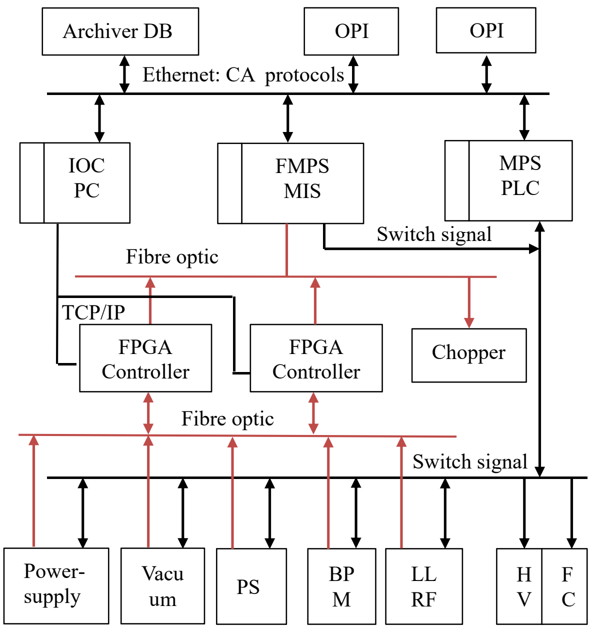

Figure 1: Injector II MPS system structure diagram.

As shown in Fig. 1, the main control system based on MIS collects the fault information and process them according to the control rules, and determine if it is necessary to issue protective signals. Because a complete beam cut-off requires the simultaneous operation of the MIS and PLC systems, so the fault signals need to be sent to both the MIS and PLC systems simultaneously[5][6]. In the process of the beam cut-off control, the MIS transmits a protect instruction to the chopper of the ion source. However, the Chopper power supply has a high voltage of 60 seconds duration, and after the 60 seconds the beam cut-off protection must be completed by other devices controlled by the PLC system. For example, the high-voltage power supply being set to zero, the Faraday tube is needed to be inserted to block the beam and the other power supply devices have to be turn off to complete a full beam cut-off process.

As there are many devices, and one MIS chassis can only receive 48 optical signals. So In the process of system design, multiple front-end FPGA controllers are used to perform initial processing for the fault signals, composing them into one input signal to the MIS main system. At the same time, the processed data from front-end FPGA controllers are uploaded to the central control room via Ethernet to be displayed and saved in the archiver database. The photoelectric module is used to convert the digital signals of superconducting cavity magnet, power supply, cryogenic system and vacuum equipment into standard optical signals, so that a unified signal interface has been established and is helpful for system maintenance and future upgrades.

KEY HARDWARE CIRCUIT MODULE

The Machine Interlock System (MIS) is a set of interlocking protection systems jointly developed by the Shanghai Institute of Applied Physics of Chinese Academy of Sciences and the Cosylab Corporation. The purpose of MIS is to provide a secure, reliable and fast response interlock protection system for the accelerator [7]. The system adopts 3U CPCI mechanical standard and customized backplane bus. The hardware includes MIS case, monitoring module, interlocking module, input module and output module. The MIS system is characterized by double redundancy for master controller and power, fast response time (µs). In the MIS for the injector is mainly used to achieve the judgment and execution of the high level control logic. The fault signal acquisition and preprocessing of the low level equipment are realized by the front-end FPGA controller, photoelectric conversion module and relay module.

Front-end FPGA Controller

The functions of the front end of the FPGA controller are: receiving and sending fault signal via the optical fiber; composing multi-channel fault signals into one fault signal output; uploading and archiving multiple fault signals through the network, in which the upload time interval is 500ms. So the front-end FPGA controller is designed to have required functional modules, such as: fiber optic transceiver, Ethernet interface and digital IO interface. The optical fiber transceiver is used to communicate with the MIS master system; the digital IO interface is used to receive the state data from device(s) via the photoelectric conversion module; the Ethernet interface is used to communicate between the operation computer and the controller. The front-end FPGA controller is shown in Fig. 2.

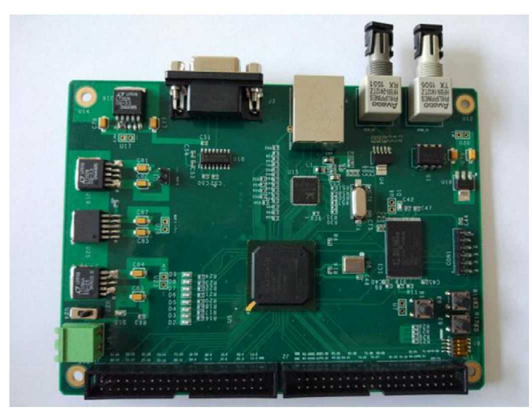

Figure 2: Front-end FPGA control board.

Photoelectric Conversion Module

The photoelectric conversion module on the device side is mainly used to interconnect the signal between the low level equipment and the front-end FPGA controller. The signal received from field devices of the injector II is mostly a TTL signal or switch signal. A few devices can directly send optical signals. Therefore, the

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photoelectric conversion module needs to have IO features such as:

- Input interfaces to receive TTL signals or switch signals;
- One optical signal output interface to send a signal (to FMPS);
- One switch signal output interface to send a signal (to PLC).

The photo of the photoelectric signal conversion module is shown in Fig. 3.

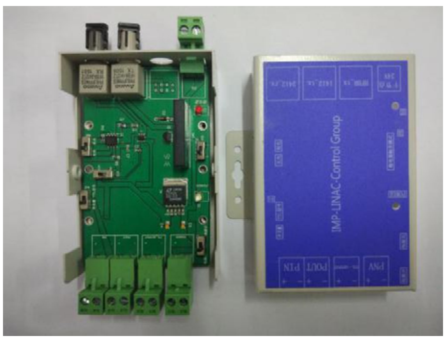

Figure 3: Photoelectric conversion module.

Relay Module

In the devices field of the injector II, all the fault signals need to be sent to both the FMPS and PLC interlocking systems simultaneously. The FMPS can deal with optical signal directly but the PLC interlock protection system only receives the switching signal. So it is necessary to design a relay module to convert the optical signal to the switching signal. We have made some configuration changes on the circuit of the photoelectric conversion module to achieve the above function. The photo of the Relay module is shown in Fig. 4.

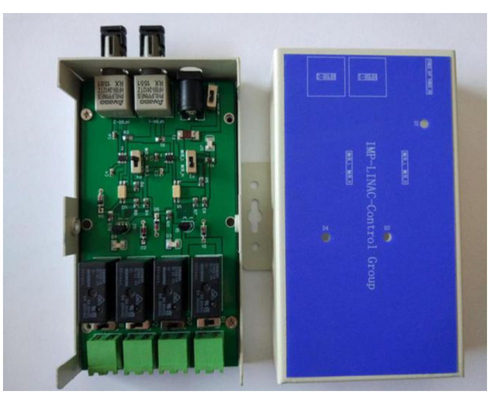

Figure 4: Relay module.

SOFTWARE PROGRAMMING

In order to fully protect the equipment, quickly find fault locations and reduce troubleshooting time, a protection software system need to be established. The system provides the fault signal acquisition, protection output, fault logging and other functions. According to the field requirements, the software system provides the following functions:

Input Signal Filter and Adjustable Filtering Time

The reason for signal filtering is: the field environment is complex, and the system will has some unavoidable noise interferences. Therefore, the pulse width of the fault signal has to be limited in the FPGA program, for example, signal smaller than 1μs to be filtered. The specific filtering time can be changed by the command through network communication.

Latch the Fault Input Signal

In order to have a reliable acquisition and recording for fault data, as long as the fault signal is detected, regardless whether the signal is automatically returned to normal, the system will hold the fault signal for 2s, after 2s the signal can be reset automatically (by system) or manually. Thus, the front end FPGA controller has enough time to output the protection action and upload the fault signal. The signal data upload time is about 500ms.

Protection Bypass Function

Each fault signal can be bypassed individually. Sometimes the devices are in the faulty status. It is necessary to shield them off so the testing and debugging of other equipment/system will be not affected. To provide more flexibility for system test, the bypass value can be modified manually as well.

The above features can be achieved using CSS software. In the total control commissioning interface, the MIS system supports 8 protection modes. It is very convenient to switch the mode automatically for machine protection systems in different debugging requirements and in beam experiment. The corresponding PLC interlock protection system can also provide fast switching functions between varieties of control modes through the PLC multitasking switching mechanism. The PLC system is built with PHOENIX CONTACT ILC 171 to achieve the corresponding protection action output by using its DI and DO modules.

The MPS fault data query GUI interface is shown in Fig. 5. According to the selected time interval the database is retrieved. The search results will be displayed in the form of a table, each row represents a fault occurred. The fast protection control GUI interface records the details of the time when the fault occurred with 1μs precision. Fig. 6 shows the curve of the device fault information. The left side list is the name of the physical device represented by the display curve. By checking the corresponding selection box, the fault history data of the specific device can be displayed.

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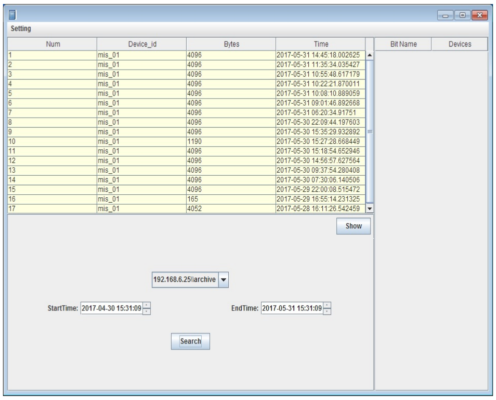

Figure 5: Fault data query GUI.

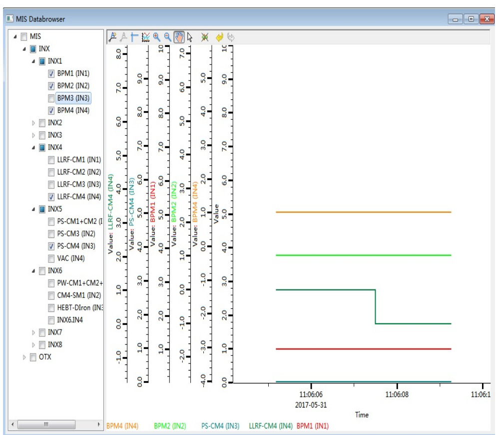

Figure 6: Fault data display GUI.

SYSTEM TEST

The test of the machine protection system mainly includes the system fault signal filter test and system response time test. In the course of the test, we set the signal to filter the pulse width of 2μs. Then we generate 1μs and 2.5μs square wave fault test signal using a signal generator respectively as input to the protection system. The signals can be observed by oscilloscope. The test results are shown in Fig. 7.

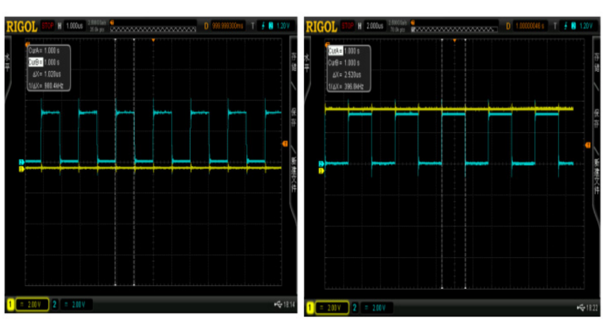

Figure 7: Test results shown on oscilloscope.

The test results show that when the pulse width of the input square wave signal is 1μs, the system determines that it is an ineffective signal as less than 2μs system setting, and the fault signal is filtered automatically, The output is still in the normal state (low level); when the square wave signal pulse width is 2.5μs, exceeded 2μs set value, the system determines the input fault signal is valid and outputs protection response signal (high level).

Through the above signal test, it was demonstrated that we had achieved the desired design goal of filtering function for the front-end FPGA controller. In addition, we tested the response time of the fast protection subsystem in the MPS system. The test waveform is shown in Fig. 8.

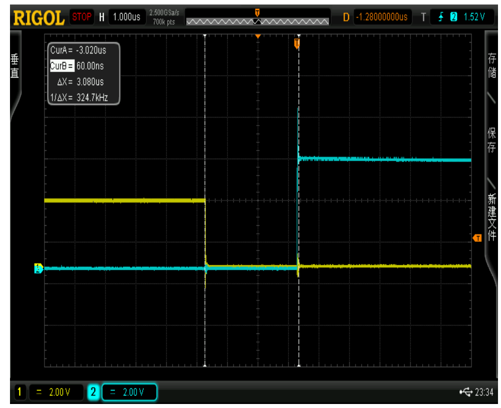

Figure 8: Fast chain protection system response time.

In the process of system testing, the front-end FPGA controller receives a valid fault signal of the equipment and then after the filtering process, sends the signal to the MIS master control system. Then MIS master control system does its logic process and issues a protection signal to cut-off the beam. The total time taken from the valid fault signal input to the system to issue the cut-off protection signal is 3.08μs. The response time from test system result fully meets the design requirements of 10μs. Note: in the test system, 3 meter optical fiber and 1 meter cable is used for the fault related input and output.

CONCLUSION

This paper has reported that a machine protection system was developed and used for the injector II use in the Chinese ADS facility. The accelerator can operate in two beam commission modes (pulsed and continuous). In the continuous beam operation mode, the control system [8] needs to provide fast machine protection. Especially in commissioning 25Mev beam energy, a FMPS is really needed to provide a μs-level fast beam cut-off protection. The injector II machine protection system is based on the FPGA control board and the PLC device, and can achieve the system response time at a μs-level from the FPGA controller and ms-level from PLC system for the control protection respectively. In May 2017, the 25MeV superconducting linear accelerator completed the construction and started pulse commissioning. The 26Mev pulsed beam commissioning was successful on June 5th, 2017 and on next day - June 6th, 2017, 25MeV continuous beam commissioning was successful as well. During the above beam commissioning process, the MPS system has been demonstrate to be stable and reliable.

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