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FPGA-BASED PULSED-RF PHASE AND AMPLITUDE DETECTOR AT SLRI

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Abstract

In this paper, the prototype of phase and amplitude detector for pulsed-RF measurement is described. The hardware is designed in VHDL and implemented using Field Programmable Gate Array (FPGA) for digital processing. The main phase and amplitude detection algorithm is implemented using state machine in the MicroBlaze soft processor. The detector system is designed to measure the phase and amplitude of a 5-microsecond wide 2,856 MHz pulsed-RF at a repetition rate of 0.5 Hz. The front-end hardware for the pulsed-RF signal acquisition is also described with the interface to the FPGA-based controller part. Initial test results of the prototype are presented.

INTRODUCTION

Synchrotron Light Research Institute (SLRI) is a dedicated synchrotron radiation facility in Nakhon Ratchasima, Thailand. Its 40-MeV linac has been operated since the first light in December 2001. The SLRI's linac is a 40 MeV electron linear accelerator consisting of five different parts to accelerate the electron beam. These parts are pre-buncher 1, pre-buncher 2, buncher, a 20-MeV accelerating tube 1, and 20-MeV accelerating tube 2. They are fed with a pulsed RF signal operating at 2,856 MHz as the accelerating field from a klystron. Currently, the phase and amplitude of the RF signal in the waveguide can be adjusted manually by the high power phase shifters and attenuators. With an increasing demand of higher electron beam quality, an improvement in phase and amplitude of the RF signal is necessary. The measurement system of the RF phase and amplitude in each part of the linac is needed for stability improvement.

In this paper, the prototype of phase and amplitude detector is described. The system is designed to measure the phase and amplitude of a 5-µsec wide pulsed RF signal at a repetition rate of 0.5 Hz. RF front-end hardware and FPGA-based detector system are presented in the next section. An algorithm implemented in the software part is described in the following section. System performance and conclusion are presented at the end of this paper.

HARDWARE

In order to measure the phase and amplitude of the pulsed RF signal correctly, both hardware and software of the detector system must be designed carefully. This section describes various hardware parts used in the design and implementation of the prototype. The RF front-end hardware is explained. A main processing system hardware based on FPGA is described and the system integration is also discussed.

RF Front-End Hardware

Each set of the RF front-end circuit is designed to measure the amplitude and phase of a 5-µsec pulsed RF from the klystron to the linac. Six RF front-end sets are needed to be installed in the linac system to perform the measurement at the five parts, as discussed in the introduction part, plus one location just after the klystron.

The amplitude measurement uses RF diode as a linear detector. The phase detection is designed to measure the phase differences between the pulsed RF and a cw RF reference line of the linac. Both of these signals have the same frequency. In the phase measurement, a double balanced mixer (DBM) is used as a phase detector. The detail of this function of the DBM can be found in [1]. A voltage-controlled phase shifter is used as a nulling detector. Other RF components comprise splitter, low-pass filters, and band-pass filters. The principle of the phase measurement technique can be referred to [2] and examples of the complete measurement system can be found in [3] and [4].

In this prototype development, the selected RF diode detector is an 8473B model with positive output from Agilent Technologies, the RF circuit components are selected from Mini-Circuits, and the voltage-controlled phase shifter is chosen from Lorch Microwave. Six of these front-end sets are tested in the laboratory with Agilent Technologies' RF Vector Signal Generator (VSG) model EXG N5172B. In addition, a narrow-pulse modulation capability is available on the VSG in order to generate the pulse modulated RF signal. For future installation in the linac cabinet system, two sets of the phase and amplitude detector are put in the chassis similar to the ones described in [4]. This makes the total of three RF chassis ready for cabinet installation. The RF circuit test set up is shown in Figure 1. Typical phase shift characteristics of voltage-controlled phase shifters is shown in Figure 2. The complete RF chassis is shown in Figure 3.

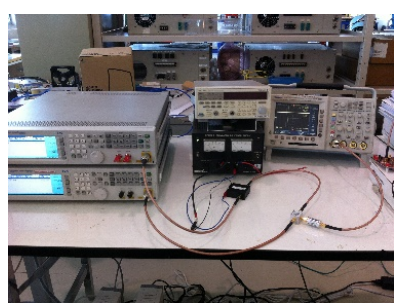

Figure 1: Laboratory test set up for RF circuit.

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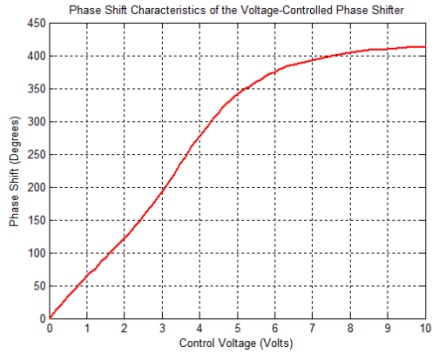

Figure 2: Typical phase shift characteristics of voltage-controlled phase shifter.

Figure 3: RF chassis of the phase and amplitude detector.

FPGA-Based Detector System

In this prototype development, FPGA evaluation board is our choice for fast digital system implementation. Xilinx's ML605 Evaluation Kit [5] featuring a Virtex-6 XC6VLX240T FPGA is chosen to be a main controller of the design. It has two FMC connectors available for connecting daughter peripheral cards.

In order to sample multiple amplitude and phase signals from the RF chassis, a multi-channel ADC is needed. For the choice of a multi-channel bipolar simultaneous sampling ADC evaluation board, the Analog Devices' EVAL-AD7656-1SDZ [6] featuring AD7656-1 ADC and its FMC adapter board are selected. The ADC has 6 channels with a resolution of 16 bits each.

To control the electronic phase shifters, a multi-channel DAC is required. Maxim Integrated's MAXSPCSPARTAN6+ board [7] is chosen. It features a MAX5135 4-channel 12-bit DAC with SPI interface and available FMC connector. Figure 4 shows how all the boards are connected as an FPGA-based detector system.

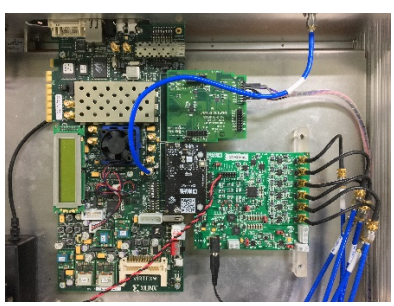

Figure 4: Virtex-6 ML605 FPGA board with AD7656-1 and MAXSPCSPARTAN6+ daughter boards.

In the Xilinx FPGA, MicroBlaze processor is implemented as a main controller. Xilinx's ISE 14.7 and the Embedded Development Kit (EDK) are the IDEs selected to develop this embedded processing system. One custom IP block is designed using VHDL [8] to interface with the ADC. The ADC driver IP is generated with a finite state machine (FSM) for proper operation. It is designed so that all interface signals meet technical timing requirements. In addition, since the valid data is available during the narrow pulse, a trigger input is implemented as a gate to enable the data sampling instance for the ADC. In the real application, the trigger signal is available from the timing system of the linac [9]. To select which ADC channel to sample data, two AXI GPIO IPs are used to connect the ADC driver IP. The final design of the ADC driver IP and its interface in EDK are shown in Figure 5 and Figure 6, respectively.

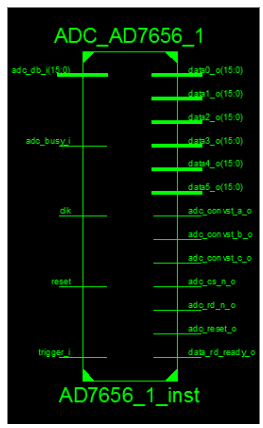

Figure 5: AD7656-1 driver IP with trigger input.

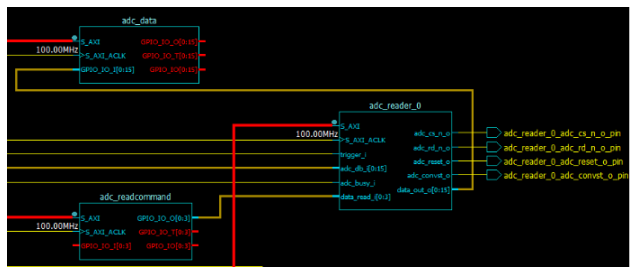

Figure 6: AD7656-1 Interface IP in EDK.

The MAX5135 DAC interface is a simple SPI standard. Figure 7 shows the digital logic block of the DAC. The MAX5135 block in EDK is implemented using AXI SPI interface as shown in Figure 8.

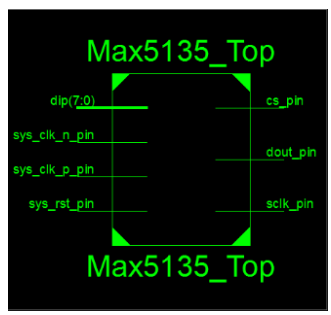

Figure 7: Max5135 logic block.

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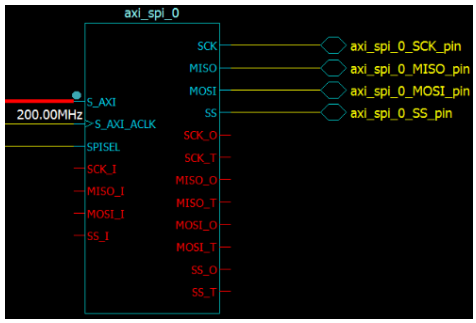

Figure 8: AXI SPI interface to MAX5135 DAC in EDK.

System Integration

From the hardware connection shown in Figure 4, the main ML605 controller board can process up to 6 analog input signals. Thus, 2 sets of this controller are required to build a complete system.

Table 1: Analog Signal Assignment for ADC

ADC Channel	Analog Signal
CH1	Phase # 1
CH2	Phase # 2
CH3	Phase # 3
CH4	Amplitude # 1
CH5	Amplitude # 2
CH6	Amplitude # 3

The system interconnection and signal interface is shown in Figure 9. This block diagram is drawn for one set of the boards. Six analog signals are assigned to the ADC board. Each channel samples the signal listed in Table 1. ADC Data Conversion and DAC Code Determination blocks are performed in the MicroBlaze processor. These two blocks are used to manage and control the signals and data flow between the FPGA logic and the main phase and amplitude calculation algorithm. In the FPGA logic part, AD7656-1 Interface and AXI SPI IPs are implemented to connect to the ADC and DAC, respectively, via FMC connectors. The timing signal that is used as a trigger input to determine the time instance to sample the data is the external trigger signal. In addition, two AXI GPIO IPs are used to connect to the AD7656-1 Interface IP, one is used to select the ADC channel and the other is used to receive the 16-bit ADC data.

SOFTWARE

The main phase and amplitude calculation algorithm is designed in the software part, written in C program, and run by the MicroBlaze processor. The operations of data conversion, DAC output generation, filtering, averaging, system control and hardware interface are performed here. The amplitude calculation of each RF signal is obtained by simply multiplying by the attenuation of each RF cable and RF circuit components in the line. The phase calculation algorithm is of our particular interest.

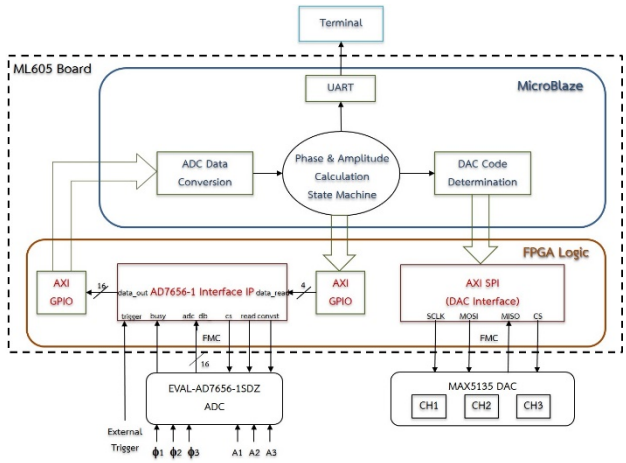

Figure 9: System block diagram for one ML605 board.

For all RF front-end phase detector circuits, each of which includes a power splitter, a band-pass filter, a low-pass filter, and a DBM, their DC output at the DBM has been recorded during the laboratory test. Each of them has its output characteristics similar to the one shown in Figure 10. The DC output has a form of a pseudo cosine function. This suggests that there are two possible values of phase difference for each value of the DBM output. This is also possible since the selected phase shifter covers 360 degrees. The phase detector output and the phase shift characteristics (as shown in Fig. 2) of each RF front-end circuit are stored in the C program for phase calculation.

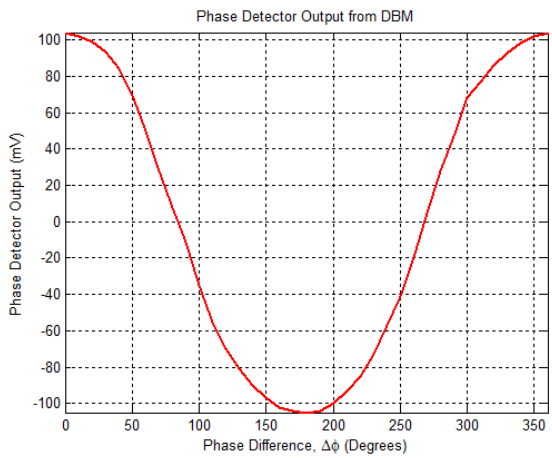

Figure 10: Phase detector output of the DBM.

The phase calculation algorithm is implemented similar to that described in [2]. The main part of the algorithm is to find the correct zero crossing point of the DBM output and the slope in its vicinity once the DAC is controlled to output the selected DC voltage. The detail of the implemented algorithm can be further explained in a state machine diagram in Figure 11. The short description of each state is summarized in Table 2. The phase and amplitude values are displayed on the PC via UART. In addition,

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important information and calculated values are sent via UART for state tracking and evaluation.

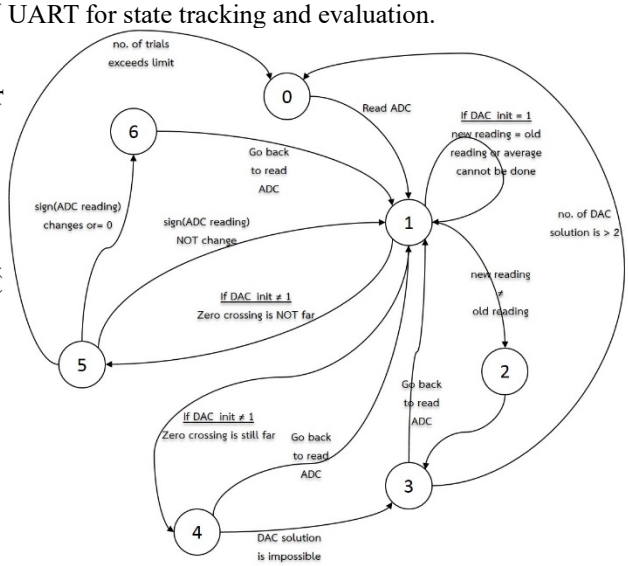

Figure 11: State machine diagram for phase calculation.

Table 2: Short Description of each State in the State Machine

State	Description
0	Initial state, set DAC output to 0 volt.
1	Read ADC data.
2	Find 2 DAC solutions from phase shift characteristics and compare to the ADC data.
3	Set DAC to output the DC voltage (0-10 V) to each solution. Then, verify the result from reading ADC data again.
4	Check if the DAC output is indeed the true phase solution (near the zero crossing point).
5	Search for the zero crossing point.
6	Determine the phase solution by interpolation, if necessary.

SYSTEM PERFORMANCE

In the hardware test, the interface between the ADC and FPGA is very important. It was first tested in order to achieve correct data and timing requirements. Figure 12 shows the ADC interface signals and data bus captured by Xilinx's Chipscope Pro software. The signals shown are chip select (cs), read (rd), and conversion start (convst). The result shows that the system meets timing requirement and provides correct data for all six ADC channels.

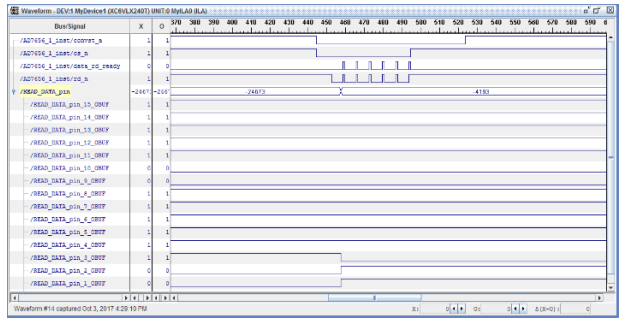

Figure 12: Interface signals and data bus between FPGA and ADC.

In the software test, the main C program was carefully tested in each state of the state machine. A number of conditions and loops were implemented. For each triggering instance from the timing signal (0.5 Hz), the algorithm can manage to make one transition from one state to the next but all six channels can be processed simultaneously. After initial state is executed and state 1 is being processed, the sampled data from each channel needs to be averaged and small delay has to be introduced. This is important so that we can obtain appropriate response from DBM output. This procedure is also performed when reset occurs (from state 5 to state 0) once the phase is out of track. The result shows that, from starting at state 0, the algorithm needs at least 12 pulses to successfully calculate the phase. In the C program, the chosen step of the DAC output constant for setting the DC voltage is 8 times the DAC unit $\left(8 \times \frac{360^\circ}{2^{12}}\right)$, which contributes to a measurement resolution of $\pm 0.70^\circ$. With the zero crossing search algorithm, the error becomes slightly less by using interpolation. The phase calculation algorithm can perform satisfactorily in the laboratory conditions.

CONCLUSION

The prototype of phase and amplitude detector is developed for pulsed RF measurement. The system is designed to measure the phase and amplitude of a 5-µsec wide pulsed RF signal at a repetition rate of 0.5 Hz. The RF front-end circuits have been designed and tested in the laboratory. FPGA evaluation board is selected as a main controller. ADC and DAC evaluation boards have been selected as daughter boards to reduce development time. A number of tests have been conducted to successfully achieve the desired result. The digital logic blocks and custom IP generated using VHDL enable concurrent operation and interface with a multi-channel simultaneous-sampling ADC and DAC. In the software part, the main phase and amplitude calculation algorithm is implemented in the MicroBlaze processor. In laboratory tests, the calculated phase and amplitude are displayed on UART terminal with small calculation errors. The overall performance of the detector, both hardware design and software implementation, is satisfactory.

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