BOOSTER RF UPGRADE FOR SPEAR3*

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Abstract

SLAC's Stanford Positron Electron Asymmetric Ring (SPEAR3) Booster Radio Frequency (RF) system was recently upgraded where the existing klystron providing RF power to a 5-cell cavity was replaced with a Solid State Amplifier (SSA) [1]. The Low Level Radio Frequency (LLRF) Controls to drive the SSA was provided by a high performance Field-Programmable Gate Array (FPGA) based system built on SLAC's Advanced Telecommunications Computing Architecture (ATCA) modules. RF Cavity Tuner Controls were replaced with EtherCAT-based stepper motor controller. New hardware was designed and built for programmable logic controller *(*PLC*)* based Machine Protection System (MPS). Fast digitizers to sample and acquire LLRF signals were implemented in a LinuxRT Server. All of these required new controls software implementation. This paper describes the controls associated with each of the above hardware upgrades.

BOOSTER RF UPGRADE CONTROLS SYSTEM

The controls layout of the upgraded Booster RF system is shown in Figure 3. The main components are the Experimental Physics and Industrial Control System (EPICS) Input/Output Controller (IOC) controls for the SSA, ATCA, PLC MPS, Booster RF Cavity Tuner and the PCIe Digitizer. Each of these is described below.

EPICS IOCS

The software controls for all the new hardware described above are via EPICS Soft IOCs running either on a Linux or LinuxRT (Real Time Linux) Server. All IOCs provide the following generic functions:

- Alarm setup capabilities and alarm handling notifications.
- EPICS Process Variable (PV) archival for History plots.
- Save/restore values on IOC boot up.
- Monitoring of processor load, memory usage and IOC heartbeats.
- Extensible Display Manager (EDM) display panels for operator control.
- Message logging.

In addition, each IOC provides functions specific to the hardware to which it interfaces.

SSA CONTROLS

The EPICS Soft IOC for SSA controls provides the following functions:

- Control of the SSA over the EPICS Channel Access (CA) network. This includes SSA ON/OFF, set operating mode to either Continuous Wave (CW) or Pulse mode, RF Operate or Standby mode, set DC Power Supply output voltage levels, enable/disable individual power supplies.
- 10 Hz Digital and Analog status updates of the SSA.
- SSA Internal and External Fault detection and Fault Reset capabilities.
- Read SSA Error Codes and provide appropriate alarms.

SSA IOC

The IOC interfaces with the SSA via the MODBUS protocol based network device. MODBUS is an application layer Messaging protocol in OSI model based on Client-Server communication. The Server in SSA's Main Controller Unit (MCU) supports MODBUS communications via on-board embedded Ethernet network device. The EPICS Soft IOC is the Modbus Client and runs on a Linux Server. The MODBUS communication protocol is over TCP/IP and uses the standard port 502. During development, "modpoll" application which is a MODBUS test utility was used for in-house SSA testing and Factory Acceptance tests. EPICS support MODBUS within the "Asyn" framework [2]. The application for the Soft IOC uses this Asyn based EPICS Module "modbus".

MODBUS supports several Data Types. The SSA uses only the 'Single bit' and '16-bit Register' Data Types. The communication between the Client (IOC) and the Server (SSA) consists of Request Messages sent from the IOC to the SSA and Response Messages received from the SSA by the IOC. The Request Message reads from or writes to 16-bit Modbus addresses defined by the SSA. The data transfer type is described as an 8-bit MODBUS function. EPICS MODBUS supports eight function codes of which the SSA uses only two function codes:

- Function Code 3: Read 16-bit SSA Registers
- Function Code 6: Write 16-bit SSA Registers

SSA Modbus I/O addresses are contiguous 16-bit Registers and begin from address 1. Spear3 Booster RF IOC currently has access to slightly over 400 SSA addresses. Each EPICS MODBUS Read operation is limited to transferring 125 16-bit words at a time. Write operations are limited to transferring 123 16-bit words. SSA responds to every Read or Write Request Messages from the IOC with a Response Message containing valid

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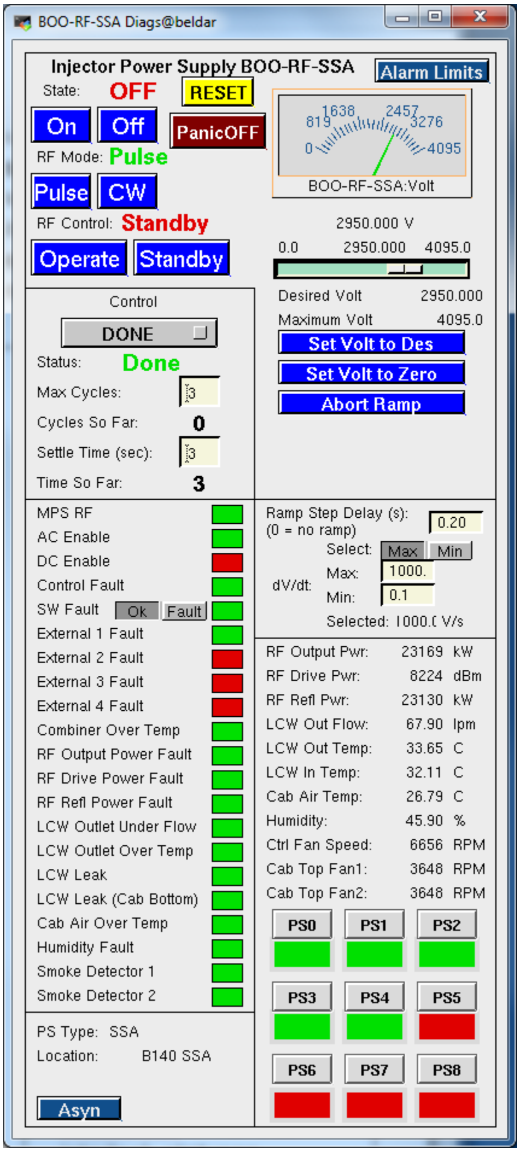
data if successful or error codes. The IOC receives analog information from the SSA such as temperature, voltage, and fan speed etc. via Analog Input (AI) Database (DB) records. These records have their SCAN fields set to "I/O Intr" and are processed when Response Messages from the SSA are received in response to periodic polling via Request Messages. SSA Digital status PVs are constructed from the 16-bit AI values. Analog Output (AO) records are used to write set points to the SSA such as threshold limits and desired voltage. Binary Output (BO) records are used for single-bit operations such as SSA ON/OFF and correspond to a single bit defined within a 16-bit word.

The EPICS EDM panel which is the User Interface of the SSA for the operators is shown in Figure 1.



BOO-RF-SSA Diags@beldar

Injector Power Supply BOO-RF-SSA

State: OFF

RF Mode: Pulse

RF Control: Standby

2950.000 V

Desired Volt 2950.000

Maximum Volt 4095.0

Control

Status: Done

Max Cycles: 3

Cycles So Far: 0

Settle Time (sec): 3

Time So Far: 3

Ramp Step Delay (s): 0.20
(0 = no ramp)

dV/dt: Select: Max Min
Max: 1000.
Min: 0.1
Selected: 1000.(V/s

MPS RF 🟩
AC Enable 🟩
DC Enable 🟥
Control Fault 🟩
SW Fault Ok Fault 🟩
External 1 Fault 🟩
External 2 Fault 🟥
External 3 Fault 🟥
External 4 Fault 🟥
Combiner Over Temp 🟩
RF Output Power Fault 🟩
RF Drive Power Fault 🟩
RF Refl Power Fault 🟩
LCW Outlet Under Flow 🟩
LCW Outlet Over Temp 🟩
LCW Leak 🟩
LCW Leak (Cab Bottom) 🟩
Cab Air Over Temp 🟩
Humidity Fault 🟩
Smoke Detector 1 🟩
Smoke Detector 2 🟩

RF Output Pwr: 23169 kW
RF Drive Pwr: 8224 dBm
RF Refl Pwr: 23130 kW
LCW Out Flow: 67.90 lpm
LCW Out Temp: 33.65 C
LCW In Temp: 32.11 C
Cab Air Temp: 26.79 C
Humidity: 45.90 %
Ctrl Fan Speed: 6656 RPM
Cab Top Fan1: 3648 RPM
Cab Top Fan2: 3648 RPM

PS0 🟩 PS1 🟩 PS2 🟩
PS3 🟩 PS4 🟩 PS5 🟥
PS6 🟥 PS7 🟥 PS8 🟥

PS Type: SSA
Location: B140 SSA

Figure 1: SSA Controls interface.

ATCA LLRF CONTROLS

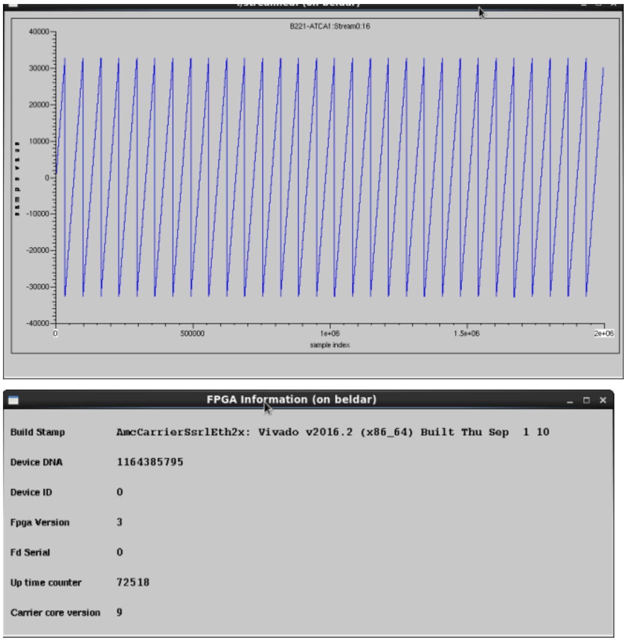
The LLRF controls comprises of a High Performance ATCA system consisting of an ATCA chassis and a SLAC-built custom ATCA carrier board with Advanced Mezzanine Card (AMC) LLRF daughter boards custom-built for the SPEAR3 Booster RF frequency. The ATCA system provides the LLRF drive to the SSA via the Digital to Analog Conversion (DAC) AMC1 module and provides RF Phase and Amplitude Fast Feedback (FF) controls using the RF signals read by the fast digitizer in the Analog to Digital(ADC) AMC0 module.

ATCA LLRF IOC

The LLRF algorithms run on the FPGA while an IOC running on the LinuxRT Server is used for communicating with the ATCA system. The main purpose of this IOC is to provide a User Interface to configure the FPGA and the AMC Modules and to perform periodic acquisition of RF waveforms for diagnostics purposes such as shown in Figure 2.

CPSW

The communication between the FPGA and the IOC is via a custom protocol "Common Platform Software" (CPSW) [3][4] over Ethernet/UDP across the fibre. The IOC uses an Asyn Port Driver based EPICS module that is layered over CPSW. This module provides support for the YAML definitions of the registers inside the FPGA which is used to auto-generate the EPICS PVs. A different Soft IOC running on the Linux Server provides Intelligent Platform Management Interface (IPMI) based monitoring and controls of both the LinuxRT Server and the ATCA chassis.



FPGA Information (on beldar)

Build Stamp AmcCarrierSsrlEth2x: Vivado v2016.2 (x86_64) Built Thu Sep 1 10

Device DNA 1164385795

Device ID 0

Fpga Version 3

Fd Serial 0

Up time counter 72518

Carrier core version 9

Figure 2: ATCA LLRF Controls interface

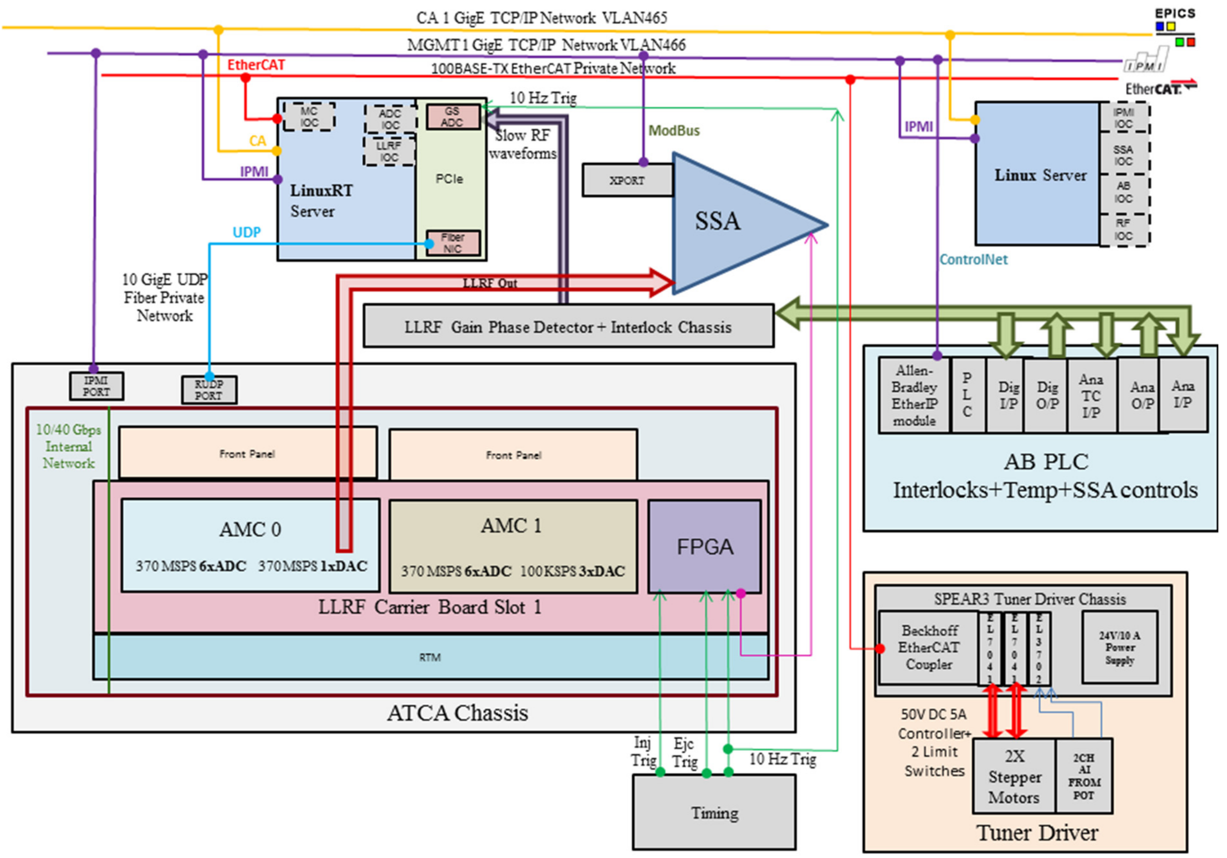

CA 1 GigE TCP/IP Network VLAN465
MGMT 1 GigE TCP/IP Network VLAN466
100BASE-TX EtherCAT Private Network
EPICS
IPMI
EtherCAT
EtherCAT
CA
IPMI
UDP
MC IOC
ADC IOC
LLRF IOC
GS ADC
PCIe
Fiber NIC
LinuxRT Server
10 Hz Trig
Slow RF waveforms
ModBus
XPORT
SSA
IPMI
Linux Server
IPMI IOC
SSA IOC
AB IOC
RF IOC
ControlNet
10 GigE UDP Fiber Private Network
LLRF Out
LLRF Gain Phase Detector + Interlock Chassis
Allen-Bradley EtherIP module
P L C
Dig I/P
Dig O/P
Ana TC I/P
Ana O/P
Ana I/P
AB PLC
Interlocks+Temp+SSA controls
IPMI PORT
RUDP PORT
10/40 Gbps Internal Network
Front Panel
Front Panel
AMC 0
370 MSPS 6xADC 370 MSPS 1xDAC
AMC 1
370 MSPS 6xADC 100KSPS 3xDAC
FPGA
LLRF Carrier Board Slot 1
RTM
ATCA Chassis
SPEAR3 Tuner Driver Chassis
Beckhoff EtherCAT Coupler
EL7041
EL7041
EL3702
24V/10 A Power Supply
50V DC 5A Controller+ 2 Limit Switches
2X Stepper Motors
2CH AI FROM POT
Tuner Driver
Inj Trig
Ejc Trig
10 Hz Trig
Timing

Figure 3: Block diagram of SPEAR3 Booster RF controls layout.

RF CAVITY TUNER CONTROLS

While the fast response LLRF Fast Feedback controls is implemented inside the FPGA of the High Performance ATCA Controls System described above, slow response LLRF feedback is accomplished via a five-cell cavity tuner control that tunes the Booster RF cavity frequency and balances the fields inside the cavity cells. Two movable tuners are present in cell 1 and cell 5 of the RF cavity and these are controlled by conventional stepper motor drives. Tuner control is implemented via two EtherCAT [5] based Beckhoff modules that control the cell1 and cell5 stepper motors which have freedom of movement in two axes – up or down. The upper and lower hard stop limit switch statuses are sensed and read as well. A linear potentiometer reads back the motor position which is read into an EtherCAT Analog Input module. All the EtherCAT Beckhoff modules as well as the drive amplifiers and power supply are located inside the Tuner Driver chassis. An EPICS Soft IOC running on the LinuxRT Server interfaces with the EtherCAT coupler module over a dedicated Ethernet cable. The functions and implementation of this Soft IOC are summarized below.

EtherCAT Tuner IOC

An EPICS Soft IOC runs on the LinuxRT Server and communicates with the Beckhoff EK1100 (EtherCAT coupler) module over the EtherCAT fieldbus protocol. It configures and controls the two EtherCAT motor driver modules EL7041 (Stepper motor driver) using Etherlab's [6] EtherCAT Master Driver open source software which is installed as a Kernel Module compiled for the LinuxRT operating system. The EtherCAT bus scanner software [7] runs on the LinuxRT Server. This is a user space utility that processes EtherCAT messages and drives the actual bus cycles and provides them to the EPIC IOC acting as a registered listener on the EtherCAT bus. Beckhoff EL3702 (2-ch AI 100KSPS 16 bit) Analog Input module is used for the potentiometer-based motor position read back. Tuner motor calibration showed linearly proportional position read back values corresponding to potentiometer readings in the full range of tuner movement as shown in Figure 4 below.

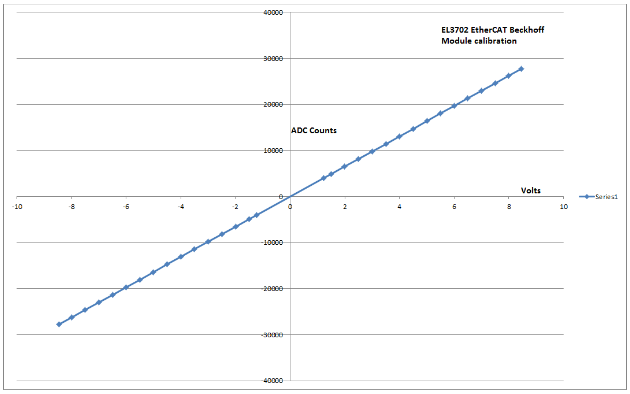
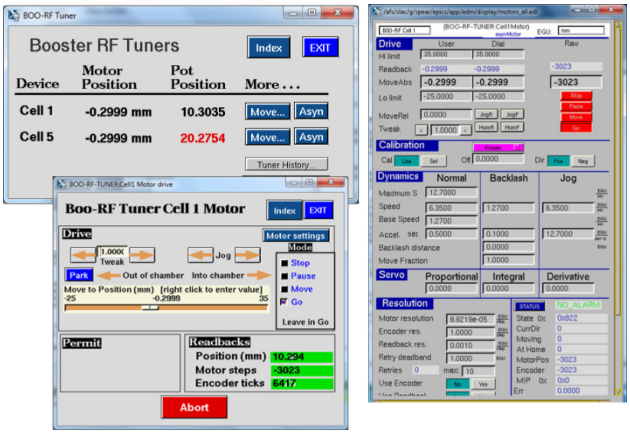


Figure 4: Booster RF Cavity Tuner Motor Calibration.

The IOC uses EPICS Asyn Port Driver layered over the EtherCAT fieldbus scanner software. Two Asyn Driver ports are created corresponding to cell1 and cell5 tuner motor driver, and one for the bus master status. EPICS motor PVs are automatically generated from the device names assigned in the EtherCAT chain description XML file.

The Cavity Tuner Controls User Interface is shown below in Figure 5.



Booster RF Tuners

Device	Motor Position	Pot Position	More . . .
Cell 1	-0.2999 mm	10.3035	Move... Asyn
Cell 5	-0.2999 mm	20.2754	Move... Asyn

Boo-RF Tuner Cell 1 Motor

Tweak 1.000(

Move to Position (mm) [right click to enter value]
-25 -0.2999 35

Readbacks
Position (mm) 10.294
Motor steps -3023
Encoder ticks 6417

BOO-RF Cell 1 (BOO-RF-TUNER:Cell1Motor) asynMotor EGU: mm

Drive	User	Dial	Raw
Hi limit	35.0000	35.0000	
Readback	-0.2999	-0.2999	-3023
MoveAbs	-0.2999	-0.2999	-3023
Lo limit	-25.0000	-25.0000	
MoveRel	0.0000		
Tweak	1.0000		

Calibration
Cal Use Set Off 0.0000 Dir Pos Neg

Dynamics	Normal	Backlash	Jog
Maximum S	12.7000		
Speed	6.3500	1.2700	6.3500
Base Speed	1.2700		
Accel. sec	0.5000	0.1000	12.7000
Backlash distance		0.0000	
Move Fraction		1.0000	

Servo	Proportional	Integral	Derivative
	0.0000	0.0000	0.0000

Resolution
Motor resolution 9.9219e-05 EGU/step
Encoder res. 1.0000 EGU/step
Readback res. 0.0010 EGU/step
Retry deadband 1.0000 EGU
Retries 0 max: 10
Use Encoder No Yes

NO_ALARM
State 0x 0x822
CurrDir 0
Moving 0
At Home 0
MotorPos -3023
Encoder -3023
MIP 0x 0x0
Err 0.0000

Figure 5: Cavity Tuner Controls interface.

PCIE DIGITIZER GTR CONTROLS

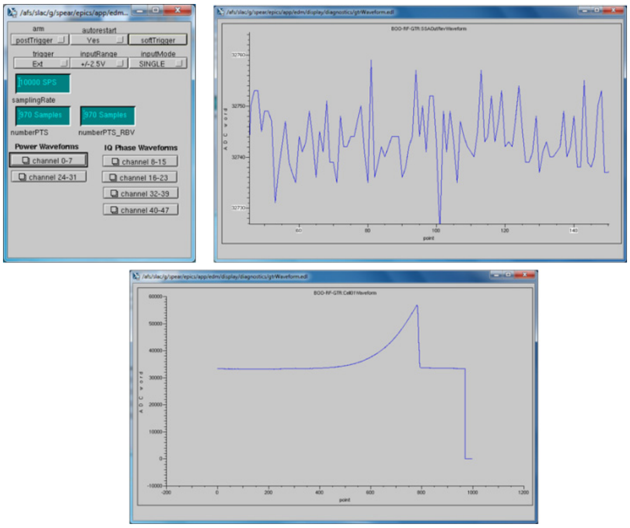
There are several Booster RF signals whose phase and amplitude need to be monitored continuously to keep track of the health of the overall system even if they are not used in LLRF feedback. The "Gain Phase Detector Chassis" was built to measure the amplitude and phase of such signals and have them monitored via a medium-speed digitizer card in the LinuxRT Server. When triggered, the General Standards 16ai64ssa PCIe ADC digitizes the envelopes of the amplitude and phase of the LLRF signals such as the forward and reverse powers from the SSA and the 5-cell Booster RF cavity probes. This 16-bit 64-channel ADC board is installed in the Server.

PCIe GTR IOC

The digitizer IOC uses an EPICS Asyn based Generic Transient Recorder (GTR) [8] module to interface with and configure the digitizer driver and to acquire the input signal waveforms. The following GTR configurations are supported:

- Mode: "Post Trigger" or "Disarm". In Post Trigger mode, the digitizer will start sampling the input signals when a trigger is received. It will not sample when it is "Disarmed".
- Auto Restart: When enabled, the device is automatically rearmed after all input signals have been sampled and read in.
- Trigger type: "External" or "Soft". When set to "External", the digitizer is triggered by a 10 Hz pulser trigger which is synchronized with the Booster Ejection trigger cycle. A "Soft" trigger is used for testing and does not need an external trigger.
- Sample Rate: Number of samples per second. This is the same for rate for all input channels.

The sampled signals are read in as waveform records by the IOC. Currently, Amplitude and Phase (as I and Q) for each of the following ten signals are monitored: (a) Cavity Cell probes 1 through 5. (b) SSA Output Forward and Reverse power. (c) Circulator Input and Output, Forward and Reverse power. Figure 6 shows the User Interface for the GTR PCIe digitizer and a couple of waveforms that are sampled.



arm postTrigger
autorestart Yes
trigger Ext
inputRange +/-2.5V
inputMode SINGLE
samplingRate 10000 SPS
numberPTS 970 Samples
numberPTS_RBV 970 Samples

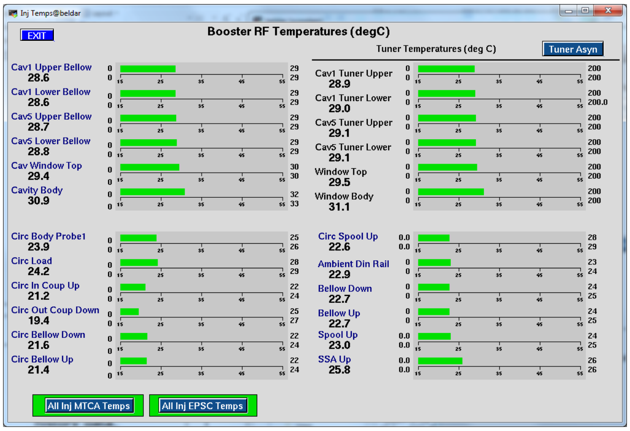
Figure 6: PCIe Digitizer GTR Controls interface.

PLC MPS IOC CONTROLS

The Machine Protection System for the upgraded Booster RF Cavity controls comprises of Allen Bradley PLC modules from the CompactLogix family. These PLCs monitor such quantities as temperatures, vacuum, water flow, etc. and provide machine protection by fault detection and system trips.

MPS IOC

The MPS Soft IOC runs on the Linux Server and communicates with the Allen Bradley PLC module using the EtherIP module [9]. Read back of various Booster RF scalar analog signals such as temperature, pressure, voltage, current etc. and digital Interlock statuses are provided by the IOC. The IOC provides Digital Output control for Fault Reset. Figure 7 shows the User Interface for the read back of the various temperatures.



Cav1 Upper Bellow 28.6
Cav1 Lower Bellow 28.6
Cav5 Upper Bellow 28.7
Cav5 Lower Bellow 28.8
Cav Window Top 29.4
Cavity Body 30.9
Circ Body Probe1 23.9
Circ Load 24.2
Circ In Coup Up 21.2
Circ Out Coup Down 19.4
Circ Bellow Down 21.6
Circ Bellow Up 21.4

Cav1 Tuner Upper 28.9
Cav1 Tuner Lower 29.0
Cav5 Tuner Upper 29.1
Cav5 Tuner Lower 29.1
Window Top 29.5
Window Body 31.1
Circ Spool Up 22.6
Ambient Din Rail 22.9
Bellow Down 22.7
Bellow Up 22.7
Spool Up 23.0
SSA Up 25.8

Figure 7: PLC MPS Controls interface.

CONCLUSION

The initial phase of the commissioning of the controls for the upgraded SPEAR3 Booster RF hardware has been completed successfully. The ATCA LLRF IOC and the PLC MPS IOC will be upgraded to include more features in the near future. A slow feedback RF IOC running on the Linux Server is also planned and will be implemented during the current run. Operator EDM panels will need to be developed and deployed in production in addition to the Expert panels that are available during the commissioning period. Operator training for the new controls is also planned. The migration of the EPICS software from the existing Concurrent Versions System (CVS) repository based source control to Git based source control is also planned.

ACKNOWLEDGMENT

Several SLAC engineers contributed towards the Booster RF Upgrade project and our thanks goes to all: TID AR RF Systems Department, TID AIR Advanced Controls Systems Department, AD EED Software Department, and SSRL Controls and Networking team members for their valuable contributions during the development of the project and for their continued support in making it a very successful one.

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