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THE IMPLEMENTATION OF KSTAR FAST INTERLOCK SYSTEM USING C-RIO*

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Abstract

In the tokamak using superconducting magnet that can operate in long pulse with high temperature and density plasma, the interlock system is becoming more and more important to protect the device itself. Korean Superconducting Tokamak Advanced Research (KSTAR) achieved high-confinement mode (H-mode) operation for 70 seconds in 2016. In this case, it is necessary to have precise and fast operation protection device to protect Plasma Facing Component (PFC) from high energy and long pulse plasma. The higher the energy of the plasma, the faster the protection is required, and the protection logic should be implemented to process the signals from the various devices as quickly as possible. To meet these requirements, KSTAR implemented the Fast Interlock System (FIS) using NI's Compact Reconfigurable Input Output (c-RIO). The c-RIO is a device using FPGA (Field Programmable Gate Array), its form is similar to PLC (Programmable Logic Controller) and is easy to expand I/O. The implemented protection logic is performed in the FPGA, so input and output can be processed quickly and much. The EPICS IOC performs communication with peripheral devices (PCS, CCS, SIS, heating devices) and operation of c-RIO. In this paper, we describe the detail implementation of the FIS in the actual KSTAR situation, as well as future plan.

INTRODUCTION

The fast interlock is an interlock that stops the heating device to prevent components in the vessel from being damaged during plasma discharge. Tokamak using superconducting magnets is capable of long pulse operation and high temperature and density plasma confinement, so that the function of the interlock system to protect the device is becoming more important than the conventional tokamak. KSTAR (High Superconducting Tokamak Advanced Research) achieved high-confinement mode (H-mode) operation for 70 seconds in 2016 [1]. In this case, KSTAR also has an accurate and fast-acting protection device for protecting in-vessel components from high energy and long pulse plasma. The higher the energy of the plasma, the faster the protection device is needed, and the protection logic must be realized using the signals from various related devices.

OVERVIEW OF KSTAR FAST INTERLOCK SYSTEM

The final target of the KSTAR device [2] is 2MA for plasma current and 300second for pulse length, and it is in the process of reaching the target value through continuous upgrade. The KSTAR team is constantly contemplating how to protect equipment from high-energy and long pulse plasma [3-5]. As results of these troubles, three versions of fast interlock system have been constructed, tested and supplemented. The core contents can be summarized as follows [6]:

- 1st Version, 2009
  Central Control System (CCS) activates heating stop from Plasma Control System (PCS) using RFM within 200 ms.
- 2nd Version, 2012
  Fast interlock interface activates heating stop from plasma current (Ip) signal using Timing Synchronization System (TSS).
- 3rd Version, 2014
  2nd Version plus
  Plasma Facing Component (PFC) fault, NB armor fault, CCS to PCS using RFM

Running the previous three versions of FIS, we needed to migrate to CCS functionality that works on the existing VME VxWorks. We also needed a new system that could easily extend I/O, easily implement control logic, and flexibly accommodate various types of information. First, the new system includes NI-Compact-RIO, which has an FPGA as a main controller and supports various I/Os. It also can be configured to process information with peripheral devices and communicate with compact-RIO in the EPICS IOC Server. The NI compact-RIO is chosen as the main processor with the following benefits.

- Fast response time, fast processing time.
- Proven device, platform, high reliability.
- Easily implement and modify logic using FPGA and labview.
- Fast system development.
- Communication with EPICS using IRIO is possible.

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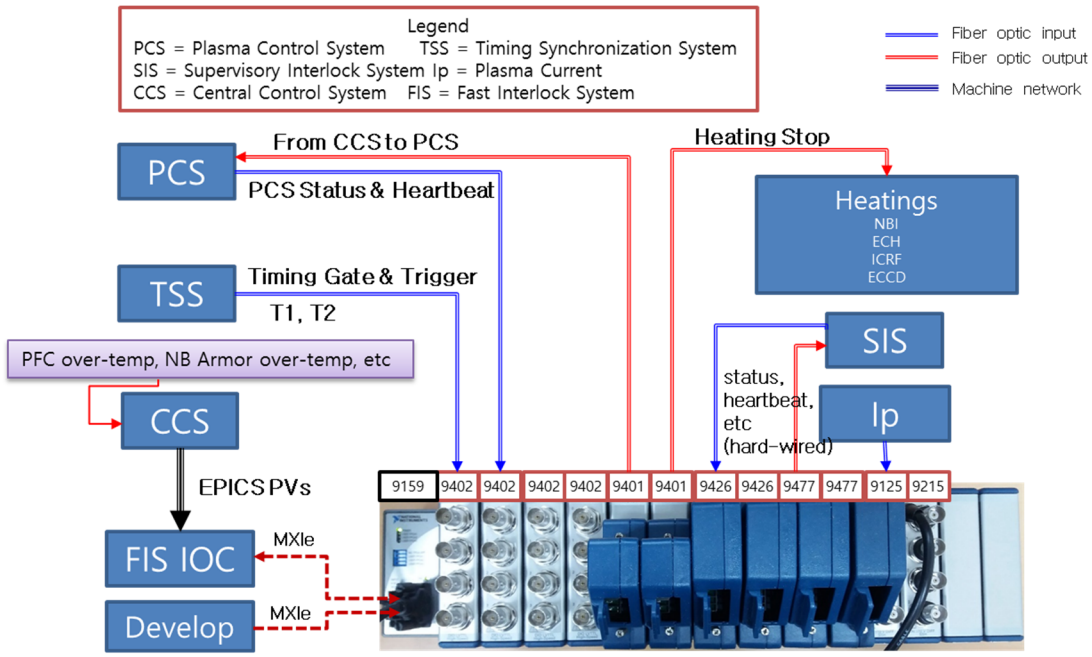

Figure 1: Configuration of KSTAR fast interlock system.

Table 1: c-RIO Module Descriptions

Modules	Description	No.
NI 9159	14-slot chassis, LX110 FPGA, MXIe	1
NI 9402	4-ch, 55 ns, DIO, BNC	4
NI 9401	8-ch, 100 ns, DIO, 25pin D-SUB	2
NI 9426	32-ch, 7 μs, DI, 37pin D-SUB	2
NI 9477	32-ch, 8 μs, DO, 37pin D-SUB	2
NI 9215	4-ch, 100 kS/s/ch, 16 bit AI, BNC	2

IMPLEMENTATION OF KSTAR FAST INTERLOCK SYSTEM

Configuration

The NI 9159 is equipped with a Virtex-5 LX110 FPGA in a 14 slot chassis and uses MXI-Express to communicate with the host EPICS IOC using IRIO. We have installed 4 NI-9402, 2 NI-9401, 2 NI-9426, 2 NI-9477, and 2 NI-9215 in consideration of future expansion [7]. The description of each module is shown in table 1. And Figure 1 shows the configuration of KSTAR Fast Interlock System. The basic concept is that compact-RIO which is a FIS main controller, processes the calculation based on the given information and directs the heating stop signal directly to each heating device. More detail, the conditions for the heating stop can be listed as follows.

- While T1 ON, Ip < Ip_{th}
- While T2 ON, Ip > Ip_{th} then Ip < Ip_{th}
- PCS fault
- NBI armour over-temperature fault via EPICS
- PFC over-temperature fault via EPICS

FPGA Programming Description

FPGA has the feature of perfect multi-tasking. Using these characteristics, the control logic is divided into three loops. Considering the processing speed of installed DI and DO module, the operating clock of the control loop is set as 100 kHz (time base as 10 µs).

The Ip protection loop generates a heating stop when Ip is less than the threshold when the T1 (+ 210 ms to shot stop) signal transmitted from the TSS is ON using the plasma current (Ip) signal from the AI module (NI 9215). When T2 (-14.9 sec to shot stop) is ON, and Ip is greater than the threshold then it becomes smaller than threshold, the heating stop is also generated. The counter loop counts the occurrence time of the event starting from T2. As shown in Figure 2, a counter to record the PCS heartbeat abnormality occurring at 1 kHz cycle, a counter to record when the PCS fault occurred, a counter to record the occurrence time of the previous heating stop, and a counter to record the NBI armour fault are transmitted to EPICS PVs such as auxAI4, auxAI5, auxAI6 and auxAI7. Finally,

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the heating stop and reset loop performs the function of delivering the previously generated heating stop signal to each heating device and transmitting the fault using EPICS PV that received from CCS to PCS. This loop also includes the function of reset signal and function of selection whether the heating stop is enable or disable for individual heating device. The concept logic can be easily embedded on FPGA using NI's labview FPGA module. Advantages of the FPGA programming using labview can be listed as follows.

- Easy implementation using labview programming rule.
- Good expandability by loop base programming.
- No need on clock calculation.
- Easy communication with EPICS using IRIO driver [8].
- Easy FPGA logic debugging using labview host interface.

LabVIEW FPGA Code for the Counter Loop

In Figure 2, using LabVIEW FPGA, the counter loop which showed in the Figure 3 displayed with concept diagram is shown. In this logic, when timing window T2 is ON, the counter increase 1 by 10 µs cycle, and each counter works independently.

Functional Operation Test

Figure 4 shows the result of the operation test for the function of counting the PCS heartbeat error among the mentioned counter loop. The test proceeds to the reset and action process. By comparing the time between the ON time of T2 recorded in EPICS PV and the time of occurrence of heartbeat error and the time recorded in the counter, it can be confirmed whether the function operates normally. Heartbeat (HBT) fault occurs when the same value exceeds 200 times during 1 kHz HBT at 10 µs clock. Theoretically, the first detection is possible only after 2 ms. In two trials, the detection time is approximately 2 ms, indicating that the function is working normally.

CONCLUSION AND FUTURE WORKS

The 4th version of the KSTAR Fast Interlock System was installed hardware and software for 2017 operation. However, due to the early termination of the unexpected campaign, commissioning on actual equipment has to be delayed until 2018. Although not applied in the actual devices, we conducted a test to verify FPGA function and confirmed that it works with the intended function. The upgraded FPGA programming is being prepared for more features and considering various situations, and will be applied in 2018 operation. Also in the long term, Fast Interlock Server will share information with PCS and RFM Gateway using Synchronous Databus Network (SDN) of ITER.

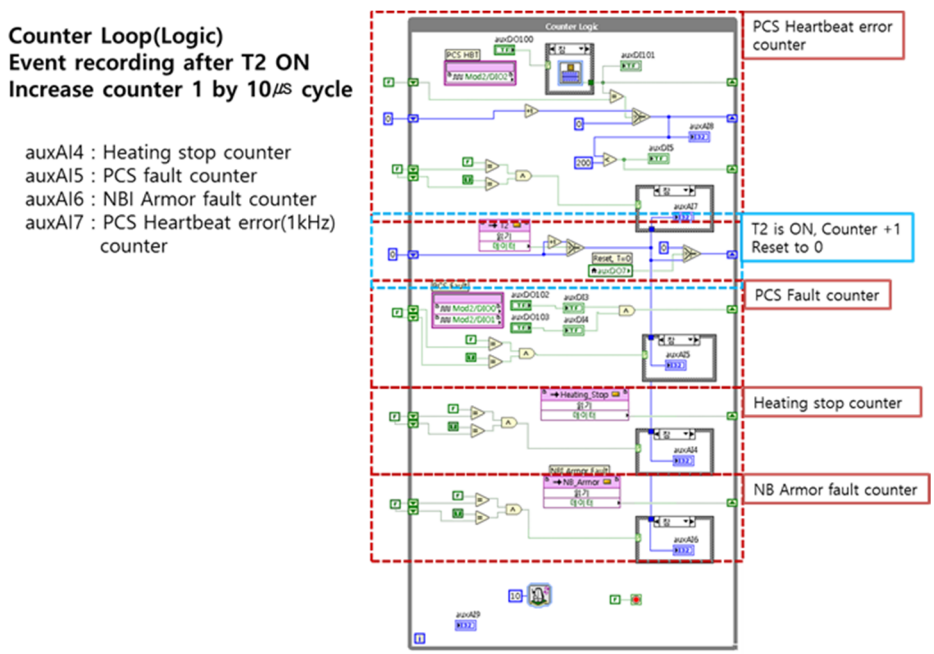

Figure 2: LabVIEW FPGA code for the counter logic.

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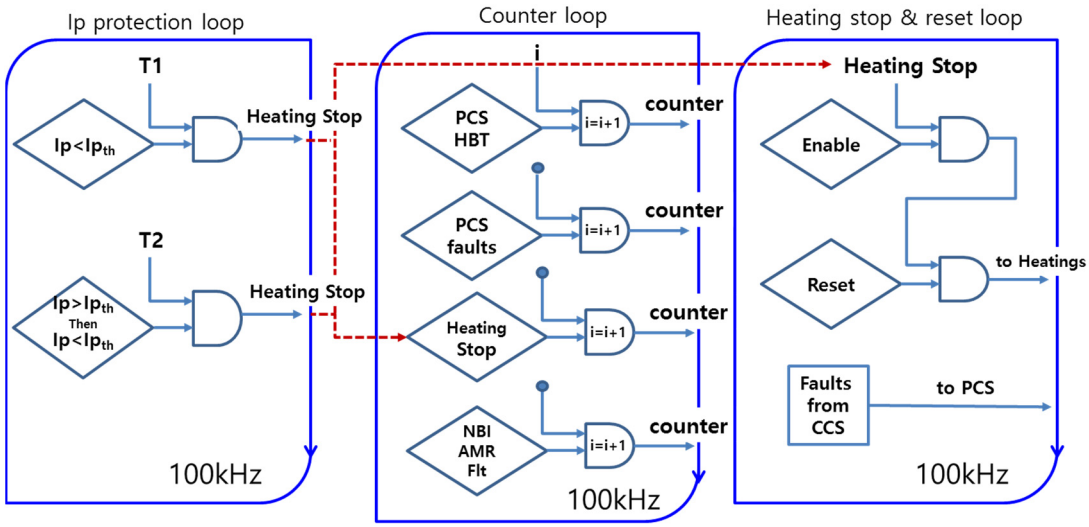

Figure 3: FPGA logics for three independent loops.

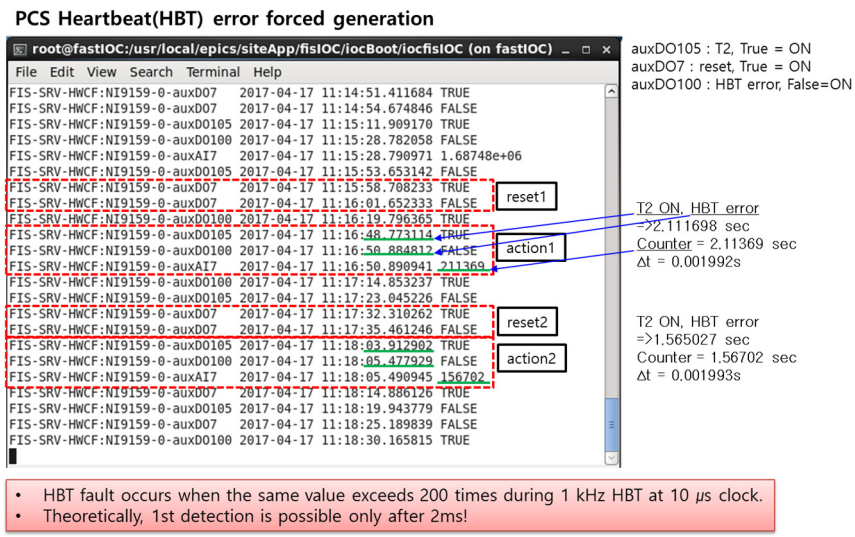

Figure 2: Functional operation test result for the PCS heartbeat error counter.

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