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DESIGN OF THE FRONT-END DETECTOR CONTROL SYSTEM OF THE ATLAS NEW SMALL WHEELS*

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Abstract

The ATLAS experiment will be upgraded during the next LHC Long Shutdown (LS2). The flagship upgrade is the New Small Wheel (NSW) [1], which consists of 2 disks of Muon Gas detectors. The detector technologies used are Micromegas (MM) and sTGC, providing a total of 16 layers of tracking and trigger. The Slow Control Adapter (SCA) is part of the Gigabit Transceiver (GBT) - "Radiation Hard Optical Link Project" family of chips designed at CERN, EP-ESE department [2,3], which will be used at the NSW upgrade. The SCA offers several interfaces to read analogue and digital inputs, and configure front-end Readout ASICs, FPGAs, or other chips. The design of the NSW Detector Control System (DCS) takes advantage of this functionality, as described in this paper.

THE NEW SMALL WHEEL UPGRADE OF THE ATLAS MUON SPECTROMETER

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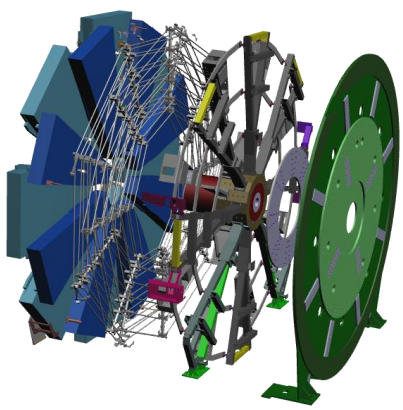

Figure 1: An exploded view of the NSW. From left to right: The detector sector envelopes, the alignment system, the structure and the New JD (shielding and support).

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SCA FUNCTIONALITY

The SCA ASIC offers several interfaces to read & control analogue/digital levels, and configure front-end Readout ASICs, FPGAs, or other chips.

The interfaces offered by the SCA are:

- 1 ADC channel, providing 31 input lines and one on-chip temperature sensor
- 1 JTAG serial bus master channel, with programmable transaction length and frequency
- 1 Digital I/O pin interface, which gives access to 32 general purpose pins (can be individually set as input or output and can generate interrupt requests)
- 16 independent I2C master serial bus channels (transfer rates 100kHz-1MHz)
- 1 SPI serial bus master with 8 individual slave select lines (programmable transaction length and frequency)
- 1 DAC interface, giving access to 4 converters with 8-bit resolution and with input range 0..1V

As described in the next sections, the above interfaces prove extremely useful for the detector control.

THE GBT-SCA IN THE NEW SMALL WHEEL

There is a big number of SCAs in the NSW ecosystem (almost 7000), each of which will be placed on a separate PCB. Given the embedded nature of this functionality, the control data needs to follow the main path like the signal and timing data.

Concerning SCA downstream connections, there will be many cases that the SCA connects to 8 front-end chips. This creates complexity at the level of the software development since parallelization of the data upload becomes a necessity but not a given.

COMMUNICATION PATH

The communication chain starts in the control room with an OPC-UA client, which talks to a quasar-based [4] OPC-UA server in the service cavern. The server, in turn, communicates the data through a front-end link exchange and a fiber cable to arrive to the on-detector electronics (Fig. 2). Some details are given in the following subsections.

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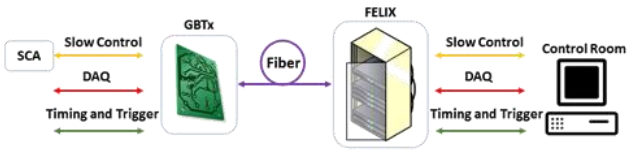

Figure 2: The NSW data path.

On-Detector Electronics

The SCA is hosted at the on-detector electronics, the front-end. Through the use of the GBTx chip, the various links are routed through the fiber to the service cavern (USA15). These links carry data for slow control, signal information (DAQ) and timing & trigger.

Front-End Link Exchange (FELIX)

The FELIX [5] PC machines are responsible for gathering the e-link data from all the front-end electronics, through optical fiber. These machines are situated in the service cavern, which is safe from radiation.

On the FELIX machines, the data arrives first on a "FELIX-card" where the first unpacking is done, and then a software application, "FELIXCore", is handling the data and forwarding to other machines or applications.

USE CASES IN THE DCS

The detector control system (DCS) of the detector participates in the monitoring, configuration and calibration of the detector.

Monitoring

It is required to monitor certain voltage levels on the front-end electronics; either ASIC pins that are used to monitor or test the output, or temperature sensors.

For this purpose, the Analog to Digital Converter (ADC) interface of the SCA is used. It offers 32 channels, 1 of which is an SCA-internal temperature sensor.

Configuration

The NSW includes more than 40k front-end ASICs and a few tens of FPGAs, which need to be configured before every run of the experiment. This process needs to be efficient and quick, since it needs to happen a few times per day.

The main ASIC to be configured is the VMM, the front-end signal pre-processing chip which can read-out 64 channels. A few kbytes of configuration data include thresholds for each channel, but also global registers to define the gain, time-to-amplitude conversion and many others. For this procedure we need to use the SPI master to communicate with the 8 SPI slaves in the VMMs. Also the GPIO interface is required, to act as an enable signal.

Moreover, a similar scheme is used for configuration of the TDS chip, which is used for timing and trigger. This is done with the I2C interface.

Another challenging task is the upload of a bit-stream to the FPGAs, through the same data path. The bit-streams in use can go as high as 14MB. Due to the protocol limitations, this data needs to be sent to the SCA in 32-bit chunks, which then is sent in 128-bit chunks to the FPGA, the complete upload requires a lot of optimization. Identification and elimination of the bottlenecks is done in cooperation with all systems in the communication path.

Calibration

A less frequent but equally important task is the calibration of the front-end electronics. The main part is the timing and charge calibration of the front-end electronics. Various calibrations are needed:

- Gain calibration is done by varying the signal input using the internal pulser of the chip. A specific configuration file needs to be loaded on the VMM chips, which is done with the SCA.
- Calibration of a time-to-amplitude converter is done by skewing the input clock, which again happens with adapting the configuration of a specific on-board.
- Baseline and noise level is defined by reading out each channel output with the ADC when no collisions are happening.

CONCLUSION

The SCA chip will be used for the configuration and monitoring of the on-detector electronics at the New Small Wheel upgrade of the ATLAS experiment, at the LHC. The use and integration of this ASIC in the NSW electronics ecosystem was presented and summarized.

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