

# LO BOARD FOR 704.42 MHz CAVITY SIMULATOR FOR ESS\*

I. Rutkowski, K. Czuba, M. Grzegorzówka, ISE, Warsaw University of Technology, Poland

## Abstract

This paper describes the requirements, architecture, and measurements results of the Local Oscillator (LO) generation board prototype. The design will provide low phase noise clock and heterodyne signals for the 704.42 MHz Cavity Simulator for the European Spallation Source. RF signal detection has critical influence on the simulation's performance and its quality depends on the quality of the two aforementioned signals. The clock frequency is a subharmonic of the reference frequency and choice of the frequency divider generating the clock signals is discussed. The performance of selected dividers was compared. The LO frequency must be synthesized and frequency synthesis schemes are investigated. Critical components used in the direct analog scheme are identified and their selection criteria were given.

## INTRODUCTION

This paper describes the requirements, architecture, and measurements results of the Local Oscillator Generation board prototype. It is a standalone module designed for the Cavity Simulator project [1] and is referred to as CS-LOG.

The Cavity Simulator will detect the amplitudes and phases of the input RF signals by downconverting them to an intermediate frequency (IF). Those signals will be sampled and digitized by high-speed precise analog-to-digital converters. The architecture necessitates synthesis of a low phase noise clock and heterodyne/LO signals. The CS-LOG module will be responsible for generation of those signals based on an externally fed reference signal. The prototype is also used to verify performance of the design intended for the low level radio frequency (LLRF) control system.

A LLRF system stabilizes the electromagnetic field inside accelerating modules. As with Cavity Simulator's signal detection, the field detection has critical influence on the regulation's quality.

The European Spallation Source (ESS) LLRF control system will be based on the Micro-Telecommunications Computing Architecture (MTCA) [2]. The remote diagnostic functionality is considered one of the main benefits of the platform. The LO board will have a rear transition module form factor and it will supply 4 neighboring LLRF systems [3].

## REQUIREMENTS

The functional requirements put on the CS-LOG and the LO RTM slightly differ. The common requirements are presented below and the ones specific to CS-LOG follow.

## Common Requirements

The input reference frequency is 704.42 MHz. The clock to reference frequency ratio is 1/6 and the IF to reference frequency ratio is 1/28 or 1/22, corresponding to 117.40 MHz and 25.16 / 32.02 MHz, respectively. LO and clock signals' phase noise requirements are presented in Table 1 and they are dependent on the sufficient quality of the reference signal. Both clock and LO signals shall be sine waves with maximum harmonic spurious level of -60 dBc. The non-harmonic spurious shall be not greater than -60 dBc for clock and not greater than -50 dB for LO.

The VSWR on each port (Reference Input, LO Outputs, CLK Outputs) shall be not greater than 1.5, corresponding to return loss of -13.979 dB.

## CS-LOG Requirements

The module shall additionally fulfill the following requirements:

- the module shall provide 2 LO outputs (power level range: +10 to +15 dBm),
- the module shall provide 4 clock outputs (power level range: +5 to +10 dBm),
- the module shall be controlled through an isolated I2C bus.

## DESIGN

This section describes frequency synthesis and signal conditioning aspects of the design. The measurements presented were obtained using evaluation boards.

## LO Frequency Synthesis Considerations

The LO frequency ( $f_{LO} = f_{reference} \pm f_{intermediate}$ ) is not a harmonic or a subharmonic of the reference signal and must be synthesized. Synthesizers may be classified into three types:

- Direct Analog,
- Direct Digital,
- Indirect Digital.

The first approach uses frequency dividers, mixers, and filters. It closely follows the phase noise of the reference signal, with additional noise induced by the frequency divider and the mixer. Far from carrier the noise can be improved by using a narrow band-pass filter. Such filters increase the cost of the device and are sensitive to mechanical vibrations.

A Direct Digital Synthesizer (DDS) uses a numerically controlled oscillator feeding a digital-to-analog converter, both being synchronized by the reference clock. The intermediate to reference frequency ratio is 1/22 or 1/28 which results in systemic frequency error by using a binary frequency tuning word.

An Indirect Digital Synthesizer utilizes a PLL with an integer or fractional frequency divider. For offset frequencies

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Table 1: Phase Noise Performance Requirements

| Offset (Hz)                                                              | 10   | 100  | 1k   | 10k  | 100 k | 1M   | 10 M |
|--------------------------------------------------------------------------|------|------|------|------|-------|------|------|
| LO Phase noise SPD $\left(\frac{\text{dBc}}{\sqrt{\text{Hz}}}\right)$    | -90  | -110 | -125 | -140 | -149  | -152 | -154 |
| Clock Phase noise SPD $\left(\frac{\text{dBc}}{\sqrt{\text{Hz}}}\right)$ | -104 | -120 | -130 | -140 | -145  | -150 | -153 |

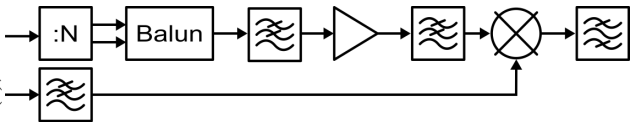


Figure 1: Block diagram of the LO synthesis circuit.

within the loop bandwidth the phase noise is determined by the reference signal’s characteristics distorted by the loop’s noise. Outside the loop bandwidth the noise is dominated by the VCO used and optional output frequency dividers.

The Direct Analog scheme is preferred and was selected for the design because no systemic frequency error is introduced and the far from carrier uncorrelated phase noise is reduced.

In the next two sections details of the mixer-based scheme of LO generation are discussed.

Direct Analog Synthesizer

A real upconverting mixer has at its output following spectral components:

- desired sideband,
- undesired sideband,
- reference ( $f_{\text{reference}}$ ),
- higher order mixing products, including  $f_{\text{reference}} \pm N \cdot f_{\text{intermediate}}$ .

All the undesired components must be suppressed using a band-pass filter. The pass-band width is limited by the IF signal bandwidth on one side and the closest undesired spectral components ( $f_{\text{reference}}$  and  $f_{\text{reference}} \pm 2xf_{\text{intermediate}}$ ) on the other. To lessen the requirements on the filter the higher sideband ( $f_{\text{reference}} + f_{\text{intermediate}}$ ) should be selected and the mixer should have isolation (transmission of signal between LO and RF ports) as high as possible. The mixer was selected for high isolation. It has low nominal LO power level (+10 dBm), which also implies low output power level. Therefore the desired sideband must be amplified (after filtering). To avoid degradation due to noise added by the LO signal amplifier, the sideband’s power should be kept as high as possible, and a low noise amplifier should be selected.

Figure 1 depicts block diagram of the LO synthesis circuit. Low-pass filters are used at the mixer’s inputs to suppress harmonics generated by the mixer, which can disturb other circuits. In the next subsection the selection of the IF divider is discussed.

IF Divider

The phase noise of the mixer output signal is a sum of the reference signal noise and additive noise of the frequency divider’s output signal (increased by any amplifier in the

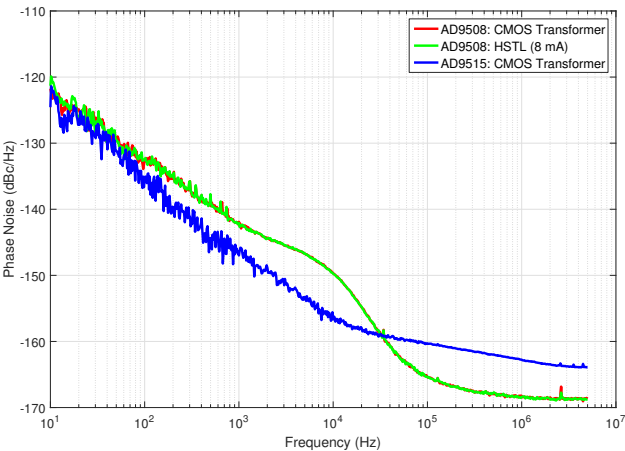


Figure 2: Phase noise spectra of IF dividers for various output signaling standards and types of counters. Division ratio: 22, input frequency: 704.42 MHz.

chain). According to authors best knowledge there are no reliable models of frequency dividers’ output phase noise.

The frequency divider in this application must divide the input frequency by a high programmable ratio (28 or 22). Many frequency divider ICs are available on the market, but only a very limited subset of them can be used for this design. Most of them belong to the AD95XX family made by Analog Devices, with few chips from other series and manufacturers. The AD95XX family supports multiple signaling standards, including CMOS, HSTL, LVPECL, and LVDS. The performance of different standards was compared using two devices under the assumption that the two types frequency division logic (1-1024 and 1-32) and outputs buffer circuits are common for all chips in the family.

The phase noise spectra of the dividers’ output signal in divide-by-22 configurations are compared in Fig. 2. The results in the divide-by-28 were very similar and therefore are not presented. To simplify the analysis the phase noise was integrated (see Table 2) per decade of offset frequency(up to 5 MHz, limited by Agilent E5052B’s offset bandwidth in the given input frequency range). The AD9508 was selected due to its lower total jitter in the 10 Hz – 1 MHz band.

Clock Divider

The clock frequency is a subharmonic of the reference frequency (frequency ratio 1/6) and it’s possible to generate the clock frequency using a frequency divider. Usage of DDS was excluded because of systemic frequency error introduced by the binary frequency tuning word for the given frequency ratio.

Table 2: Comparison of the Output Signal's Jitter (Integrated Phase Noise, in fs) per Frequency Offset Decade of Selected IF Dividers. Division Ratio: 22, Input Frequency: 704.42 MHz.

| Divider ↓ | Start Offset (Hz) | 10    | 100   | 1k    | 10k   | 100 k | 1M    | 10     | 1k     |
|-----------|-------------------|-------|-------|-------|-------|-------|-------|--------|--------|
|           | End Offset (Hz)   | 100   | 1k    | 10k   | 100 k | 1M    | 5 M   | 5 M    | 5 M    |
| AD9508    | CMOS Transformer  | 26.83 | 24.76 | 28.26 | 21.80 | 24.54 | 47.20 | 73.77  | 64.06  |
|           | HSTL 8mA          | 25.66 | 24.94 | 28.37 | 21.80 | 24.55 | 47.45 | 73.63  | 64.30  |
| AD9515    | CMOS Transformer  | 21.64 | 16.23 | 16.03 | 22.80 | 53.50 | 92.76 | 113.93 | 110.64 |

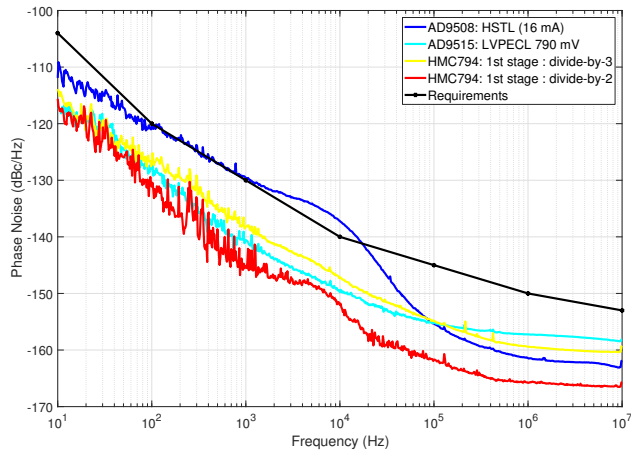


Figure 3: Phase noise spectra of frequency dividers for various output signaling standards and types of dividers. Division ratio: 6, input frequency: 704.42 MHz.

As observed earlier the clock frequency should be generated using a frequency divider. The two static frequency dividers considered for IF synthesis (AD9508 and AD9515) were compared with two stage divider using HMC794LP3E, which most probably is an injection-locked divider. This divider has the division ratio programmable in the 1 – 4 range. Two permutations of divide-by-2 and divide-by-3 can be used and both were measured.

Both the phase noise spectra (shown in Fig. 3) and the integrated jitter per decade of frequency offset (summarized in Table 3) indicate that the two stage divider using HMC794LP3E is the best solution for clock frequency synthesis. This solution satisfies the requirements by a substantial margin.

## TESTS AND MEASUREMENTS

5 boards were produced and assembled. All passed the test and the results of measurements were similar, therefore results for only one CS-LOG board (see Fig. 4) are presented. The reference input is visible in the top-left corner. The LO generation (the upper part and the top-right corner) and the clock generation (the lower part and the bottom-right corner) sections are separated to minimize interference.

### Impedance Matching

Impedance matching at a given port was measured with all other ports terminated. At the reference port the input reflectivity at 704 MHz equals -15.785 dB (meeting the

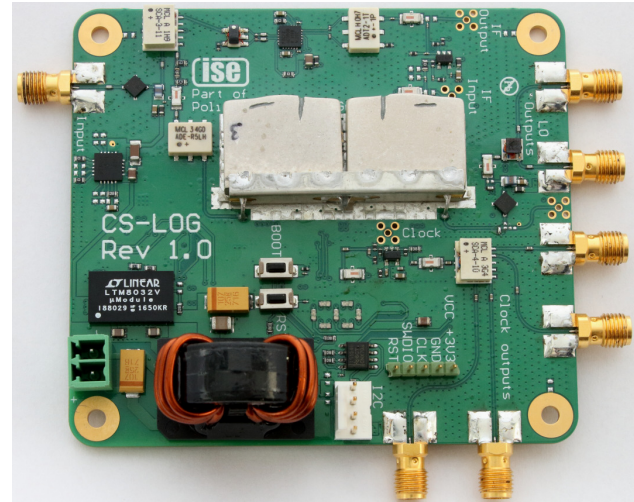


Figure 4: Picture of an assembled CS-LOG board.

requirements) and Table 4 provides clock outputs' reflectivity at 117.4 MHz. The clock ports' matching doesn't meet the requirements and must be improved in future design. The reflectivity at the LO port varies strongly as the function of frequency due to filter's characteristic in the pass-band (see Fig. 5). At output port one the reflectivity equals -15.400 dB for frequency corresponding to division-by-28 LO generation and for division-by-22 equals -13.927 dB. The reflectivity at port two was lower by around 0.5 dB in both divider configurations. The LO ports' matching (besides division-by-22 at port one) meets the requirements with a very small margin and should be improved in future design.

### Phase Noise

The LO signal's phase noise (see Fig. 6) follows the reference signal's phase noise closely up to 100 kHz. There are some minor differences in far-from-carrier phase noise between two signaling standards of the IF divider (AD9508). In divide-by-22 configuration the HSTL 8 mA standard is slightly better, but for division ratio 28 (see Fig. 7) the HSTL Boost is better. The requirements are satisfied by a substantial margin.

The clock signal's phase noise was very similar to measured using evaluation modules and is not presented again.

Table 3: Comparison of the Output Signal's Jitter (Integrated Phase Noise, in fs) per Frequency Offset Decade of Selected Clock Dividers. Division Ratio: 6, Input Frequency: 704.42 MHz.

| Divider ↓ | Start Offset (Hz)   | 10    | 100   | 1k    | 10k   | 100 k | 1M    | 10    | 1k    |
|-----------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|
|           | End Offset (Hz)     | 100   | 1k    | 10k   | 100 k | 1M    | 10 M  | 10 M  | 10 M  |
| AD9508    | HSTL 8mA            | 27.47 | 29.95 | 36.68 | 26.79 | 18.99 | 44.50 | 77.84 | 66.36 |
| AD9515    | LVPECL 790 mV       | 13.68 | 9.39  | 8.88  | 12.18 | 26.44 | 72.87 | 80.70 | 78.97 |
| HMC794    | 1st stage: div-by-3 | 15.07 | 13.38 | 12.89 | 14.07 | 20.49 | 47.78 | 58.95 | 55.38 |
|           | 1st stage: div-by-2 | 11.44 | 6.79  | 6.86  | 6.38  | 10.45 | 28.03 | 34.09 | 31.35 |

Table 4: Clock Ports' Reflectivity at 117.4 MHz

|           |            |
|-----------|------------|
| Channel 1 | -11.772 dB |
| Channel 2 | -11.650 dB |
| Channel 3 | -11.836 dB |
| Channel 4 | -11.786 dB |

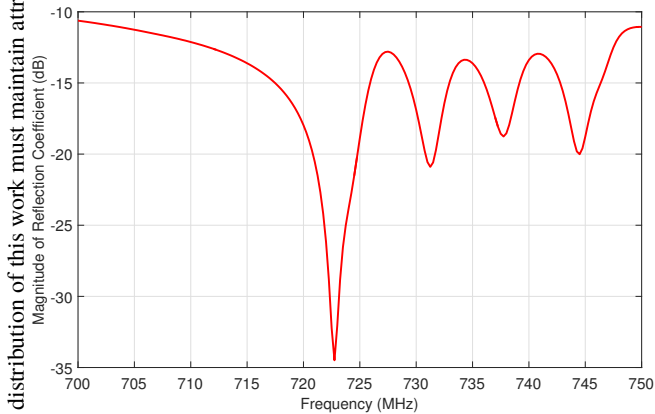


Figure 5: Magnitude of reflection coefficient measured at the LO output port one.

## CONCLUSION

The requirements, architecture, and measurements results of the LO generation board prototype were presented. The CS-LOG meets phase noise requirements, but at some ports the impedance matching must be improved in future revision.

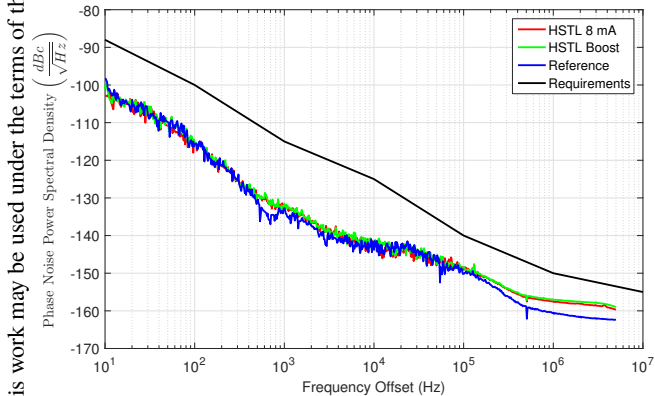


Figure 6: Phase noise spectra of the LO signal for two signaling standards and an ideally converted reference signal. Division ratio: 22, input frequency: 704.42 MHz.

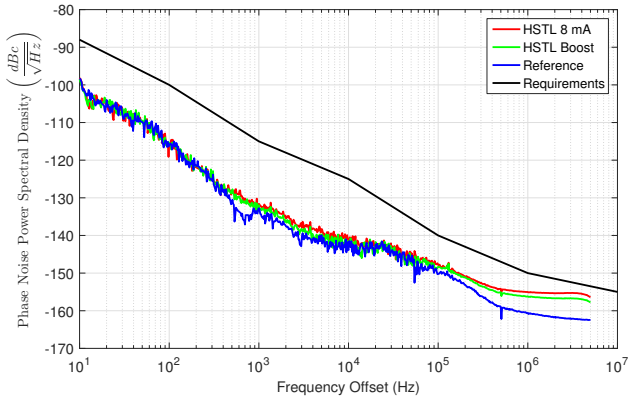


Figure 7: Phase noise spectra of the LO signal for two signaling standards and an ideally converted reference signal. Division ratio: 28, input frequency: 704.42 MHz.

The design of LO RTM can be based on the prototype without any major changes.

## REFERENCES

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