

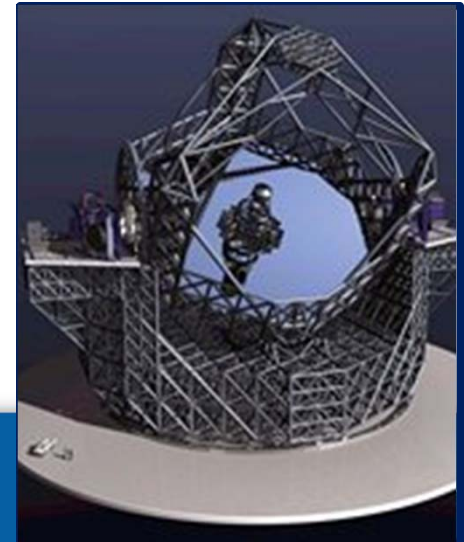


Customized Off-The-Shelf Technologies Through Industry – Research Facility Partnership

Dr. James Truchard
President, CEO & Cofounder
National Instruments

Today's Engineering Challenges

- Doing more with less
- Time to experiment
- Managing global projects
- Adapting to evolving application requirements
- Delivering on increasingly complex initiatives
- Maximizing operational efficiency
- Protecting system and resource investments



Transition to Customized COTS

Vacuum Tube



General
Radio

1920

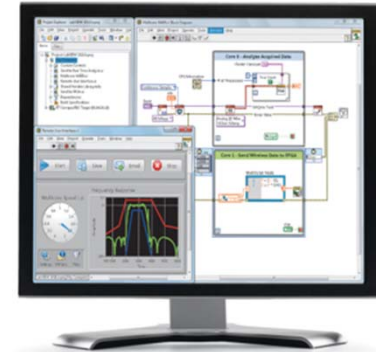
Transistor
(Integrated Circuit)



Hewlett
Packard

1965

Software

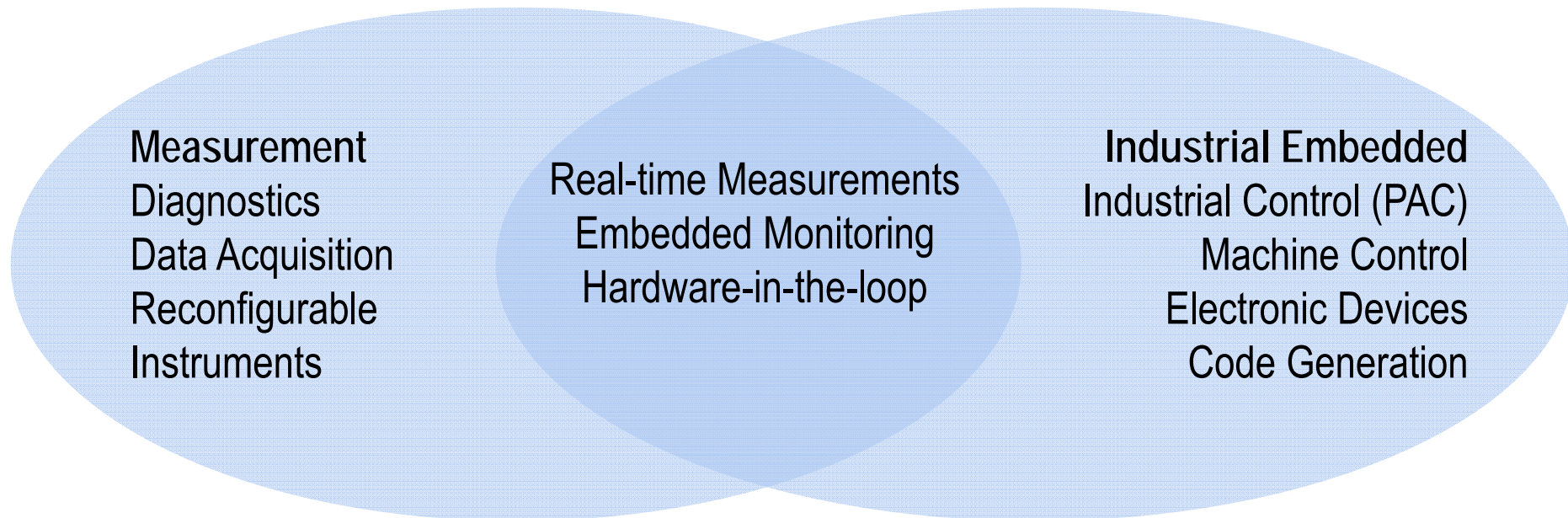


National
Instruments

2010

The National Instruments Vision, Evolved...

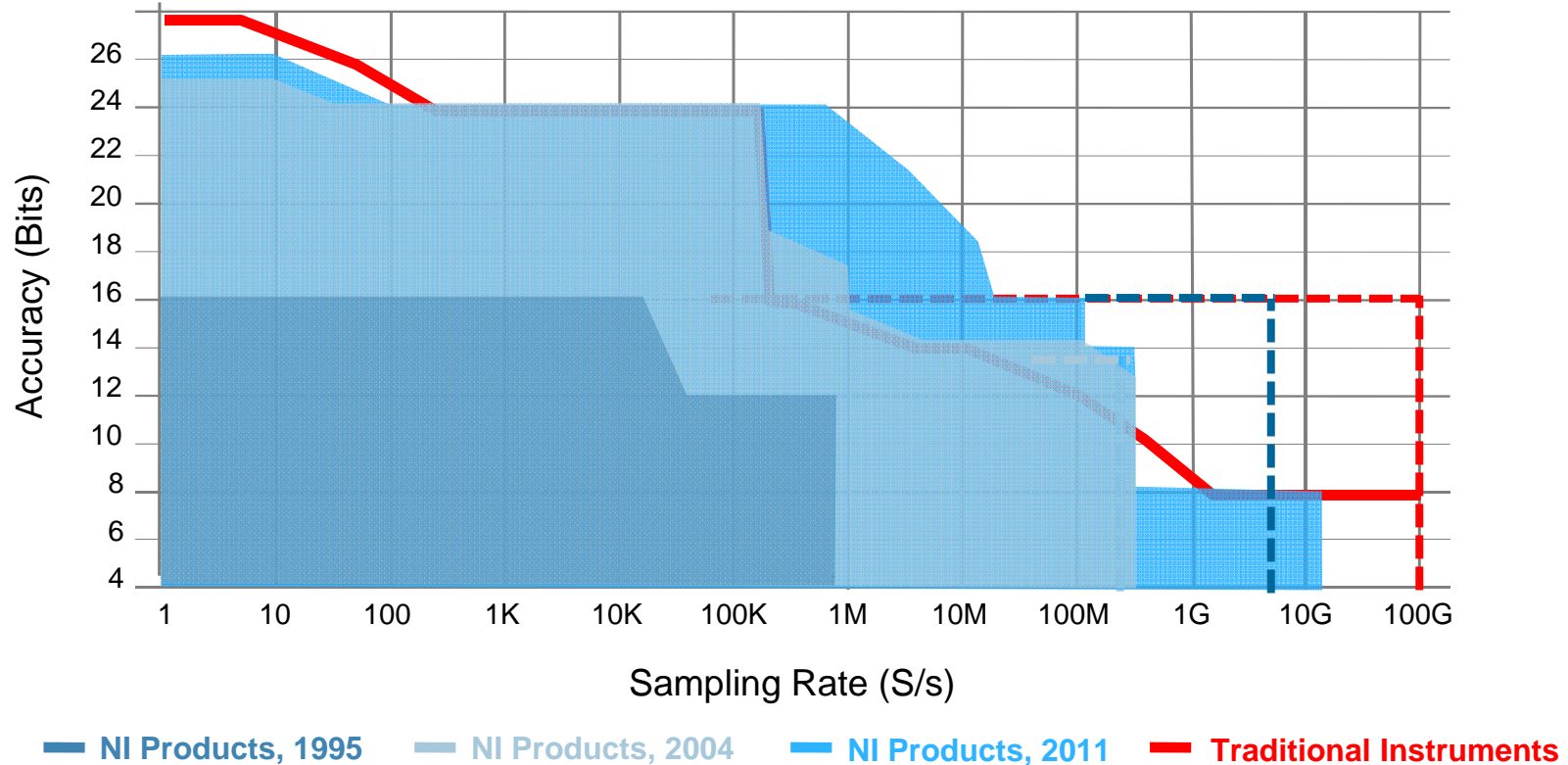
Graphical System Design



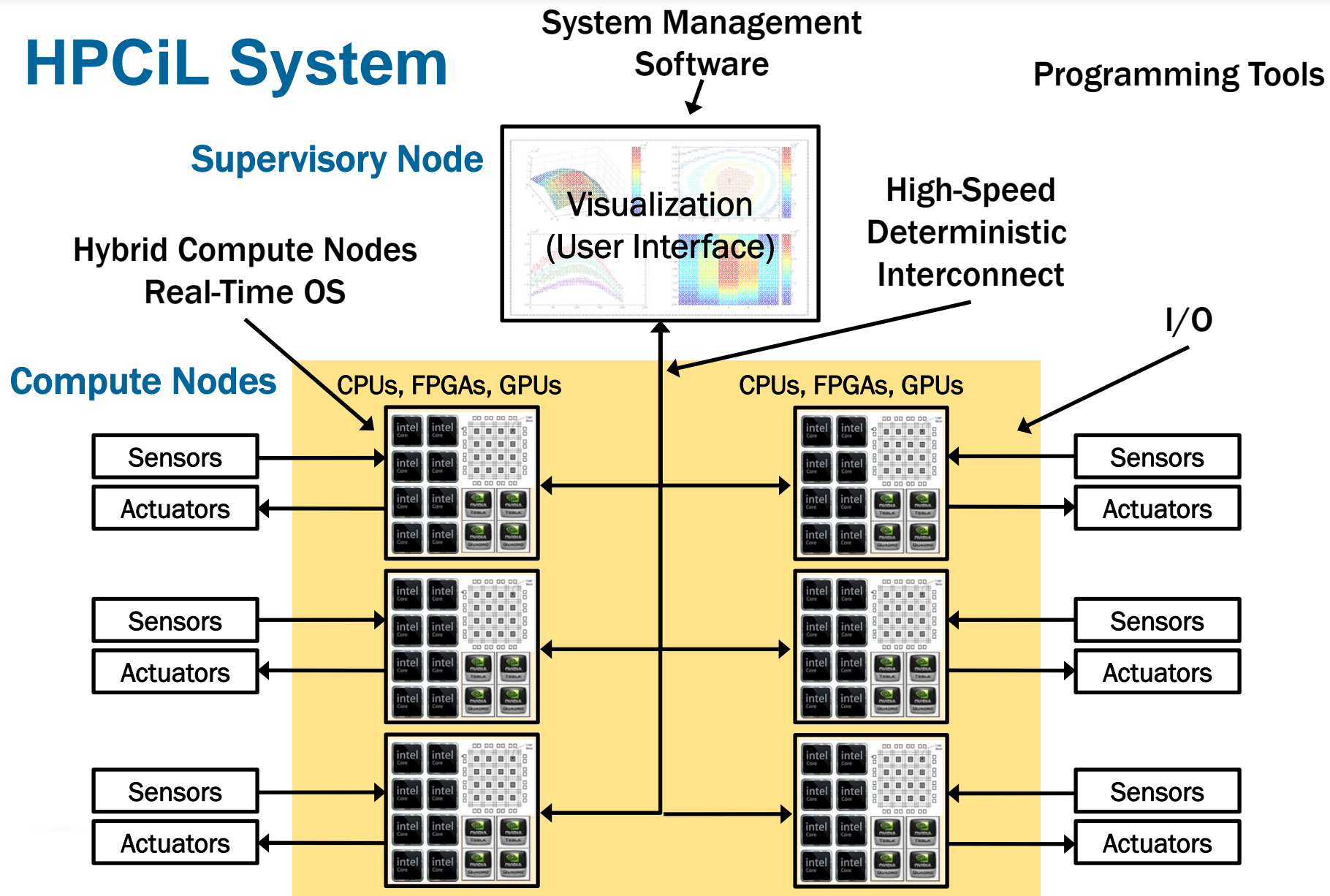
“To do for test and measurement
what the spreadsheet did
for financial analysis.”

“To do for embedded what the PC
did for the desktop.”

Expanding Measurement Capabilities



HPCiL System



Partnership with Industry

Continuous innovation

- Leverage R&D investment and latest technology
- Tools and platforms that allow faster iteration

Simplification and cost reduction

- Empower domain experts
- Open platforms to adapt vertical and emerging standards

Long term maintenance and support

- Life cycle management
- Services and consulting

Partnership with Industry

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Long term maintenance and support

- Life cycle management
- Services and consulting

National Instruments

Corporate headquarters: *Austin, Texas*

Year established: *1976*

Revenue: \$873 million in 2010

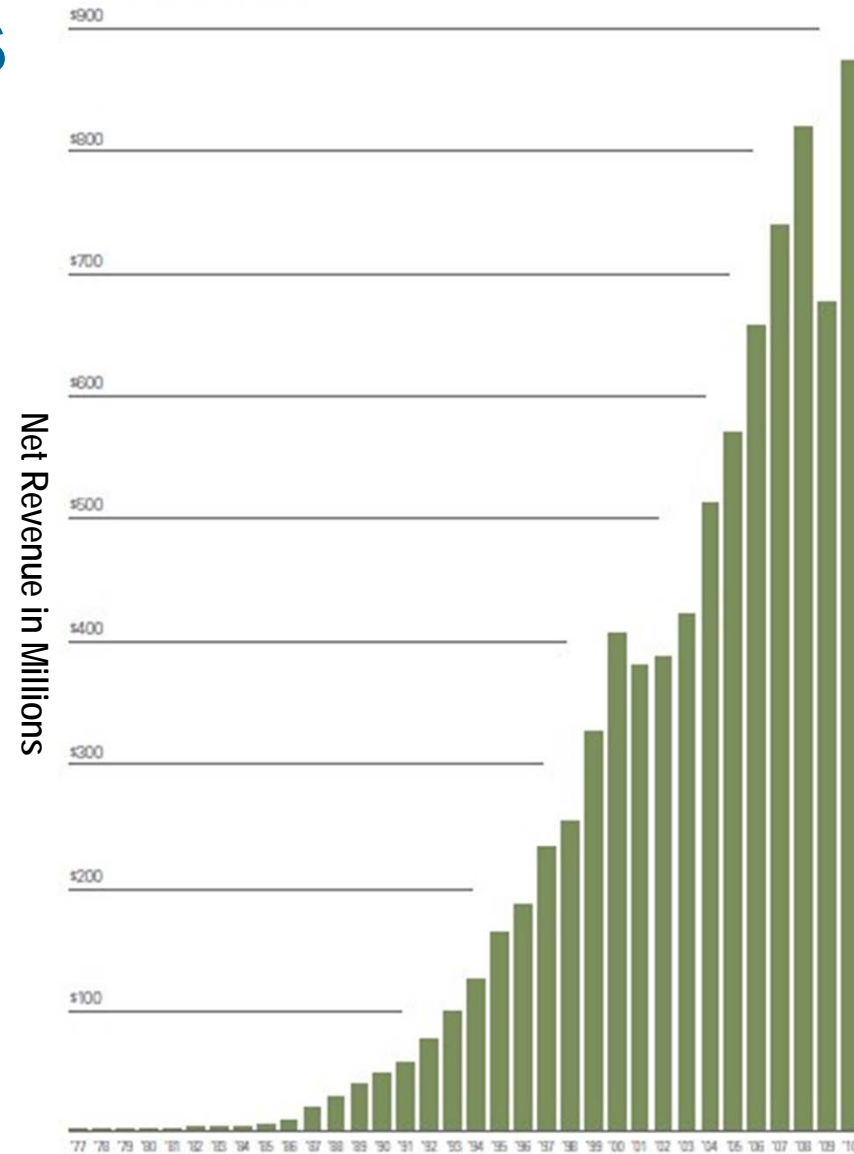
Global operations: *offices in 43 countries*

Investment in R&D: *16% of annual revenue*

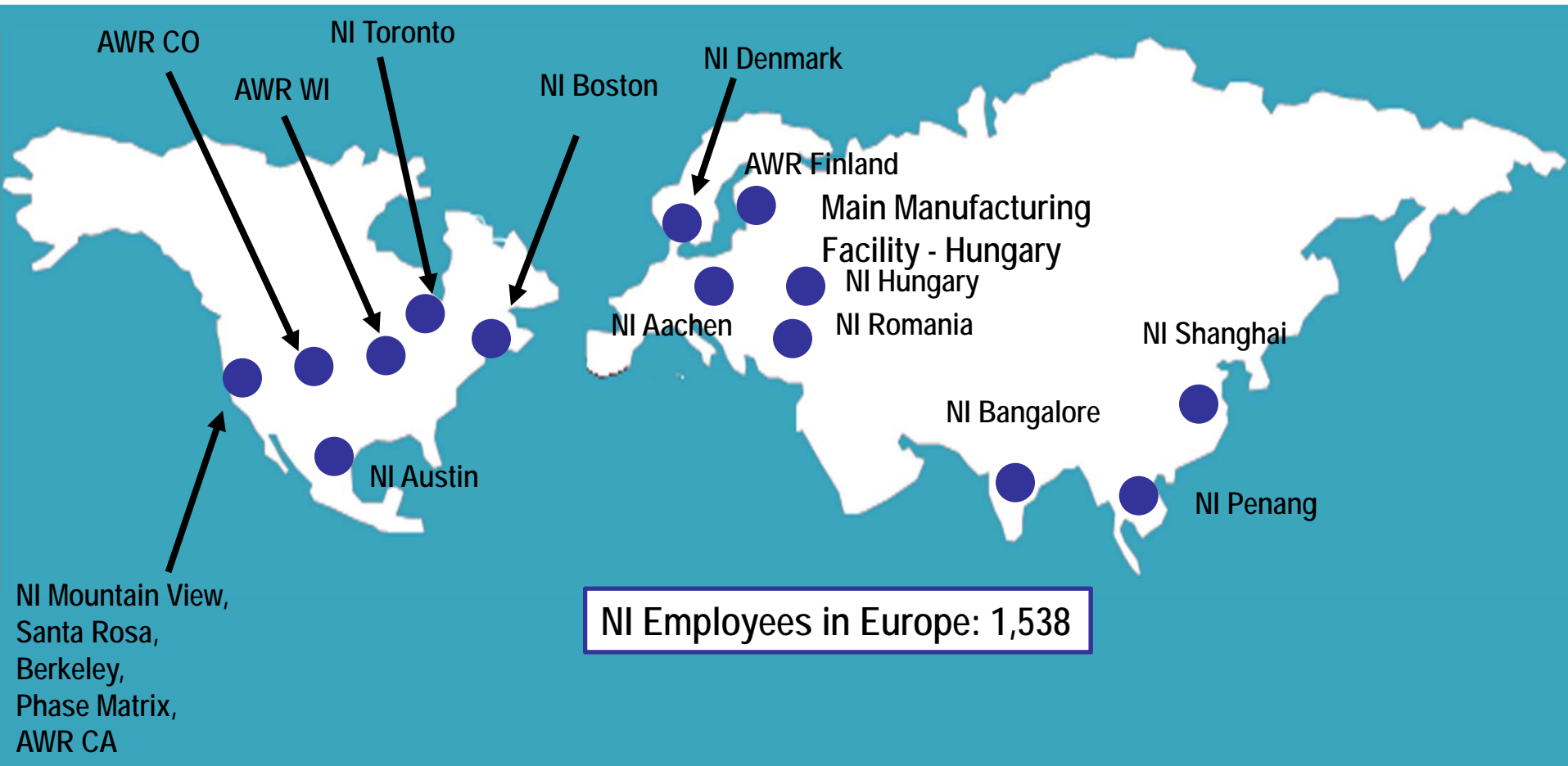
Customer base: *30,000 companies annually*

Network: More than 600 Alliance Partners

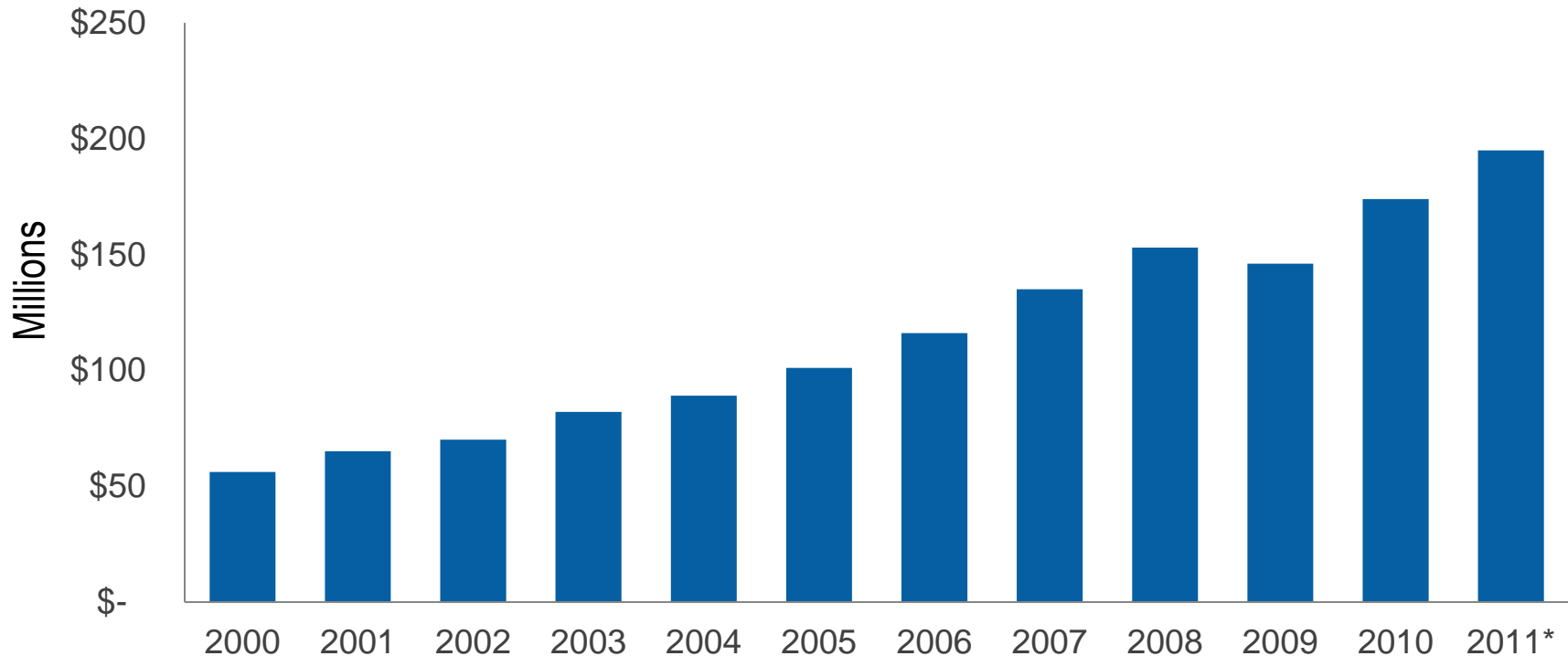
Diversity: *no industry makes up more than
15% of revenue*



NI Global R&D Organizations



NI's Increasing Investment in R&D



*Represents National Instruments expected investment, communicated June 28, 2011.

Leveraging Industry Relationships

- Apply technologies from wide array of vendors
 - Next generation FPGAs, ADCs, GPUs and processors
- High access to information
 - Regular executive meetings
 - Ability to influence roadmaps



Adapting To Changing Needs



iPhone 3



2 years



iPhone 4



Dell Latitude 5200



3 years



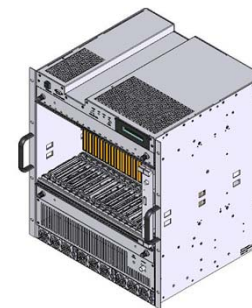
Dell Latitude 6400



Custom Design



10 years



Custom Design

Keep Up With Technology While Preserving Investment



iPhone 3



2 years



iPhone 4



Dell Latitude 5200



3 years



Dell Latitude 6400



COTS Platforms



3 Years



COTS Platforms

Leveraging R&D Investment

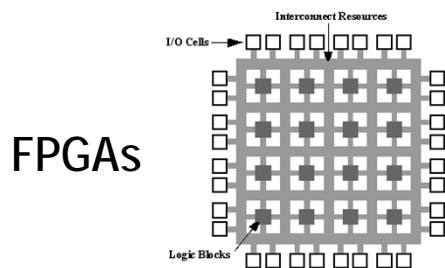
Investment from Industry in 2010

- > \$170M from NI (1800 man years)
- >1,600M from Intel
- >\$500M from Analog Devices

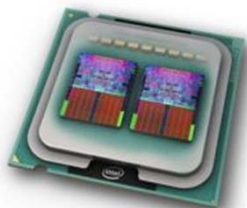
Combining Laboratory Expertise and off-the-shelf technology

- Custom Front End
- Signal Conditioning
- Algorithm

Tools From the Industry



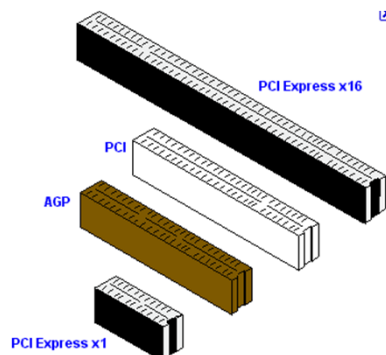
Multicore Processors



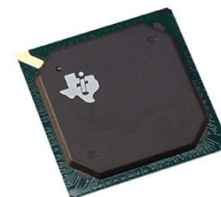
GPUs



Processors



Communication Bus



ADC/DAC

Putting it together.....



Embedded Controller
(Processor)



Chassis with T&S
(Communication Bus)

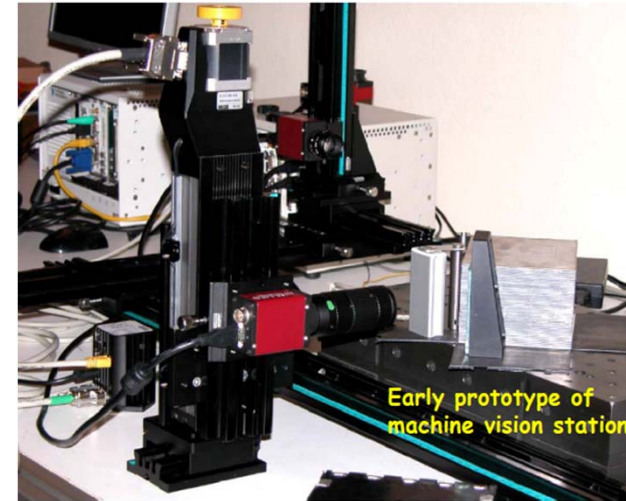


I/O Modules
(ADC/DAC)

INFN Gran Sasso – CERN

OPERA Detector for Neutrino Events

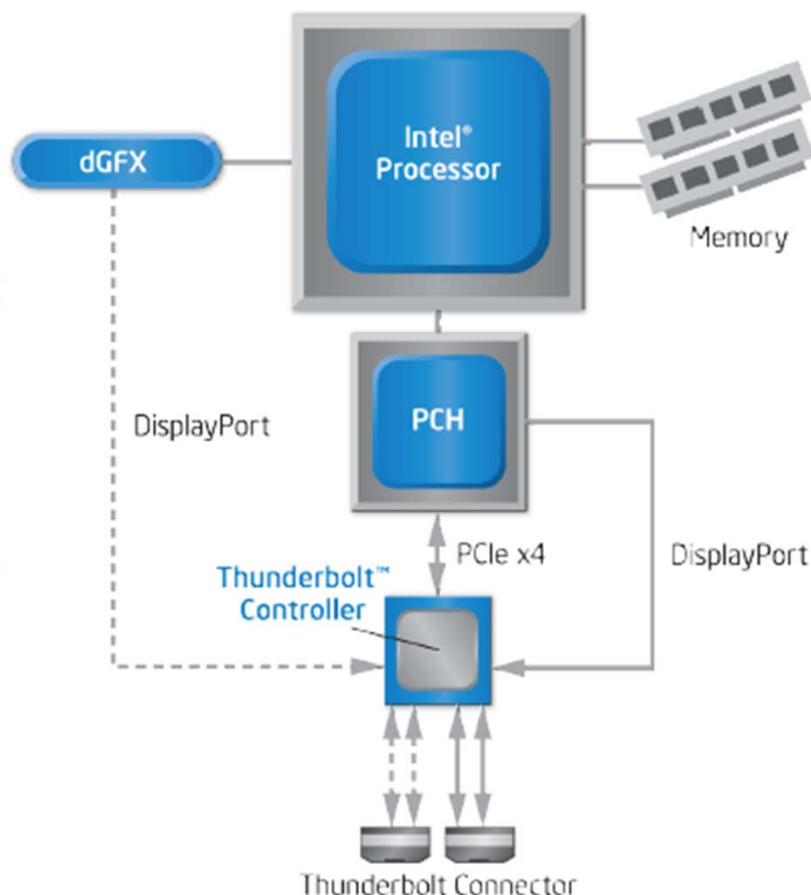
- Brick Assembly Machine for the hybrid detector
 - Machine Vision System
 - Dimensional measurements
- NI platforms provide hardware and software
 - LabVIEW programming environment
 - IMAQ Vision Libraries



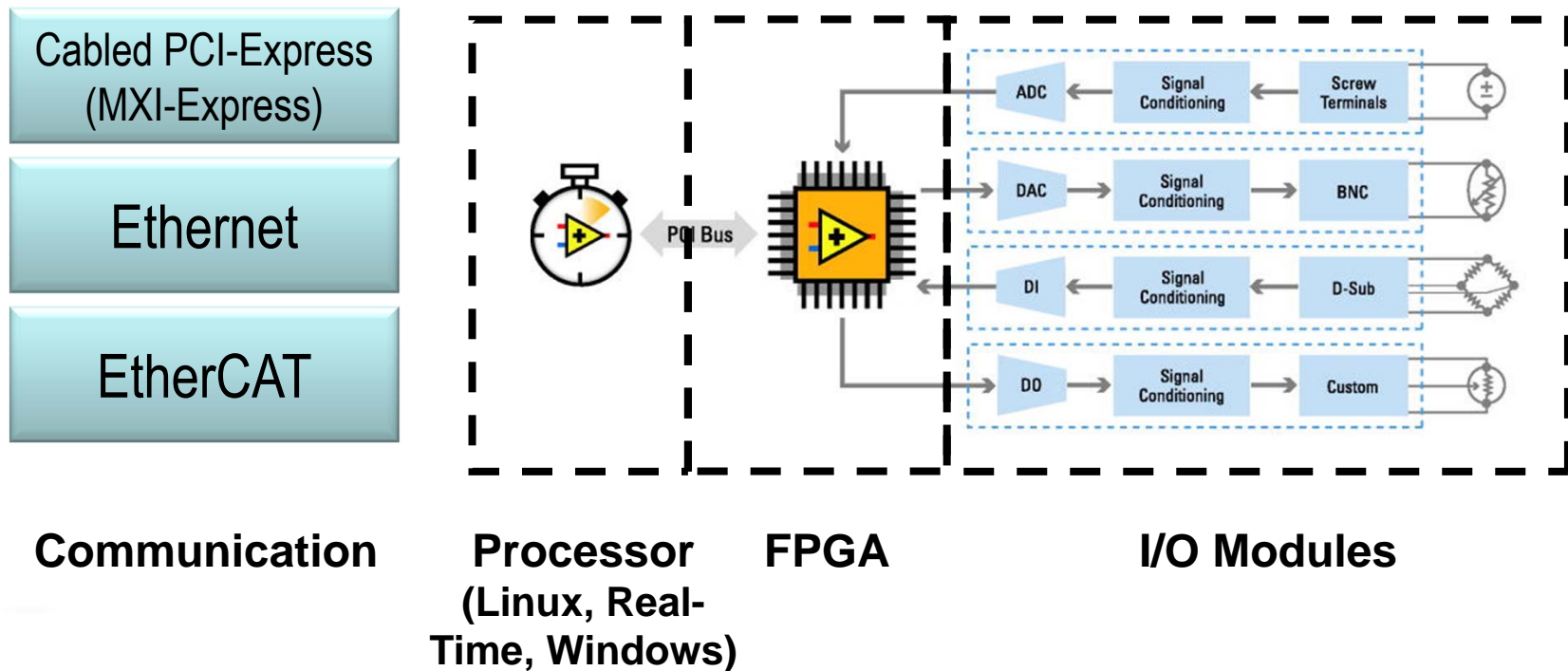
Technology Architecture

- 10Gbps per channel, bidirectional performance
 - 2 channels per cable
- Native PCIe* and DisplayPort* protocols
 - Uses native PCIe and DP drivers
- Compatible with standard DisplayPort
 - Thunderbolt™ ports can operate in native DP mode
- Small connector with cable options
 - Active electrical cable (up to 3m) w/ 10W power, or can be extended with...
 - Active optical cable (up to tens of meters)
- Daisy chain topologies
 - 6 Thunderbolt devices and 1 native DisplayPort display

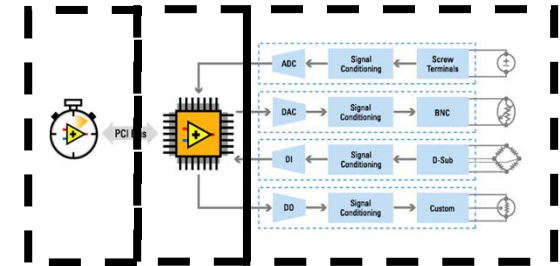
Example PC System Diagram
Other system configurations possible



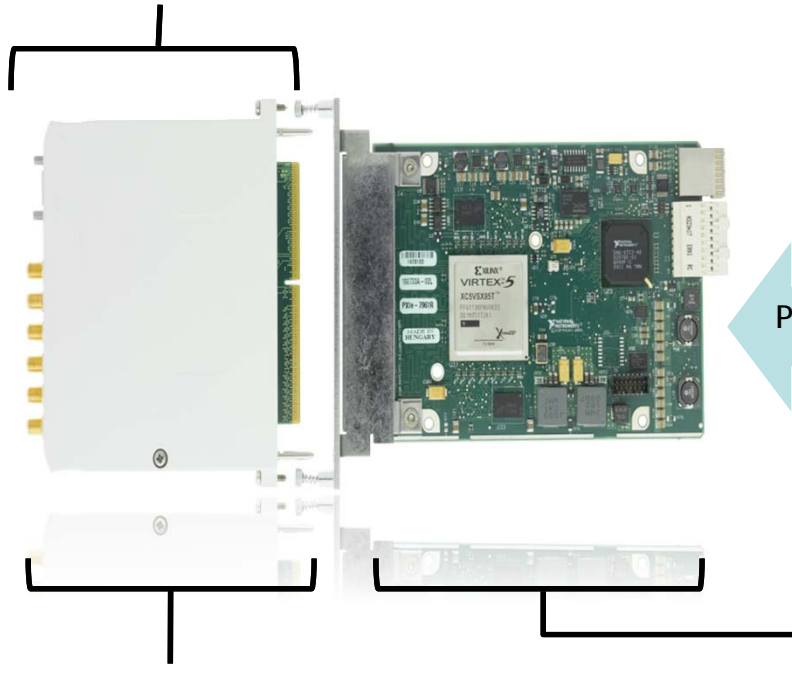
Combining COTS With Your Design: *RIO Architecture*



FlexRIO Architecture



Customizable
Front-End

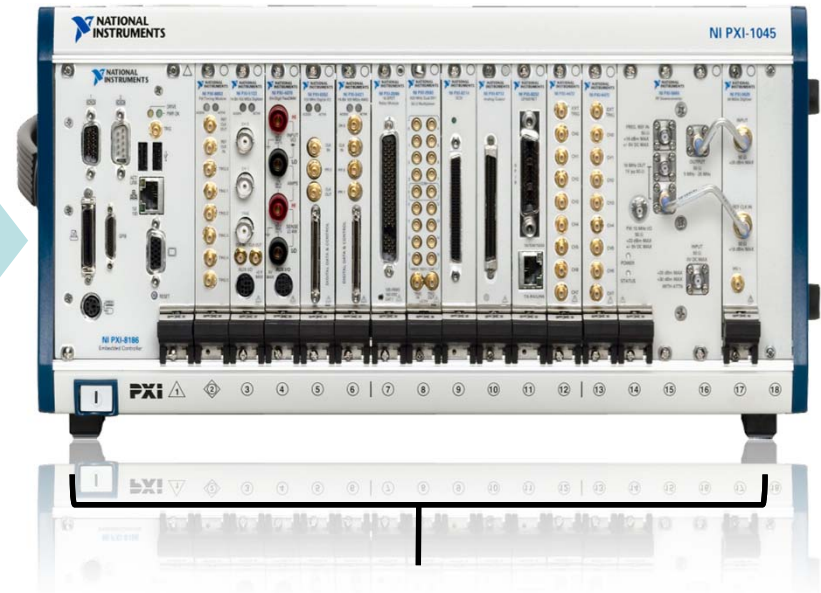


NI FlexRIO Adapter Module

- Interchangeable I/O
- Digital or analog
- NI FlexRIO Adapter Module Development Kit (MDK)

NI FlexRIO FPGA Module

- Virtex-5 FPGA
- 132 digital I/O lines
- Up to 512 MB of DRAM
- Peer-to-peer data streaming



PXIe Platform

- Data transfer
- Synchronization
- Clocking/triggers
- Power/cooling

Released FlexRIO Adapter Modules

Digital



100 MHz SE
DIO



200 MHz
LVDS DIO



200 MHz
SE/LVDS DIO



Camera Link



RS-485/422

Analog



2 ch. 100 MS/s
AI/AO



32 ch. 50 MS/s
AI

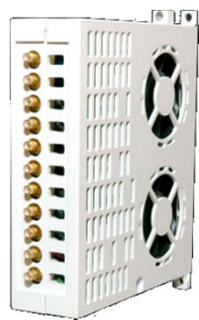


4 ch. 250 MS/s
AI



16 ch. 50 MS/s
AI

Custom FlexRIO Modules



100 MHz
PPMU



Camera Link
and GigE



Multi-gigabit
optical



Dual gigabit
Ethernet



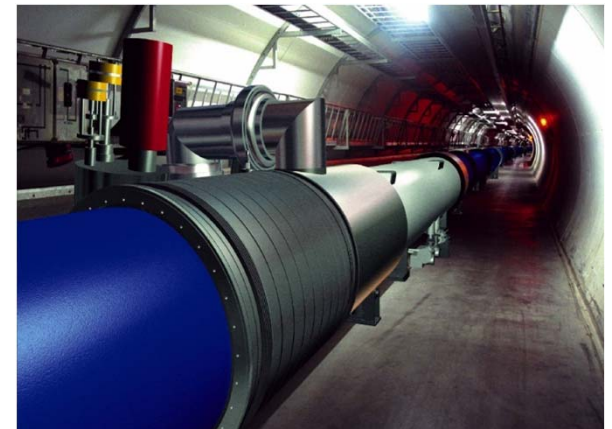
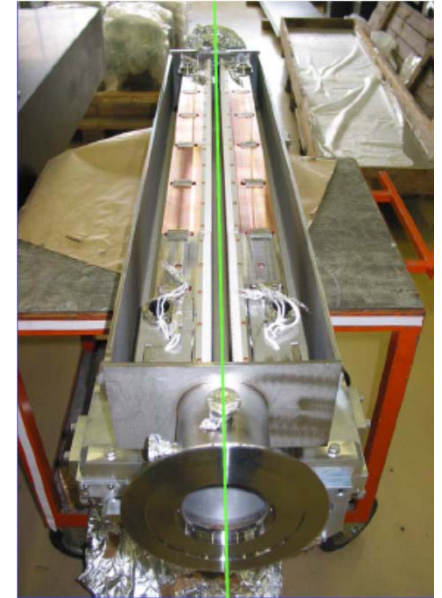
Video and
Automotive



Time to Digital
Converter

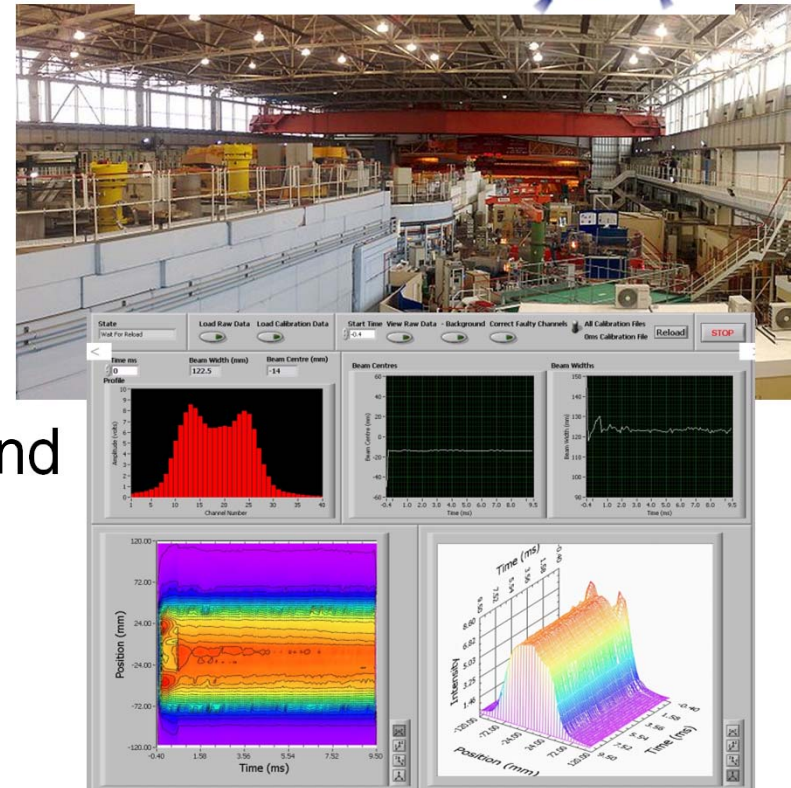
Example - CERN Collimator Alignment

- 550+ axes of motion
- Across 27 km distance
- The jaws have to be positioned with an accuracy which is a fraction of the beam size ($200\mu\text{m}$)
- Synchronized to
 - $< 5\text{ms}$ drift over 15 minutes
 - Maximum jitter in μs

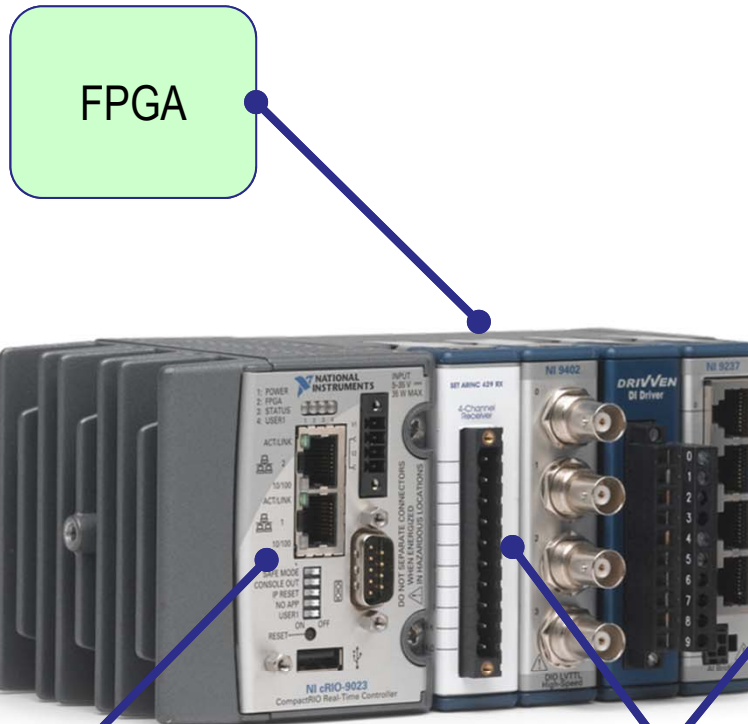
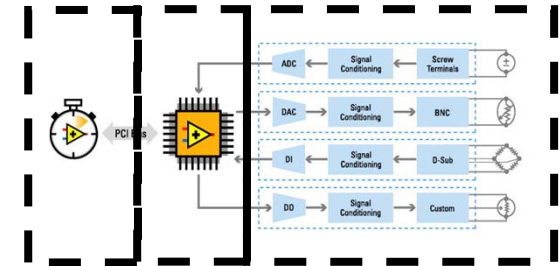


ISIS Synchrotron, Rutherford Appleton Labs

- Beam data acquisition and analysis
 - Beam loss monitoring
 - Beam position monitoring
 - Multichannel profile monitoring
- Hardware based on PXI platform
 - High speed digitizers
 - Timing and synchronization
- LabVIEW based control system and process display data



CompactRIO Architecture



FPGA

Host
Processin
g
Real-Time

Varied Modular
I/O for any signal

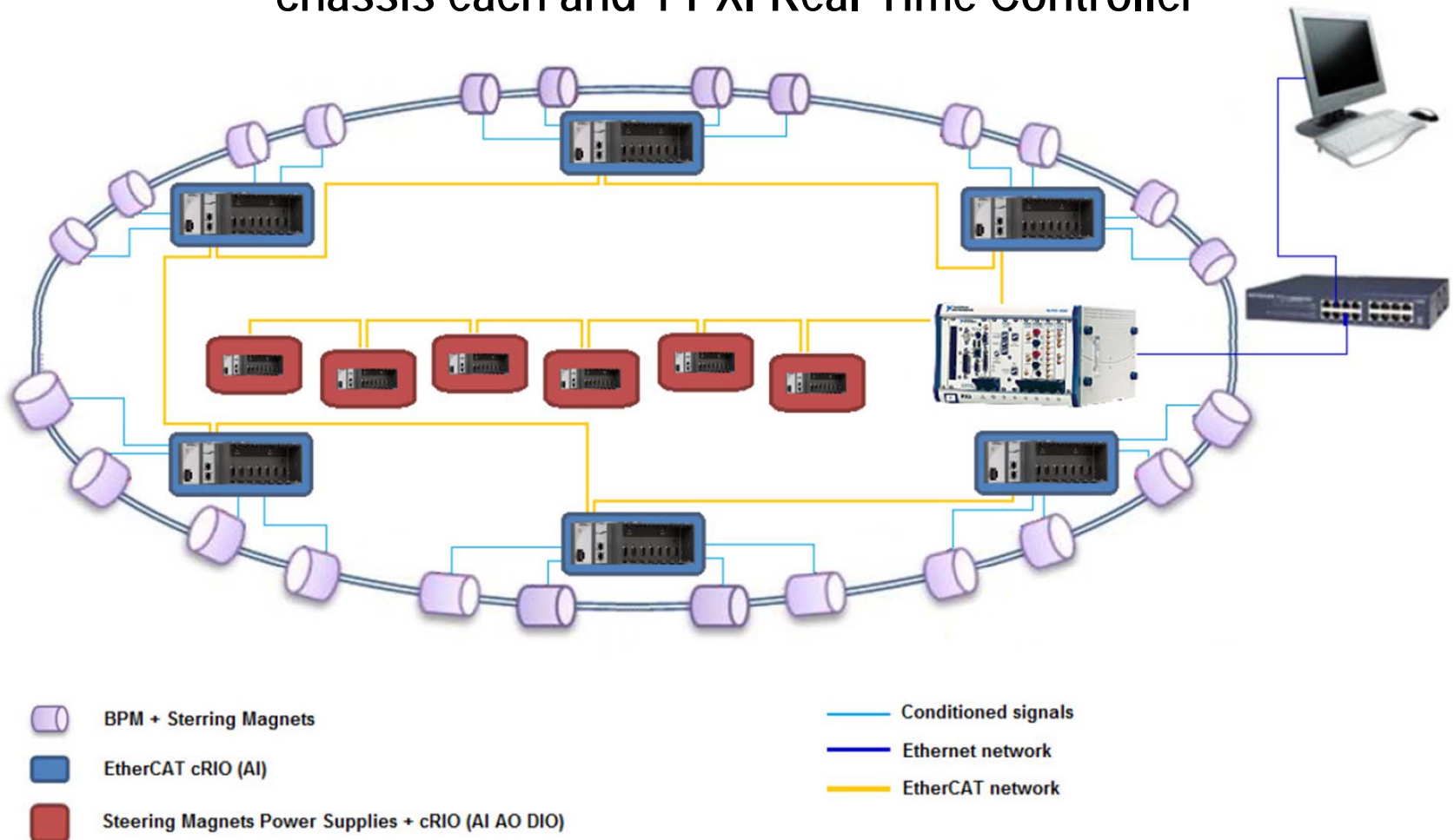


LNLS – Brazilian Synchrotron

Fast Orbit Feedback Control System

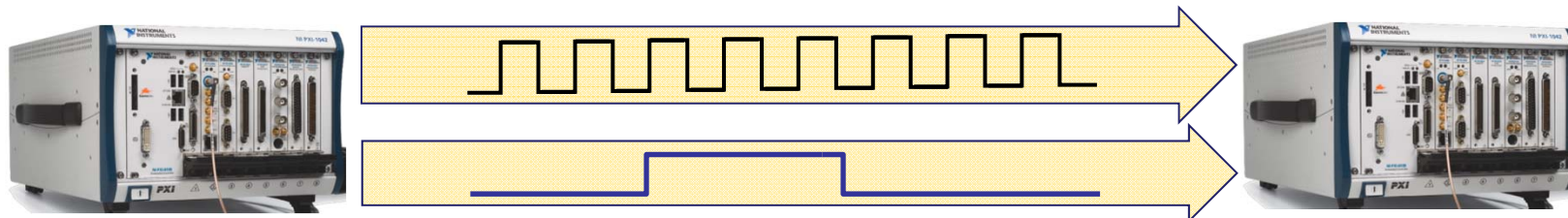


New orbit control system topology: 2 EtherCAT loops with 6 cRIO chassis each and 1 PXI Real-Time Controller



Signal vs. Time-Based Synchronization

Signal-Based



Share Physical Clocks / Triggers

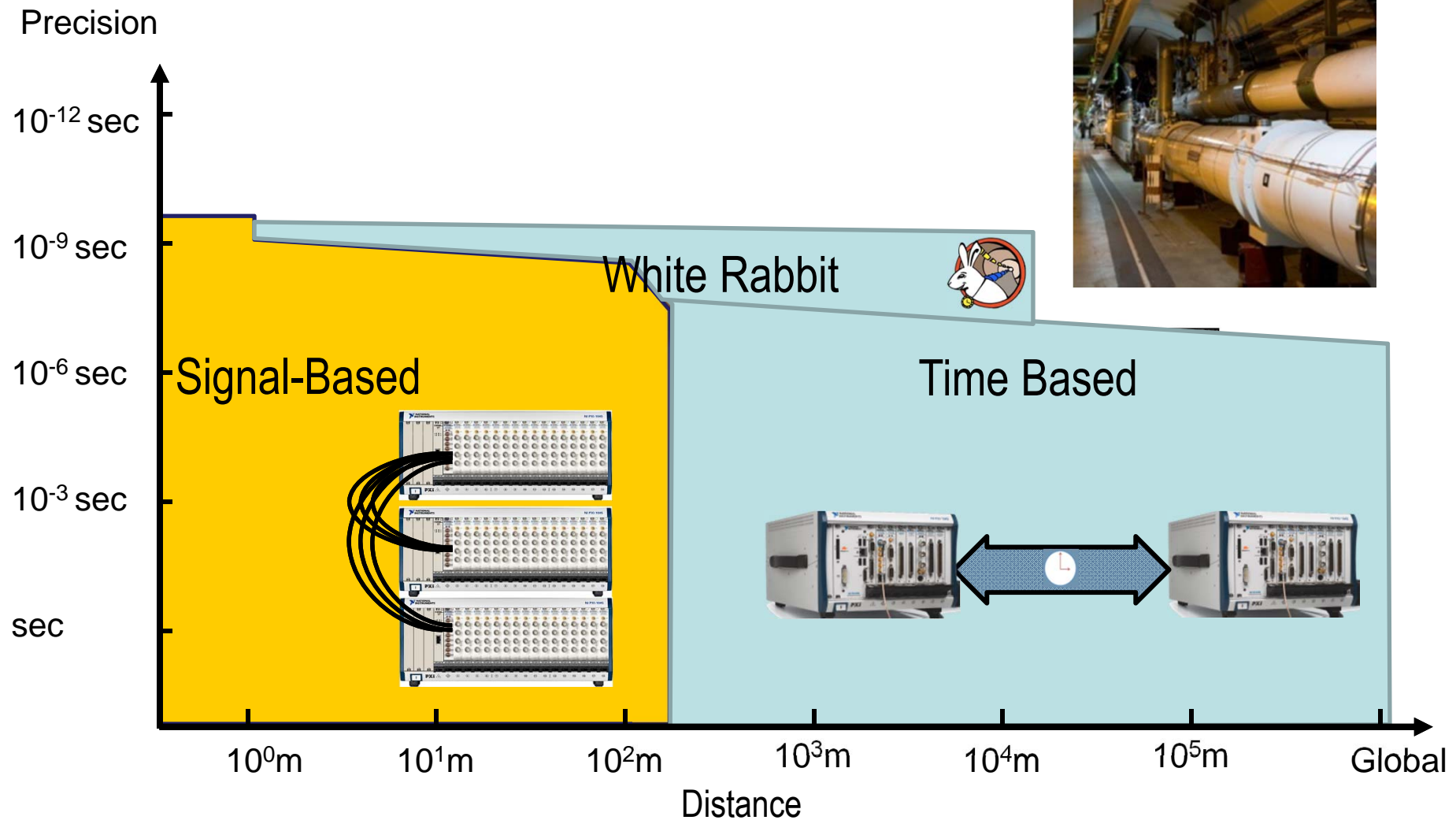
Time-Based



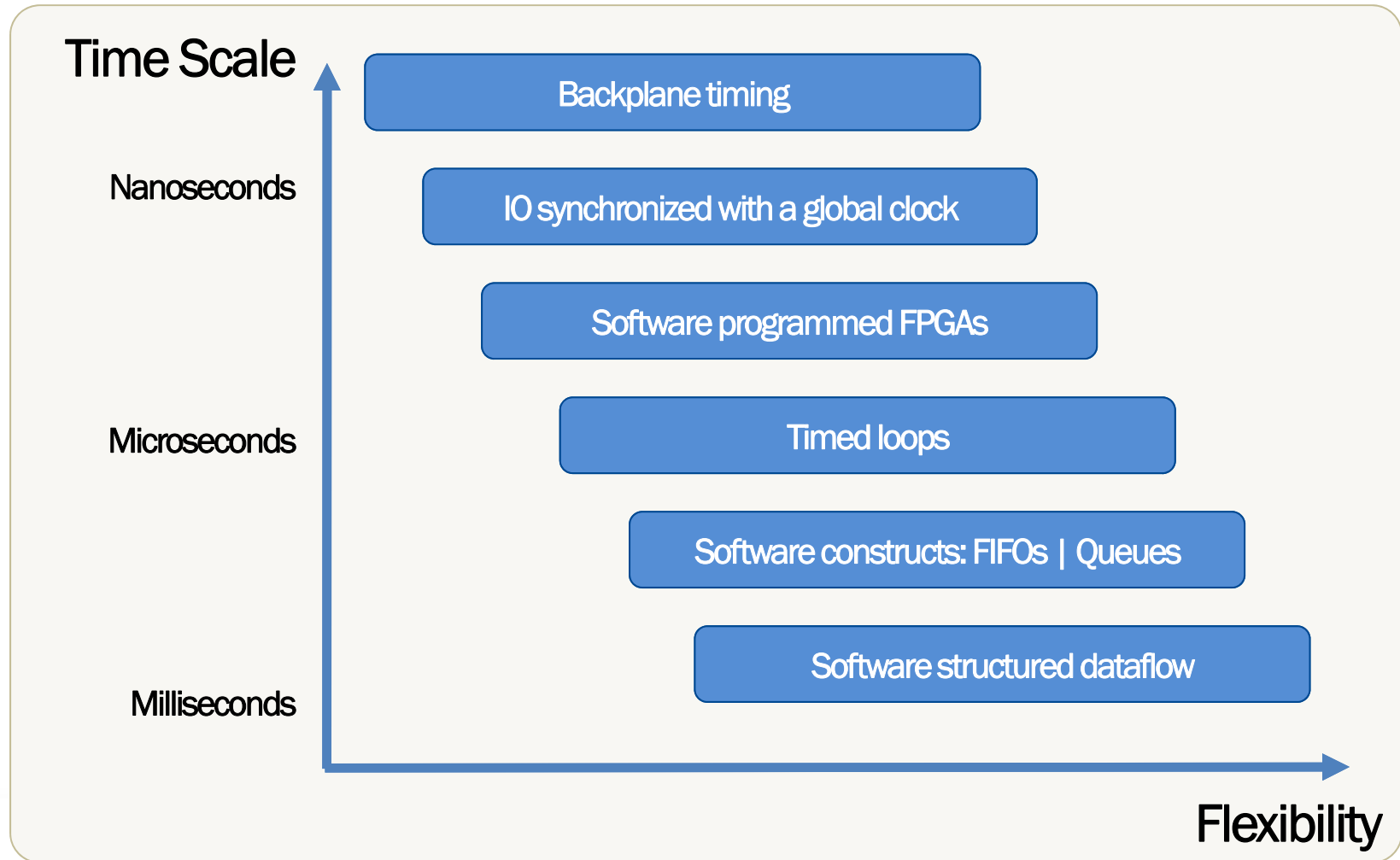
Share Time
Ethernet (1588)
IRIG
GPS
Etc.



White Rabbit: Synchronization over Distance



Technologies for Time and Concurrency

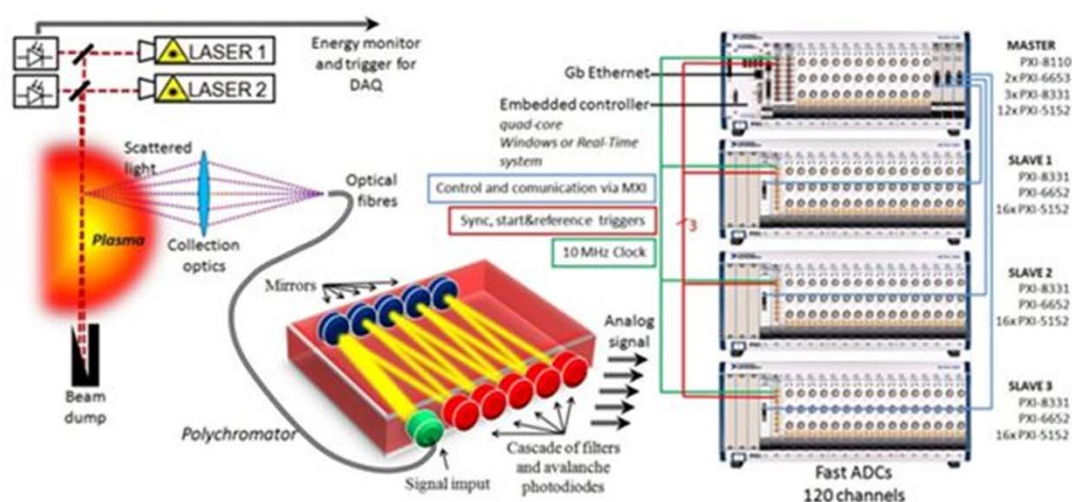


Cooperation: NI and CERN White Rabbit

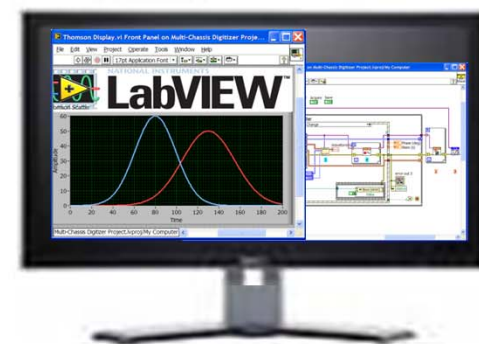


- Partnering with CERN in developing White Rabbit (WR)
- Performance
 - **Distance:** > 10 km
 - **Scale:** > 2000 nodes
 - **Accuracy:** < 1ns skew, < 100 ps jitter
 - Compensates for propagation delay (cable length, temperature variation, etc.)
- Leverage Industry standards (802.x, **IEEE 1588**, SyncE)
 - Gigabit Ethernet communication with deterministic capability
- Generally Applicable
- Leverage for future PXle modules





- Thomson scattering system
- Synchronized high speed data acquisition
 - 120 channels running at 1GS/s
 - Tight synchronization over 4 PXI chassis
 - Skew < 500 ps



Partnership with Industry

Continuous innovation

- Leverage R&D investment and latest technology
- Tools and platforms that allow faster iteration

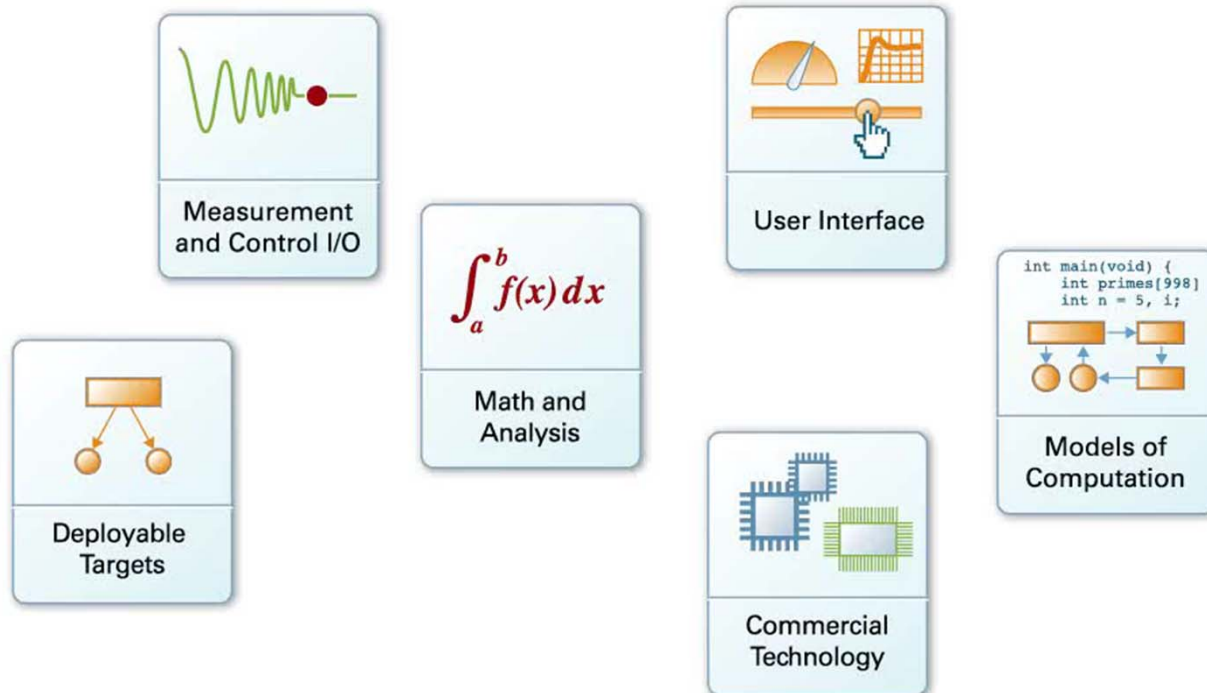
Simplification and cost reduction

- Empower domain experts
- Open platforms to adapt vertical and emerging standards

Long term maintenance and support

- Life cycle management
- Services and consulting

Integrating Elements of Graphical System Design



Graphical System Design

Software

COMMUNITY

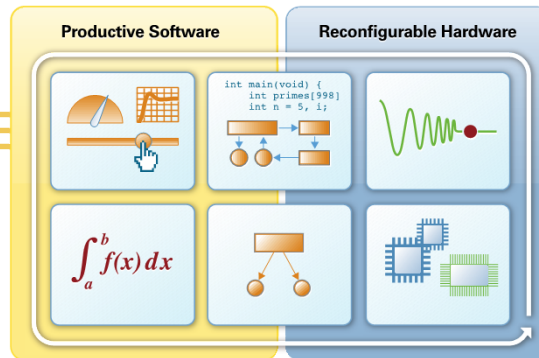
140,000+ online members
250+ registered user groups
1000+ job postings online
400K+ children through LEGO

CONNECTIVITY

9000+ instrument drivers
8000+ example programs
1000+ motion drives
1000+ smart sensors
1000+ Third-party PAC devices

COLLABORATION

280+ third-party add-ons
400+ Solution partners
1000+ value added resellers
35+ training courses



Hardware

PROCESSOR

Intel, Microsoft, Freescale, Wind River
Multi-core and real-time technology

FPGA

Xilinx Virtex & Spartan
Reconfigurable hardware

IP

Control & signal processing IP & I/O drivers
Built-in graphical IP, integrate user IP

I/O

Analog Devices, Texas Instruments
Connect to any sensor & actuator

BUS

PCI/PCIe, Enet, USB, wireless,
deterministic Enet, Open architecture

A WORLD-CLASS TECHNOLOGY ECOSYSTEM

Graphical System Design

A Platform-Based Approach

Test



Monitor



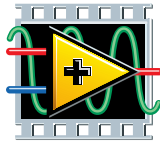
Embedded



Control



Cyber Physical



NATIONAL INSTRUMENTS
LabVIEW™



Desktops and
PC-Based DAQ

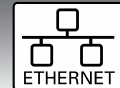


PXI and Modular
Instruments



RIO and Custom
Designs

GPB
IEEE-488

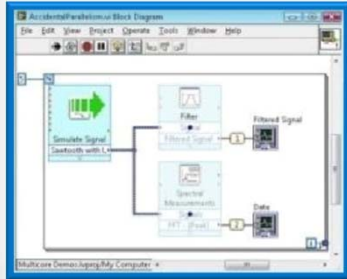


HI-SPEED
CERTIFIED **USB**

Open Connectivity
with 3rd Party I/O

High-Level Design Models

Data Flow



C Code

```

#include "stdint.h"
#include "stdio.h"
#include "stdlib.h"
#include "string.h"
#include "math.h"

// Global variables
int *A;
int *B;
int *C;
int *D;
int *k;

// Function prototypes
void init_arrays(int n);
void calculate_C(int n);
void calculate_D(int n);

// Main function
int main(int argc, char *argv[])
{
    // Initialize arrays
    init_arrays(1000);

    // Calculate C = A * B
    calculate_C(1000);

    // Calculate D = k * A
    calculate_D(1000);

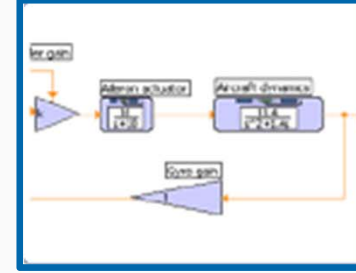
    return 0;
}
    
```

Textual Math

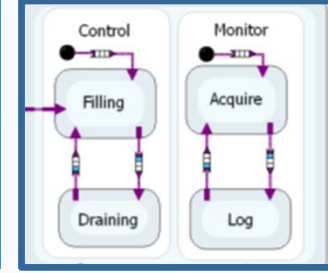
```

1  A = [1 3; 4 2];
2  B = [6 7; 2 3];
3  C = A*B;
4  eigC = eig(C);
5  D = k*A
    
```

Simulation



Statechart



NATIONAL INSTRUMENTS

LabVIEW™

Graphical System Design Platform



PC/Mac/Linux



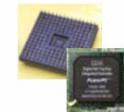
PXI



CompactRIO



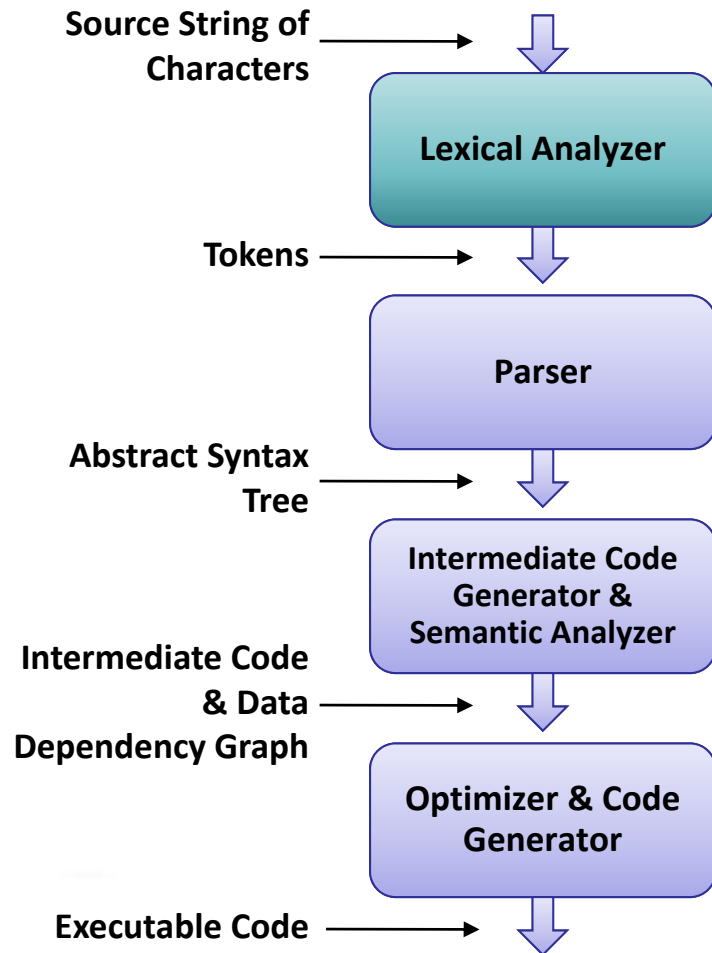
FlexRIO



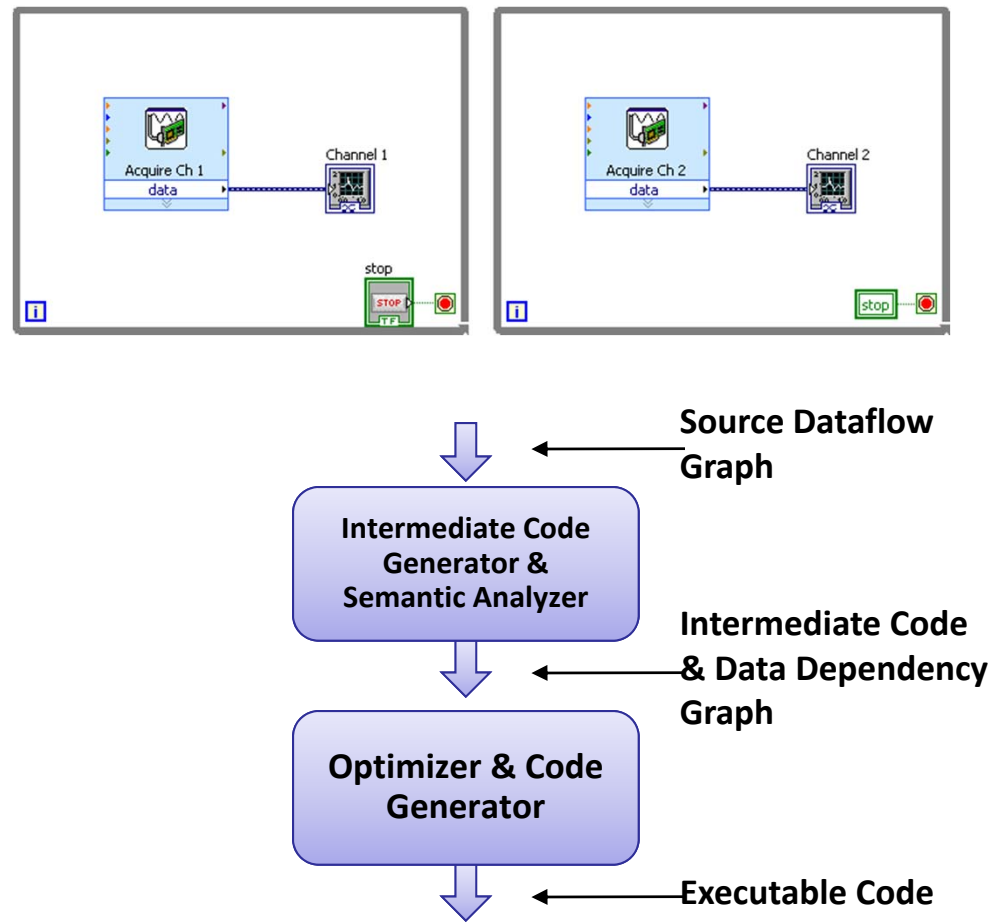
Custom

Eliminating Artificial Complexity

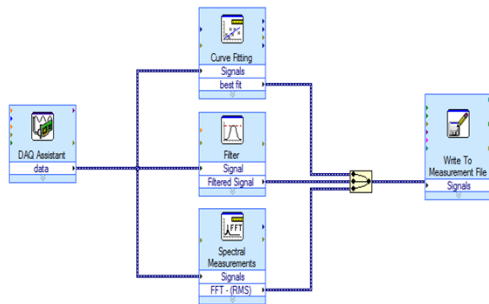
Text-based Compiler



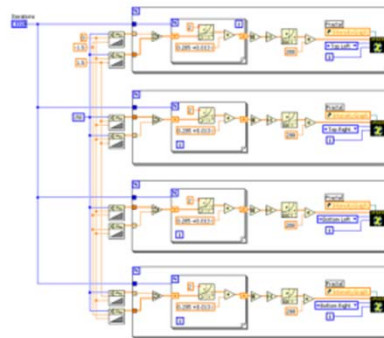
LabVIEW Compiler



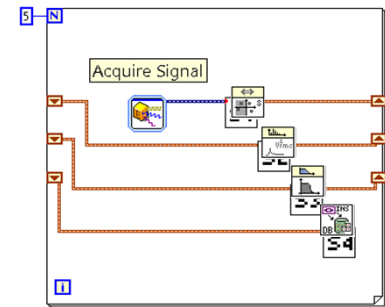
Parallel Programming with LabVIEW



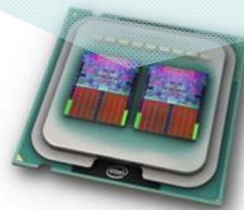
Task Parallelism



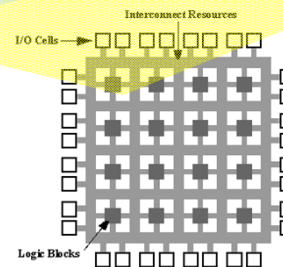
Data Parallelism



Pipelining

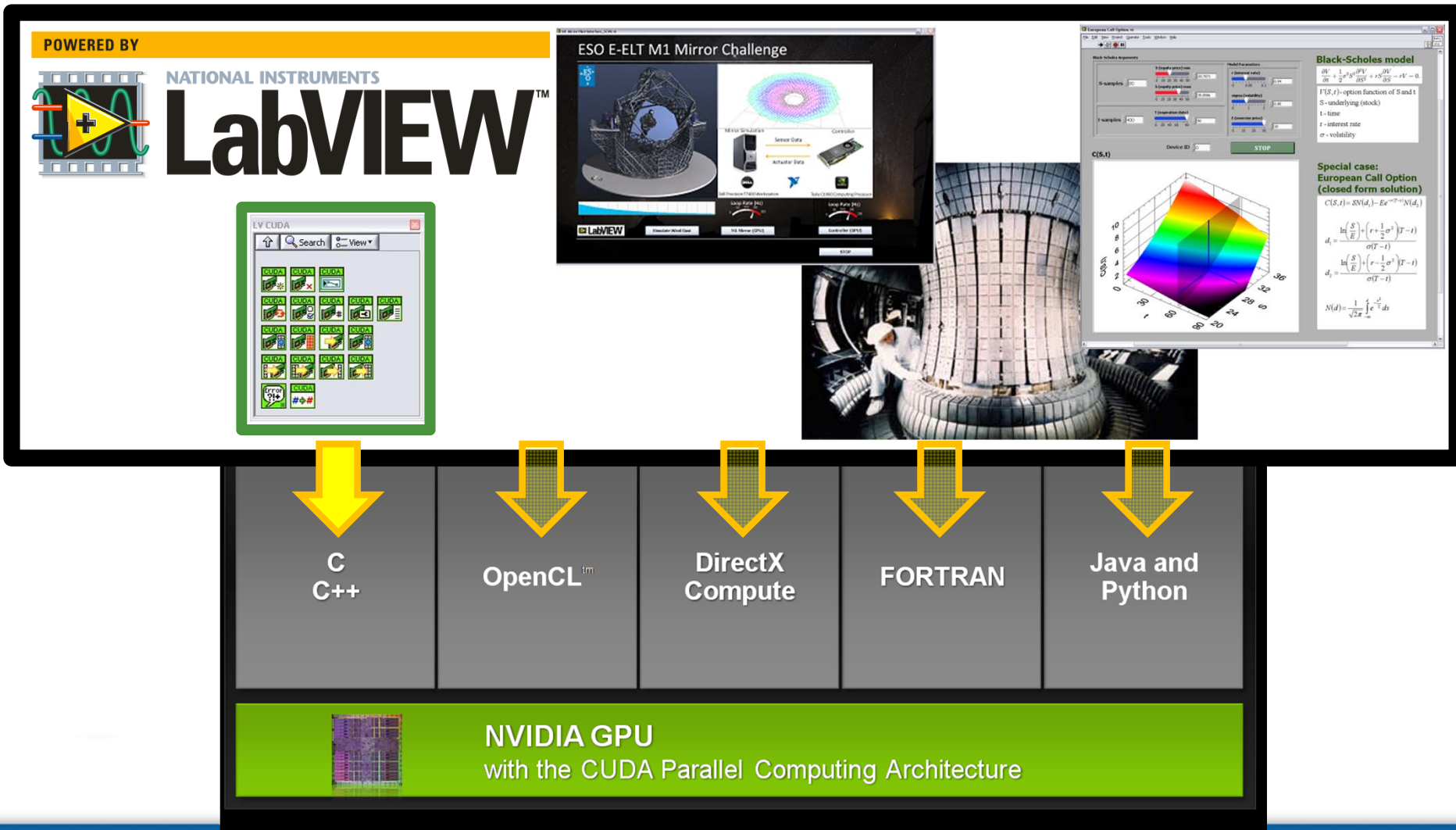


Multicore Processors

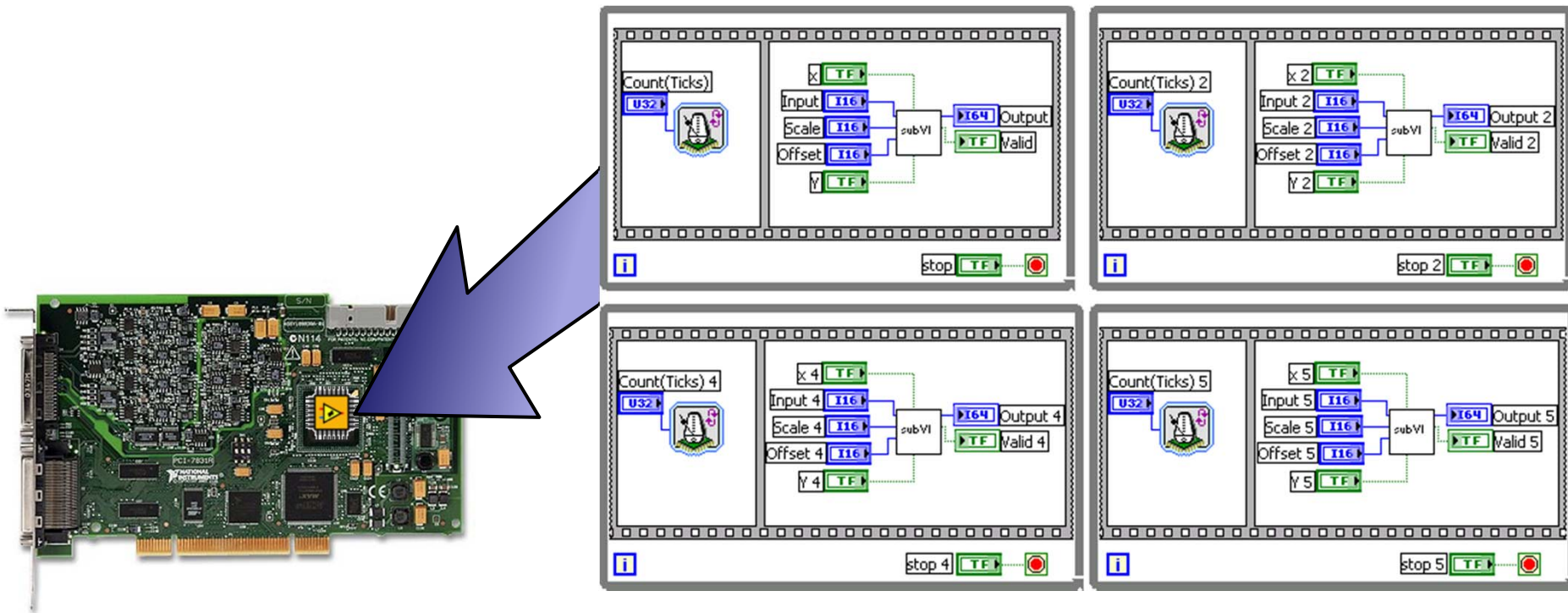


FPGAs

LabVIEW's GPU Computing Module



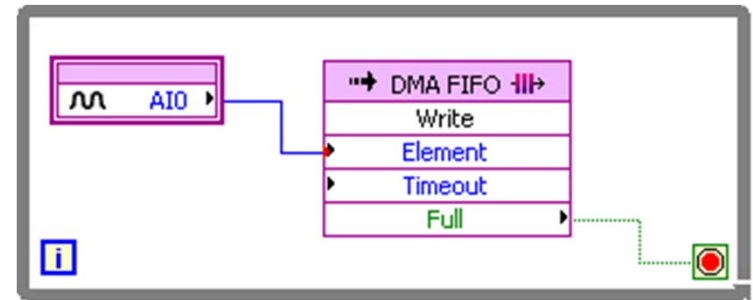
FPGA Programming: Multicore, Multiprocessor Development



Abstraction to the Pin



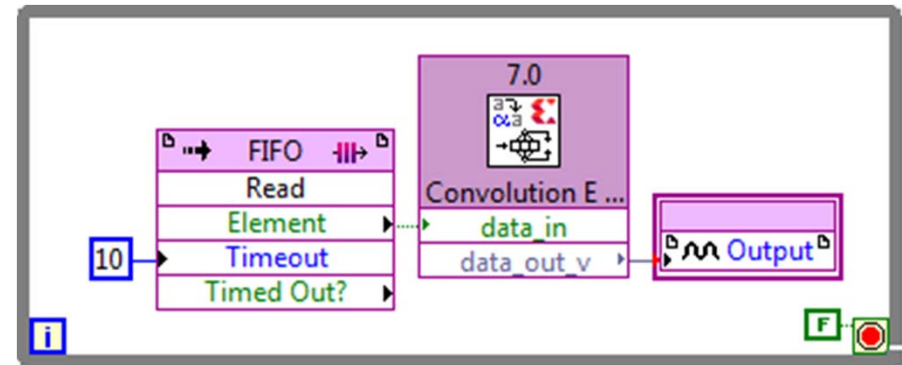
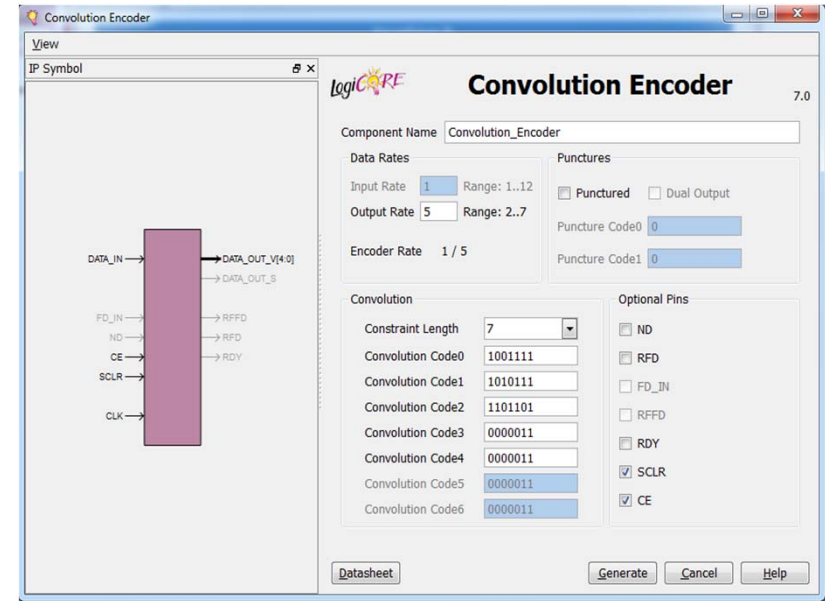
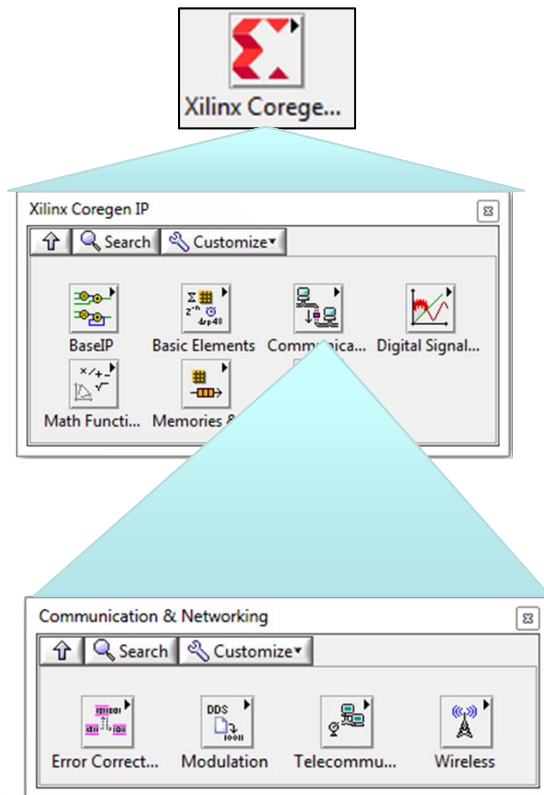
VHDL



LabVIEW FPGA

LabVIEW FPGA

Direct Access to Preexisting Xilinx CORE Generator IP Libraries



LabVIEW FPGA IP Integration Node

1

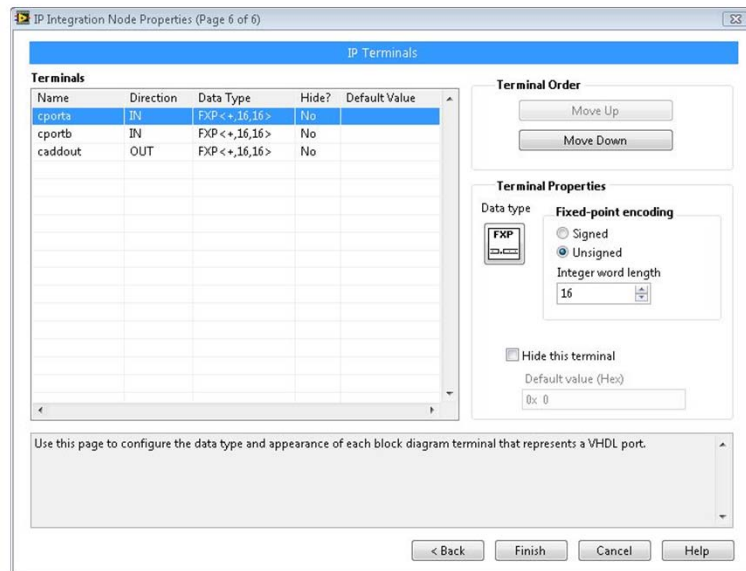
Use Core Generator or Custom VHDL



```
aclr : in    std_log
clk  : in    std_log
a    : in    std_log
b    : in    std_log
q    : out   std_log
```

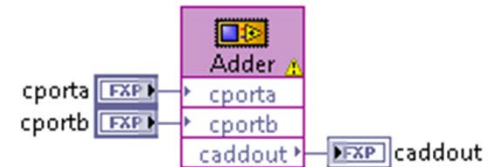
2

Configure IP Integration Node and Generate Simulation Model

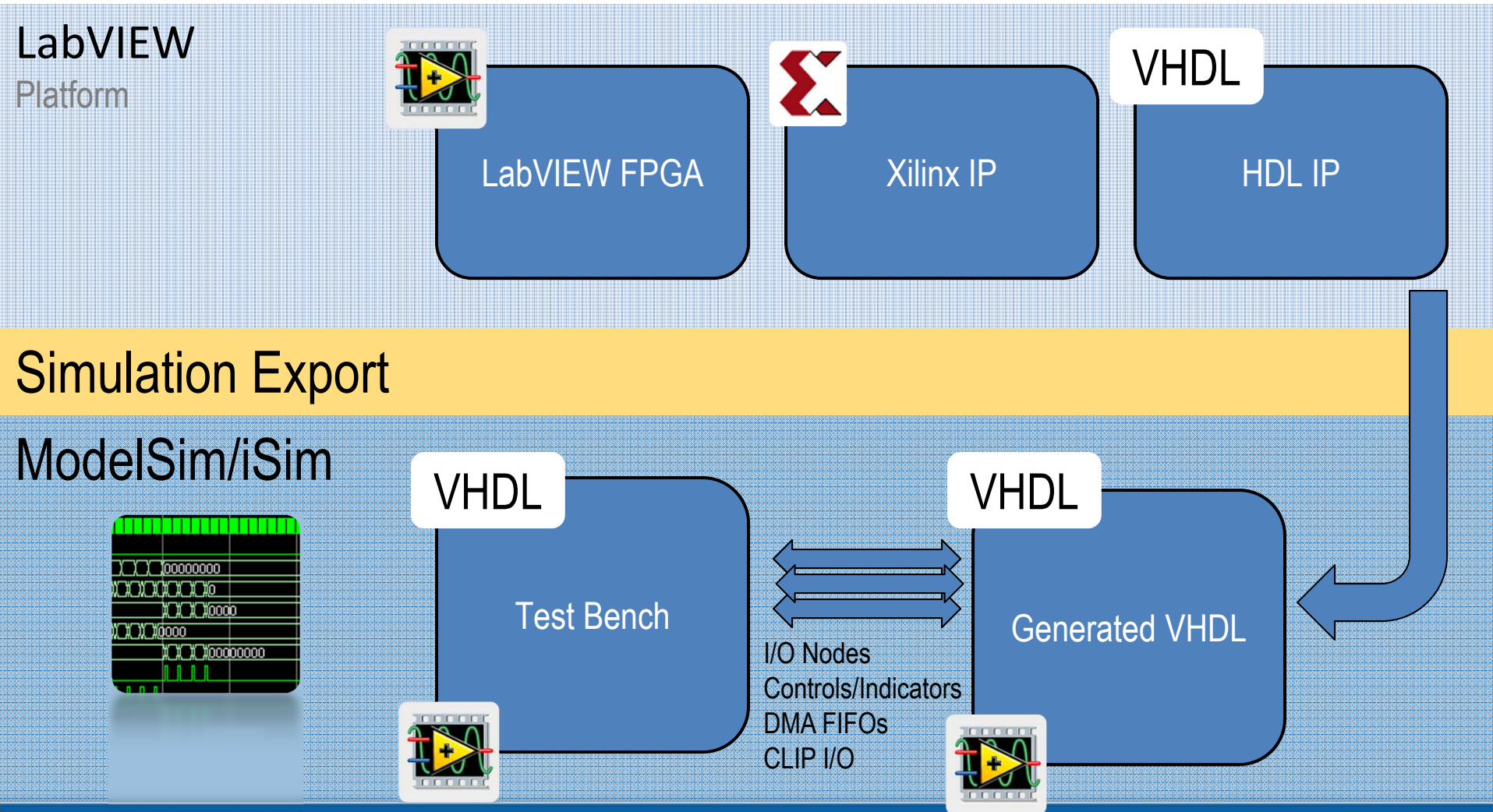


3

Use the IP Block Using Standard LabVIEW I/O Interfaces



Cycle-Accurate Simulation with ModelSim



Lawrence Livermore National Labs

Developed automated maintenance process for world's largest laser array at the National Ignition Facility using NI LabVIEW and PXI

- LabVIEW increased productivity by 3X over Java and C++
- Developed complex application consisting of over 1,000 VIs

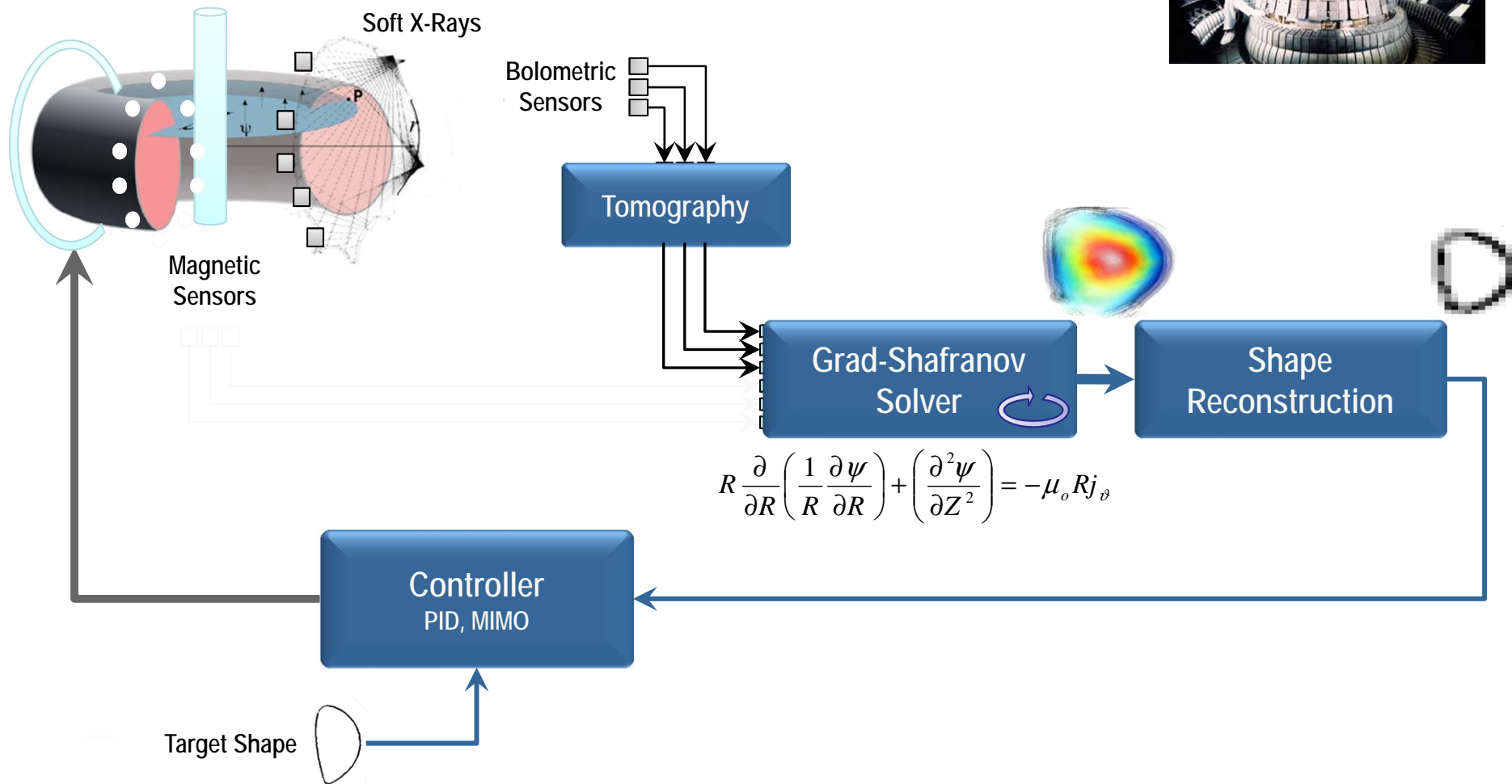


An overhead view of one of the main laser chambers

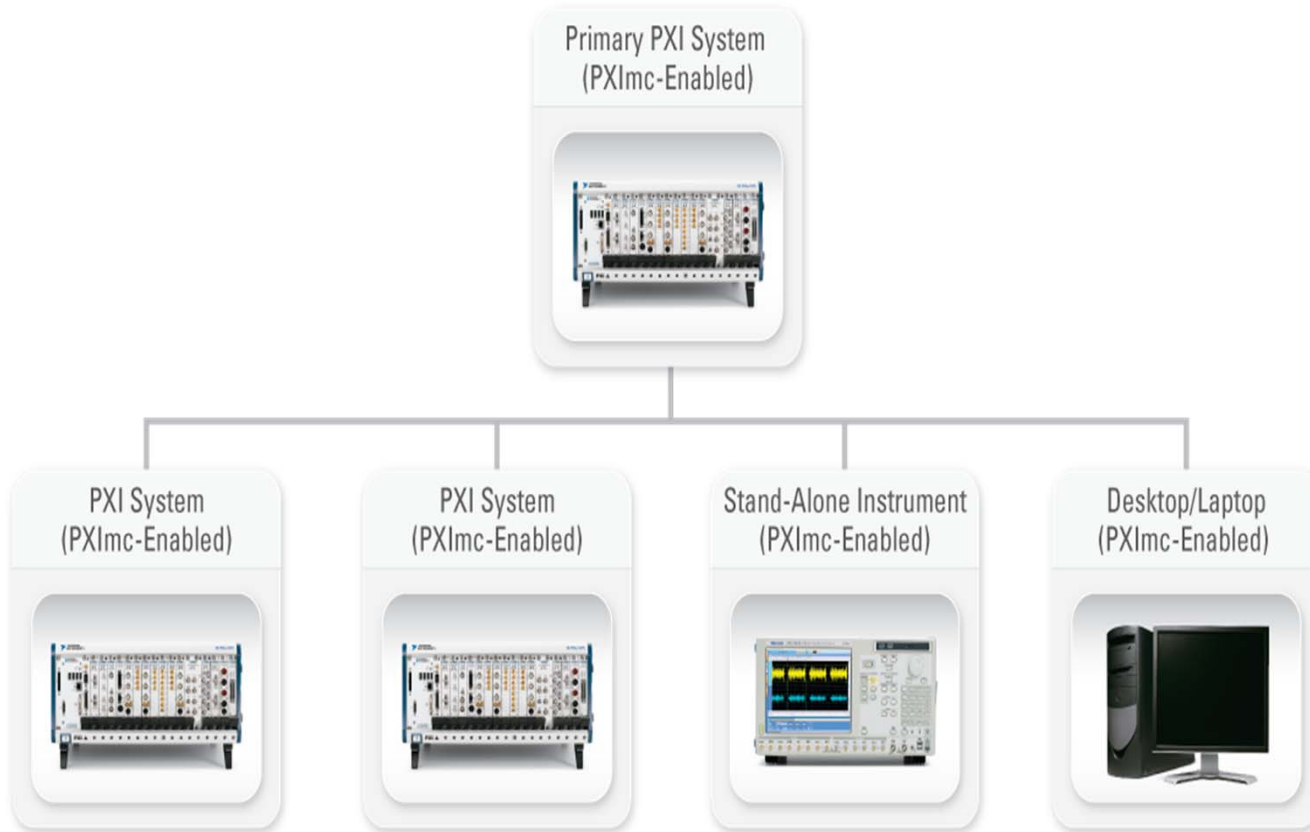
"The value in using the graphical dataflow language is the speed in which a team can deliver a robust solution while still using proper software engineering practices."

- Glenn Larkin, LLNL

Example -Tokamak – Shape Control



PXI Multi-Controller (PXImc)



One Way Latency = 6 μ S, Throughput = 670 MB/S

Plasma Diagnostics & Control with NI LabVIEW RT

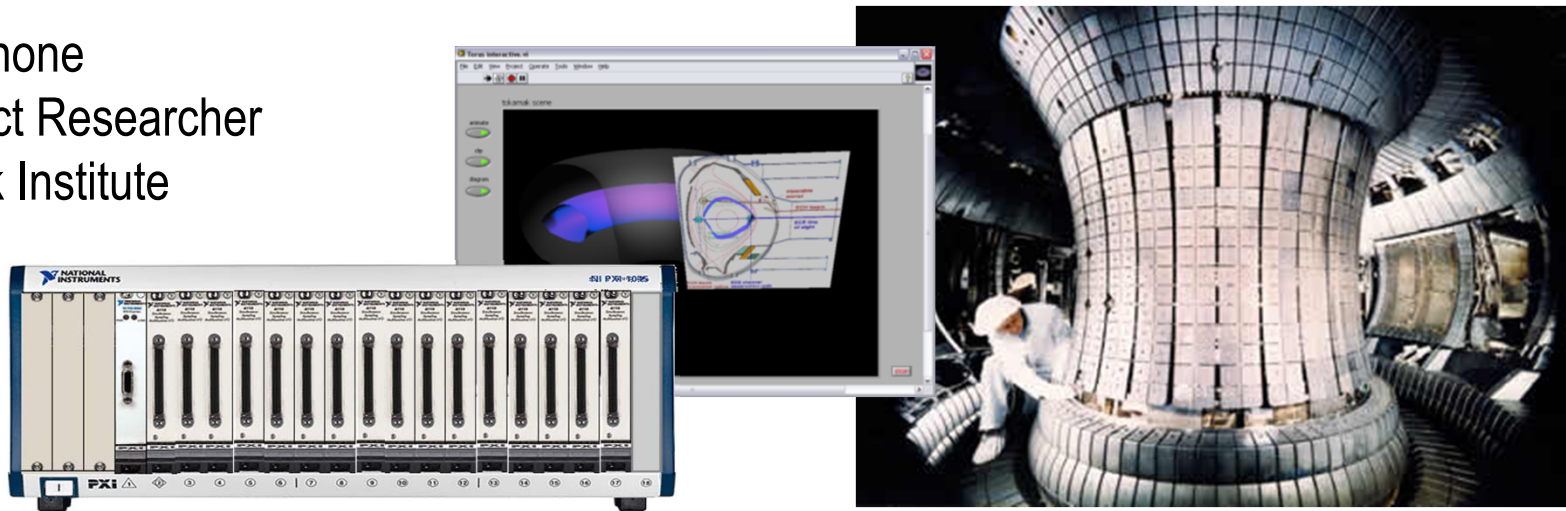


Max-Planck-Institut
für Plasmaphysik

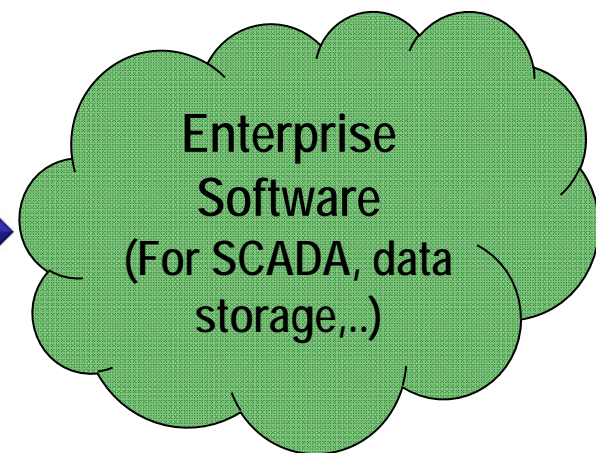
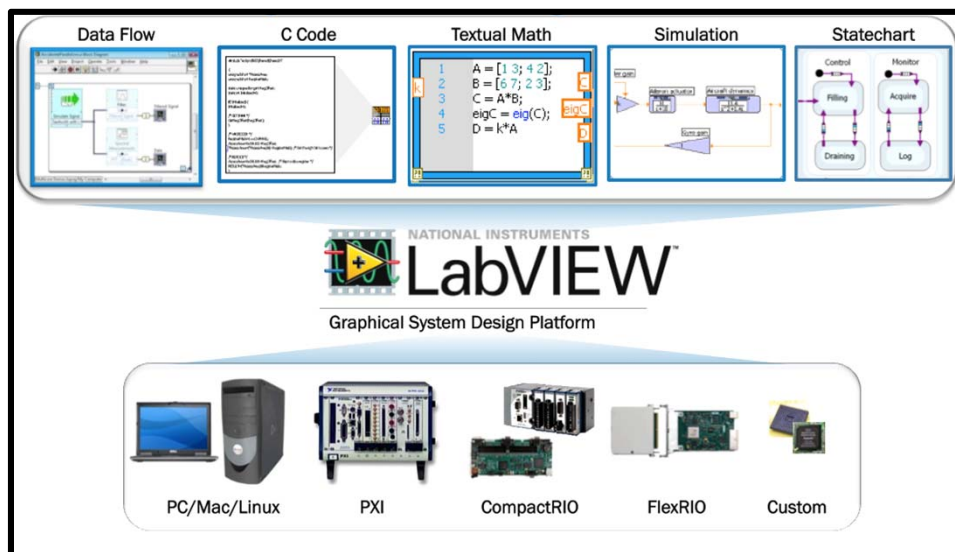
- Max Planck Institute
- Plasma control in nuclear fusion Tokamak with LabVIEW on an eight-core real-time system

"...with LabVIEW, we obtained a 20X processing speed-up on an octal-core processor machine over a single-core processor..."

Louis Giannone
Lead Project Researcher
Max Planck Institute



Open Architecture

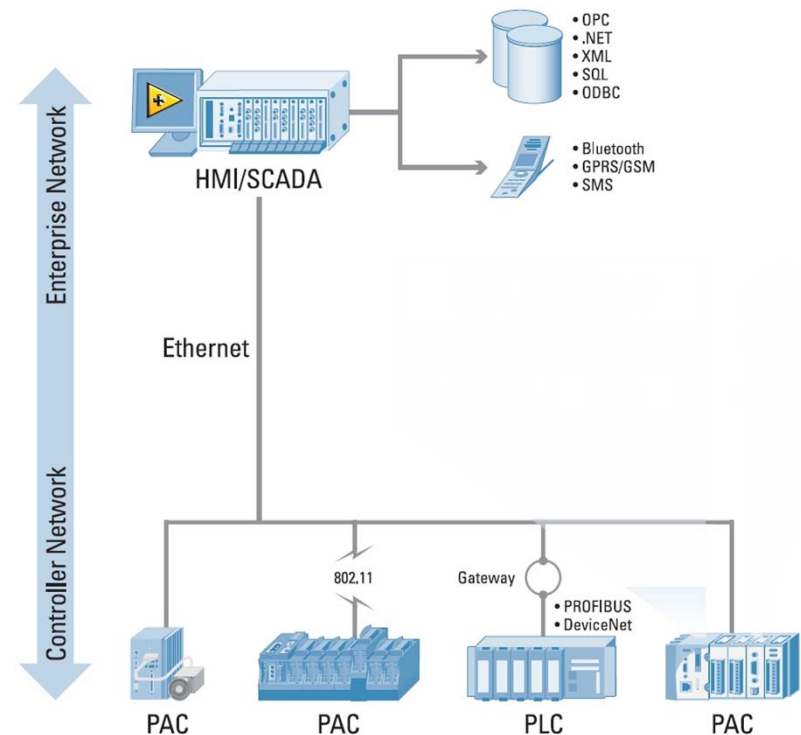


Domain Specific
Language

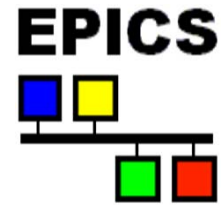
General Purpose
Language

Open Architecture

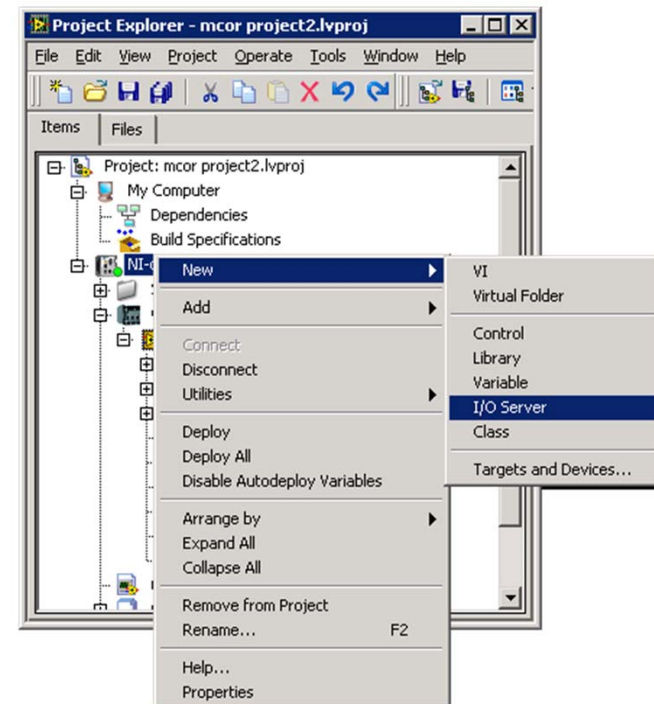
- Controls standards
 - EPICS, TANGO, CORBA, TINE, C
- Connectivity to different devices
 - OPC, Modbus, TCP/IP, UDP, EtherCAT, Serial
- Flexibility
 - Windows, RTOS, FPGA



EPICS Integration With LabVIEW

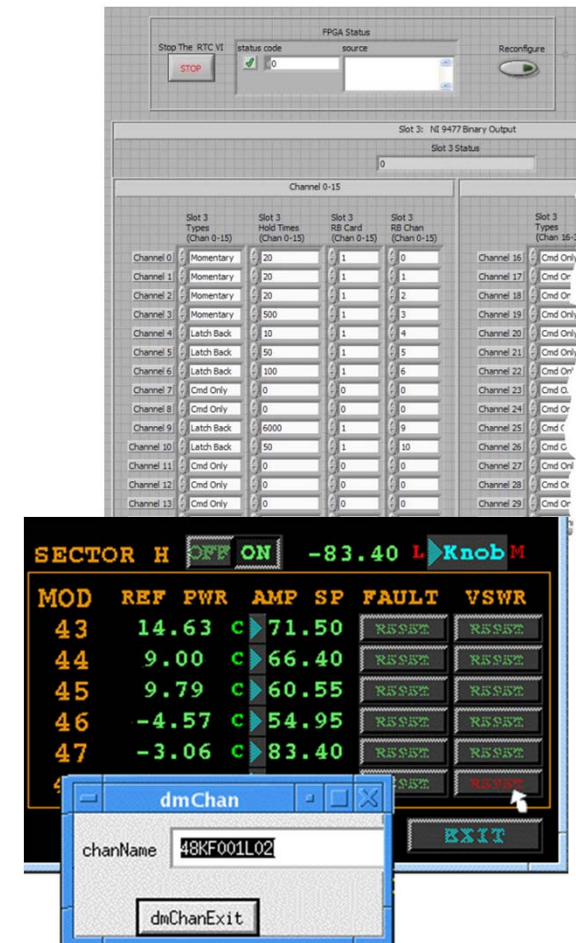


- Native LabVIEW support for Channel Access server and client
 - Windows
 - RT - VxWorks & Pharlap (Server only)
- Option to run full EPICS IOC server side by side with LabVIEW RT
 - Custom option for CompactRIO
- Prototype EPICS device driver support for FPGA-based products
 - Linux
- Linux support with Hypervisor



Example – Los Alamos LANSCE

- Ongoing migration to a cRIO system with embedded EPICS
- Full IOC functionality
- Maximum flexibility for partitioning the problem
 - LabVIEW for beam diagnostic
 - EPICS for industrial control



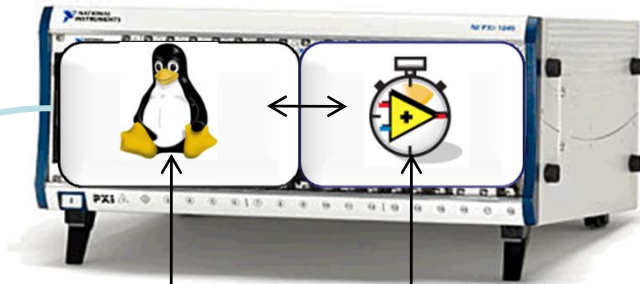
Real-Time Hypervisor for Linux

Windows PC



*Must program
LabVIEW Real-Time
application from Windows

Hypervisor System*



Supported
Linux I/O

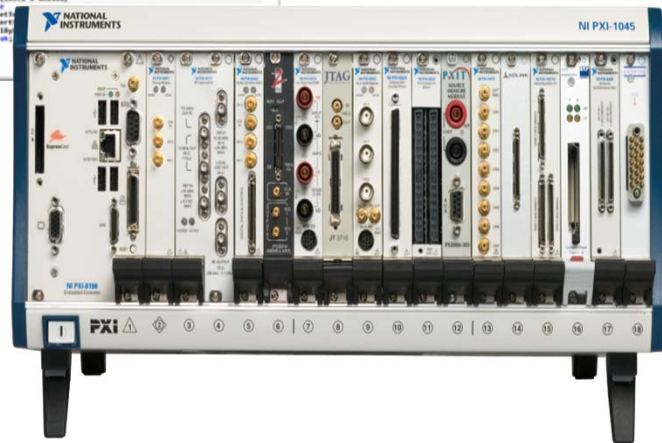


Supported
RT I/O



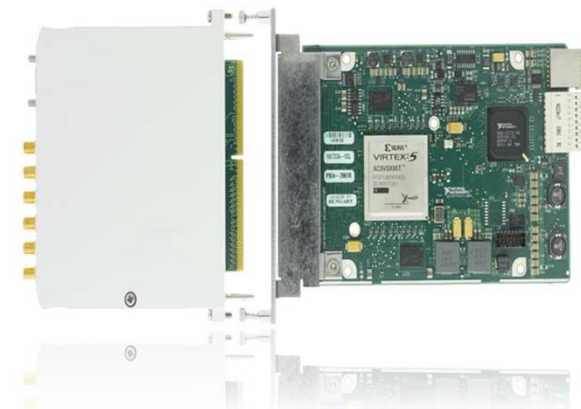
FPGA Interface C API for Linux

```
EVENT_HANDLER ON (int param, int control, int event, void *writeBufferData,  
int readBufferData, int eventData)  
  
static int param, writeBufferData;  
static char writeBuffer[1000], readBuffer[1000];  
  
if (event == EVENT_CONNECTED)  
{  
    printf("FPGA connected, PM_FPGA_FPGA, %d\n", param);  
    return (param);  
}  
  
if (event == EVENT_WRITE)  
{  
    printf("FPGA write, PM_WRITE, writeBuffer\n");  
    SetWriteBufferData(param, PM_WRITE_MID, writeBufferData, 1);  
    ProcessWriteBufferData();  
    printf("FPGA write, writeBuffer, strlen(writeBuffer)\n");  
    SetWriteBufferData(param, PM_WRITE_MID, writeBufferData, 0);  
    ProcessWriteBufferData();  
    if (strlen(writeBufferData) > 0)  
    {  
        return (param);  
    }  
}  
  
if (event == EVENT_READ)  
{  
    printf("FPGA read, PM_READ, readBufferData\n");  
    SetReadBufferData(param, PM_READ_MID, readBufferData, 1);  
    ProcessReadBufferData();  
    printf("FPGA read, readBuffer, readBufferData\n");  
    SetReadBufferData(param, PM_READ_MID, readBufferData, 0);  
    ProcessReadBufferData();  
    if (strlen(readBufferData) > 0)  
    {  
        return (param);  
    }  
}
```



Linux Target (RHEL or Scientific)

FPGA Interface
C API



NI FPGA Device

Examples – FPGA Interface C API for Linux

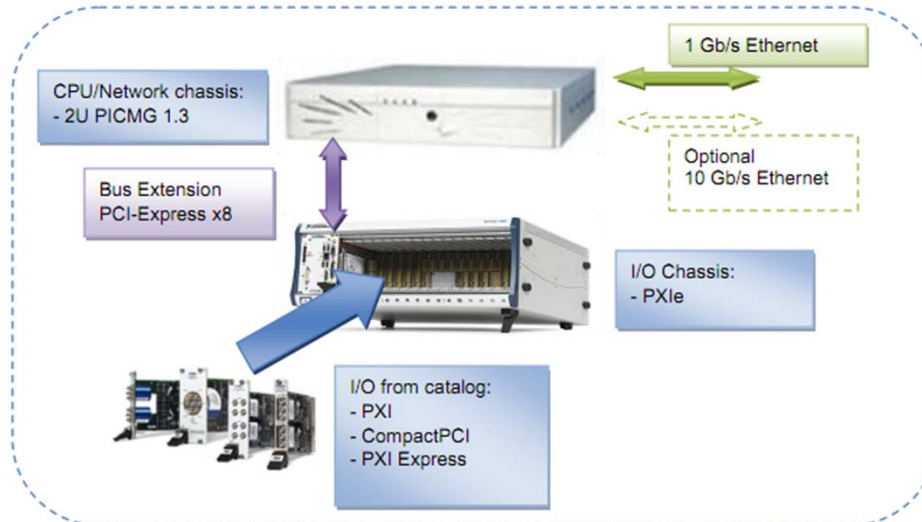


Figure 1 – A General Purpose Fast Controller

Courtesy: www.ITER.org

- Prototype for ITER Fast Controller
 - PXI FlexRIO
- Prototype for ITER Interlocks
 - CompactRIO expansion chassis

- Project under work at
 - SPring8
 - NIFS
 - PSI

Partnership with Industry

Continuous innovation

- Leverage R&D investment and latest technology
- Tools and platforms that allow faster iteration

Simplification and cost reduction

- Empower domain experts
- Open platforms to adapt vertical and emerging standards

Long term maintenance and support

- Life cycle management
- Services and consulting

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- Local technical support worldwide
- Systems engineers to assist with reference and application designs
- Active online user community and extensive online support 24 hours a day



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Calibration
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Training and Certification

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Custom Training Plans
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Professional Services
Partner-Provided Services

Alliance Partners Program



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Consulting, programming, integration, and project management

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NI & Physics Community

35 Years of Successful Cooperation

Continuous innovation

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Simplification and cost reduction

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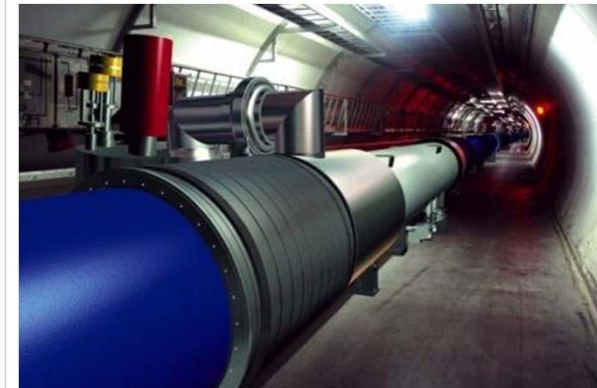
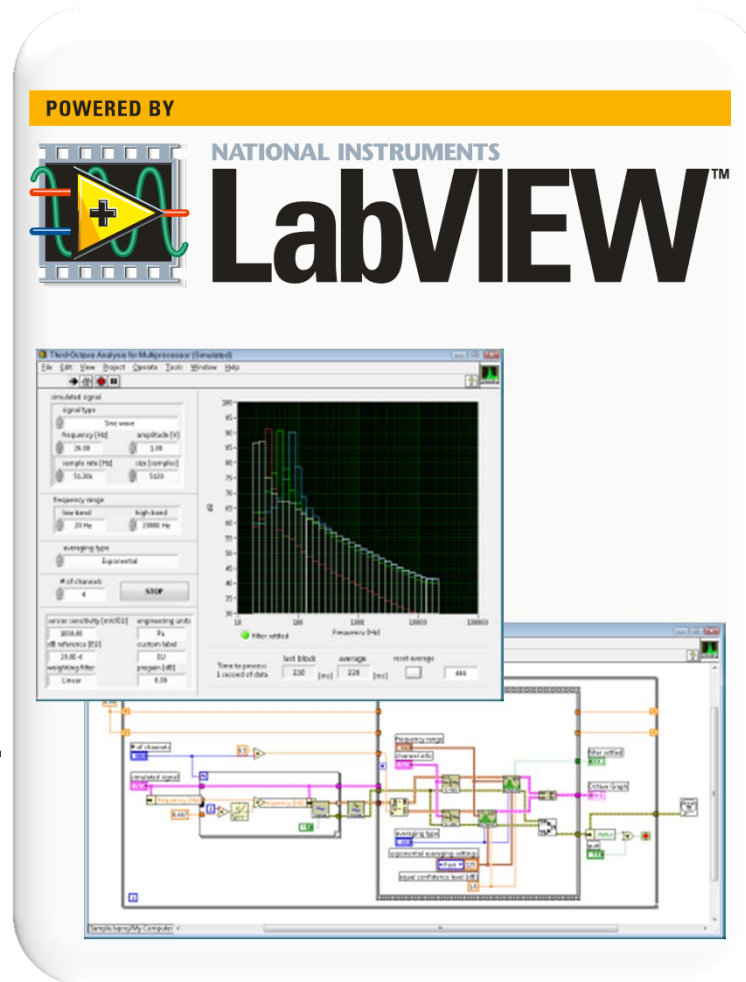
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Graphical System Design



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